Gowin AHB to AHB APB Async IP

User Guide

IPUG908-1.0E,12/12/2019

Disclaimer

Revision History

Date	Version	Description
12/12/2019	1.0E	Initial version published.

Contents

List of Figures

List of Tables

1 About This Guide

1.1 Purpose

The purpose of Gowin AHB to AHB APB Async IP User Guide is to help users learn the features and usage of Gowin AHB to AHB APB Async IP by providing the description of the functions, ports, call and configuration.

1.2 Supported Products

The information in the guide applies to all Gowin FPGA products.

1.3 Related Documents

The related latest user guides are available on our Website: www.gowinsemi.com

1.4 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FIFO	First Input First Output
IP	Intellectual Property
RAM	Random Access Memory
BSRAM	Block Static Random Access Memory
SSRAM	Shadow Static Random Access Memory
LUT	Look-up Table
REG	Register
AHB	Advanced High Performance Bus

Terminology and Abbreviations	Meaning
APB	Advanced Peripheral Bus

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail:support@gowinsemi.com

Tel: +86 755 8262 0391

2 Overview

2.1 Introduction to Gowin AHB to AHB APB Async IP

There are two main features of Gowin AHB to AHB APB Async IP:

- An AHB bus master device communicates with an AHB bus slave device;
- An AHB bus master device communicates with an asynchronous APB bus slave device.

Table 2-1 Gowin AHB to AHB APB Async IP

Gowin AHB to AHB APB Async IP	
IP Core Application	
Supported Devices	Gowin all FPGA products
Logic Resource	See Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Test and Design Flow	
Synthesis Software	Synplify_Pro
Application Software	GowinYunYuan

2.2 Key Feature

The master width can be configured: 1,2,3,4.

2.3 Resource Utilization

Gowin AHB to AHB APB Async IP is implemented by Verilog, and its resources vary greatly due to different configurations. Take the default configuration and master width =1 as an example, resource utilization is as shown in Table 2-2.

Table 2-2 Resource Utilization of Gowin AHB to AHB APB Async IP

Device	Speed Grade	Name	Resource Utilization	Remarks
GW2A-18	C8/I7	LUT	197	Master Width = 1
		REG	123	

3 Functional Description

There are two main features of Gowin AHB to AHB APB Async IP:

- An AHB bus master device communicates with an AHB bus slave device;
- An AHB bus master device communicates with an asynchronous APB bus slave device.

The master width can be configured: 1,2,3,4.

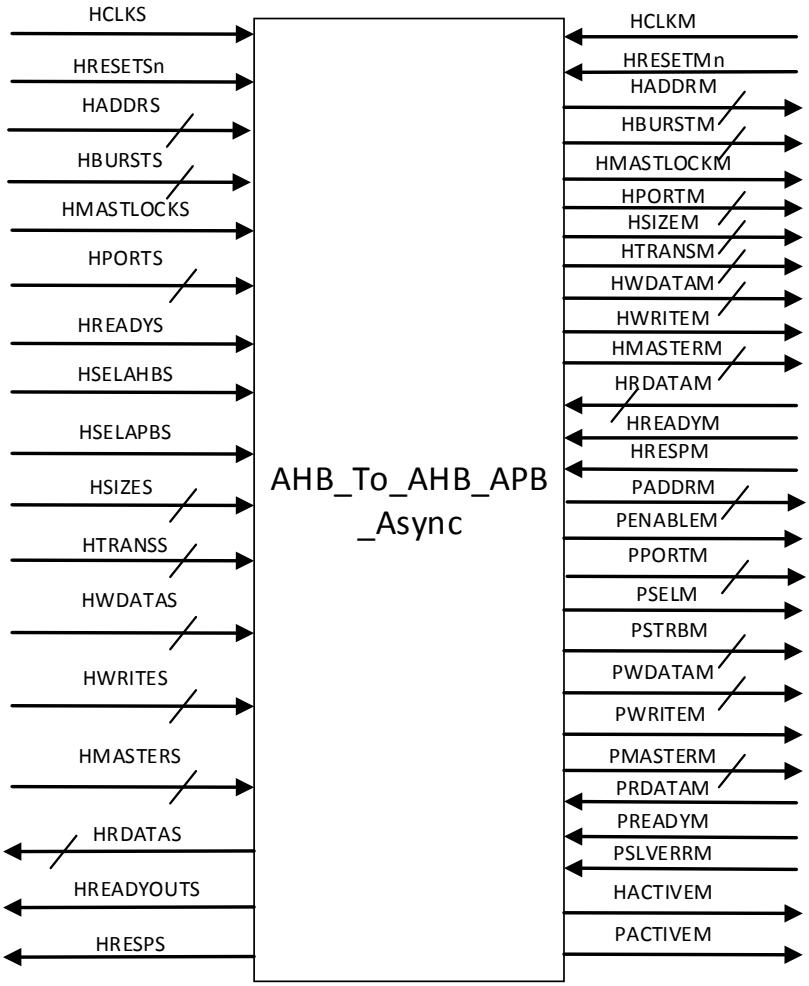
Note!

If a master is with the ability of multithreading, the master width can be configured as 2, 3, 4 to distinguish.

4 Port Description

The ports of Gowin AHB to AHB APB Async IP are as shown in Figure 4-1.

Figure 4-1 Ports of Gowin AHB to AHB APB Async IP



The details of Gowin AHB to AHB APB Async IP I/O ports are shown in Table 4-1.

Table 4-1 Ports Description of Gowin AHB to AHB APB Async IP

Name	I/O	Bit Width	Description
AHB-Lite slave interface			
HCLKS	Input	1	System clock
HRESETSn	Input	1	Reset signal, active-low
HADDRS	Input	32	AHB 32-bit system address bus
HBURSTS	Input	3	AHB burst signal
HMASTLOCKS	Input	1	The signal is high, indicating the current transmission has locked one sequence; The sequence is the same as the one of the address and control signal.
HPROTS	Input	4	Protect and control signal, providing additional information for bus access.
HREADYS	Input	1	The signal is high, indicating transmission completed on the bus.
HSELAHBS	Input	1	The signal is high, indicating the bus bridge receiving AHB signal and sending it to the device on AHB interface; This signal and HSELAPBS can not be high at the same time.
HSELAPBS	Input	1	The signal is high, indicating the bus bridge receiving AHB signal and converting to APB signal, then sending it to the device on APB interface; This signal and HSELAHBS can not be high at the same time.
HSIZES	Input	3	The data size; The typical units are byte, nibble and word.
HTRANSS	Input	2	The transmission type
HWDATAS	Input	32	AHB write data
HWRITES	Input	1	AHB write enable
HMASTERS	Input	Master Width-1	Indicating which bus master is transmitting
HRDATAS	Output	32	AHB read data
HREADYOUTS	Output	1	The signal is high, indicating transmission completed on the bus.
HRESPS	Output	1	Response signal; High, error and low, okay
AHB-Lite master interface			
HCLKM	Input	1	System clock
HRESETMn	Input	1	Reset signal, active-low
HADDRM	Output	32	AHB 32-bit system address bus
HBURSTM	Output	3	AHB burst signal
HMASTLOCKM	Output	1	The signal is high, indicating the current transmission has locked one sequence; The sequence is the same as the one of the address and

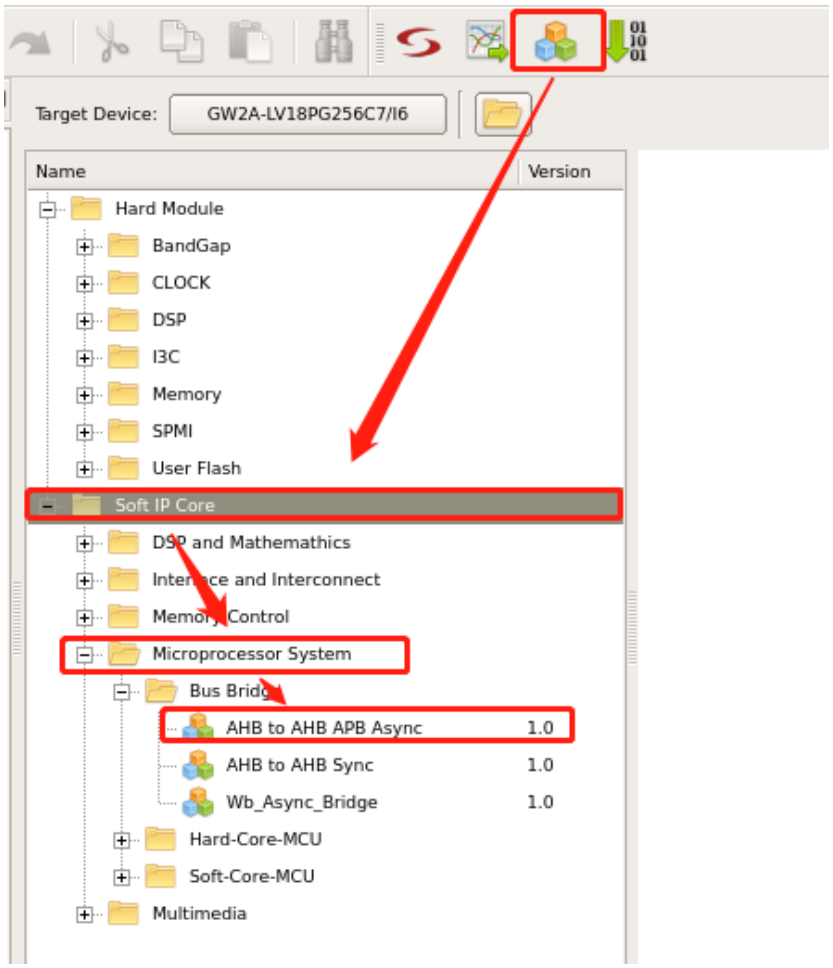
Name	I/O	Bit Width	Description
			control signal.
HPROTM	Output	4	Protect and control signal, providing additional information for bus access.
HSIZEM	Output	3	The data size; The typical units are byte, nibble and word.
HTRANSM	Output	2	The transmission type
HWDATAM	Output	32	AHB write data
HWRITEM	Output	1	AHB write enable
HMASTERM	Output	Master Width-1	Indicating which bus master is transmitting
HRDATAM	Input	32	AHB read data
HREADYM	Input	1	The signal is high, indicating transmission completed on the bus.
HRESPM	Input	1	Response signal; High, error and low, okay
APB master interface			
PADDRM	Output	32	32-bit APB address bus
PENABLEM	Output	1	APB enable signal
PPROTM	Output	3	APB protect and control signal, providing additional information for bus access.
PSELM	Output	1	The slave device is selected and one transmission is requested.
PSTRBM	Output	4	Used to indicate byte lanes in write; It is 1 in read.
PWDATAM	Output	32	APB write data
PWRITEM	Output	1	APB write enable
PMASTERM	Output	Master Width-1	Indicating which bus master is transmitting
PRDATAM	Input	32	APB read data
PREADYM	Input	1	The signal is high, indicating one bus transmission completed.
PSLVERRM	Input	1	The signal is high, indicating one bus transmission failed.
HACTIVEM	Output	1	Gate signal of AHB system clock
PACTIVEM	Output	1	Gate signal of APB system clock APB

5 Call and Configuration

5.1 Gowin AHB to AHB APB Async IP Call

Select "Tools > IP Core Generator > Soft IP Core > messenger > Bus Bridge > AHB to AHB APB Async" on the interface of Gowin Yun Yuan software to complete the call of Gowin AHB to AHB APB Async IP, as shown in Figure 5-1.

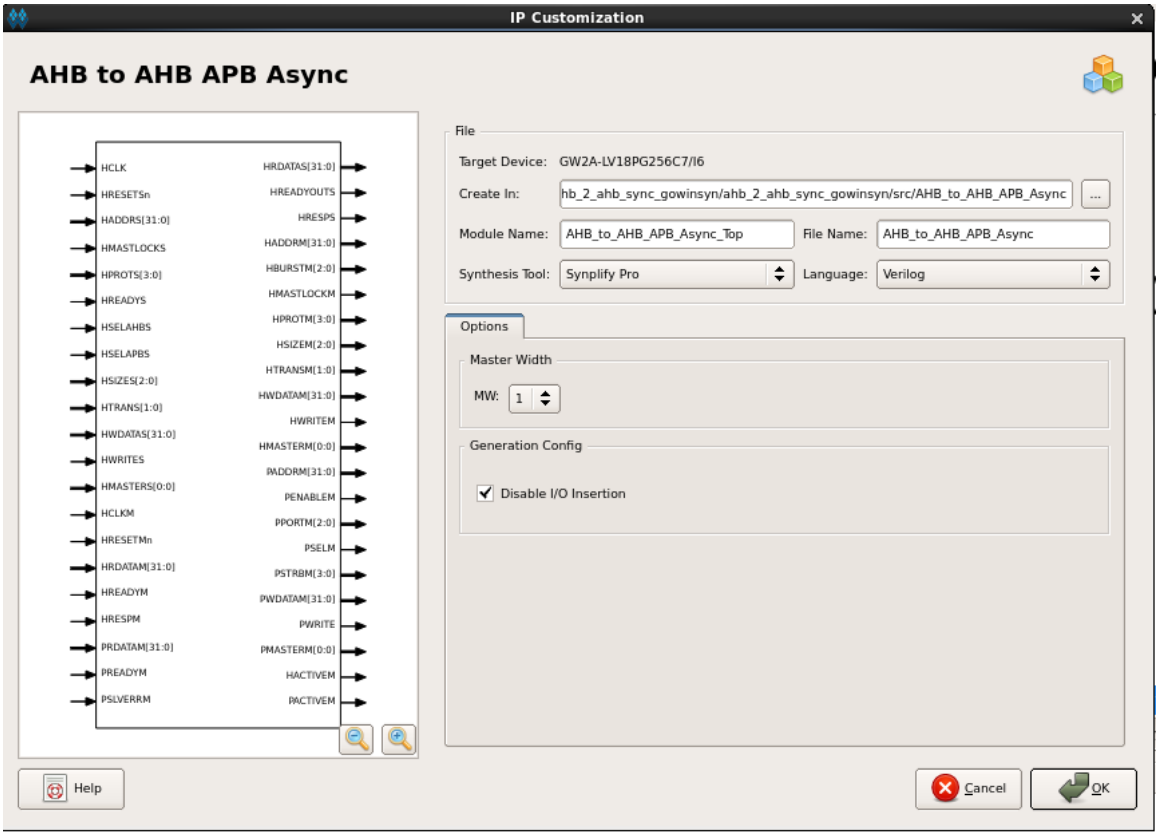
Figure 5-1 Gowin AHB to AHB APB Async IP Call



5.2 Gowin AHB to AHB APB Async IP Configuration

The configuration interface of Gowin AHB to AHB APB Async IP is as shown in Figure 5-2.

Figure 5-2 Configuration Example of Gowin AHB to AHB APB Async IP



1. Click "Create In" to change the path of the file generated by Gowin AHB to AHB APB Async IP.
2. Click "Module Name" to configure the generated top module name of Gowin AHB to AHB APB Async IP;
3. Click "File Name" to configure the generated file name of Gowin AHB to AHB APB Async IP;
4. Click "Option" to configure the master width: 1,2,3,4.

Note!

Master Width=1 by default.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