



Gowin AHB to AHB Sync IP

User Guide

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Revision History

Date	Version	Description
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1 About This Guide

1.1 Purpose

The purpose of Gowin AHB to AHB Sync IP User Guide is to help users learn the features and usage of Gowin AHB to Gowin AHB to AHB Sync IP by providing the description of the functions, ports, configuration and call.

1.2 Supported Products

The information in the guide applies to all Gowin FPGA products.

1.3 Related Documents

The latest user guides are available on our Website:
www.gowinsemi.com

1.4 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FIFO	First Input First Output
IP	Intellectual Property
RAM	Random Access Memory
BSRAM	Block Static Random Access Memory
SSRAM	Shadow Static Random Access Memory
LUT	Look-up Table
REG	Register
AHB	Advanced High performance Bus

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

Tel: +86 755 8262 0391

2 Overview

2.1 Introduction to Gowin AHB to AHB Sync IP

The main feature of Gowin AHB to AHB Sync IP is that an AHB bus master device communicates with an AHB bus slave device.

Table 2-1 Gowin AHB to AHB APB Async IP

Gowin AHB to AHB Sync IP	
IP Core Application	
Supported Devices	Gowin all FPGA products
Logic Resource	See Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Test and Design Flow	
Synthesis Software	Synplify_Pro
Application Software	GowinYunYuan

2.2 Key Feature

The master width can be configured: 1,2,3,4.

2.3 Resource Utilization

Gowin AHB to AHB Sync IP is implemented by Verilog, and its resources vary greatly due to different configurations. Take the default configuration and master Width =1 as an example, resource utilization is as shown in Table 2-2.

Table 2-2 Resource Utilization of Gowin AHB to AHB Sync IP

Device	Speed Grade	Name	Resource Utilization	Remarks
GW2A-18	C8/I7	LUT	54	Master Width = 1
		REG	89	

3 Functional Description

The main feature of Gowin AHB to AHB Sync IP is that an AHB bus master device communicates with an AHB bus slave device.

The master width can be configured: 1,2,3,4.

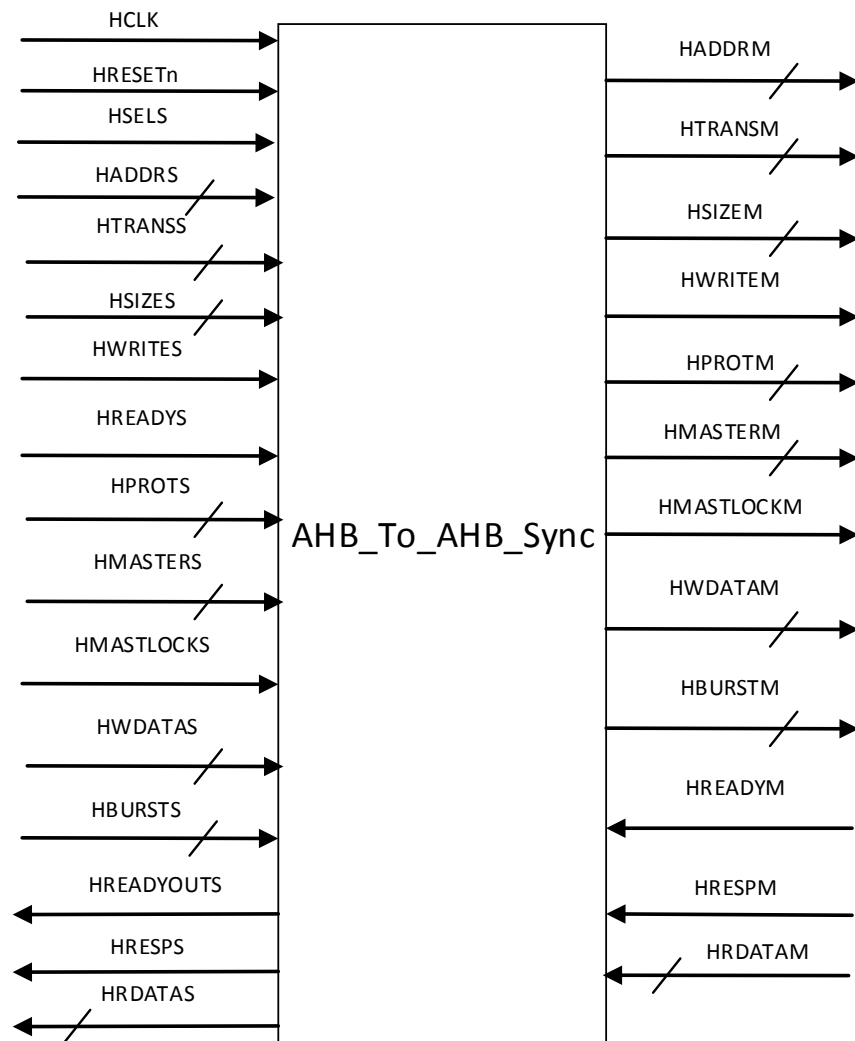
Note!

If a master is with the ability of multithread, the master width can be configured as 2, 3, 4 to distinguish.

4 Port Description

The ports of Gowin AHB to AHB Sync IP are as shown in Figure 4-1.

Figure 4-1 Ports of Gowin AHB to AHB Sync IP



The details of Gowin AHB to AHB Sync IP I/O ports are shown in Table

4-1.

Table 4-1 Ports Description of Gowin AHB to AHB Sync IP

Name	I/O	Bit Width	Description
AHB connection to master			
HCLK	Input	1	System clock
HRESETn	Input	1	Reset signal, active-low
HSELS	input	1	Indicating whether the current slave is selected; Each AHB slave has its own selection signal.
HADDRS	Input	32	AHB 32-bit system address bus
HTRANS	Input	2	Transmission type
HSIZES	Input	3	Data size; The typical units are byte, nibble and word
HWRITES	Input	1	AHB write enable
HREADY	Input	1	The signal is high, indicating the bus transmission completed.
HPROT	Input	4	Protect and control signal, providing additional information for bus access
HMASTERS	Input	Master Width-1	Indicating which bus master is transmitting
HMASTLOCKS	Input	1	The signal is high, indicating the current transmission has locked one sequence; The sequence is the same as the one of address and control signals.
HWDATAS	Input	32	AHB write data
HBURSTS	Input	3	AHB burst signal
HREADYOUTS	Output	1	The signal is high, indicating the bus transmission completed.
HRESPS	Output	1	Response signal; High, error and low, okay.
HRDATAS	Output	32	AHB read data
AHB connection to slave			
HADDRM	Output	32	AHB 32-bit system address bus
HTRANS	Output	2	Transmission type
HSIZEM	Output	3	Data size; The typical units are byte, nibble and word.
HWRITEM	Output	1	AHB write enable
HPROTM	Output	4	Protect and control signal, providing additional information for bus access
HMASTERM	Output	Master Width-1	Indicating which bus master is transmitting
HMASTLOCKM	Output	1	The signal is high, indicating the current transmission has locked one sequence; The sequence is the same as the one of address and control signals.

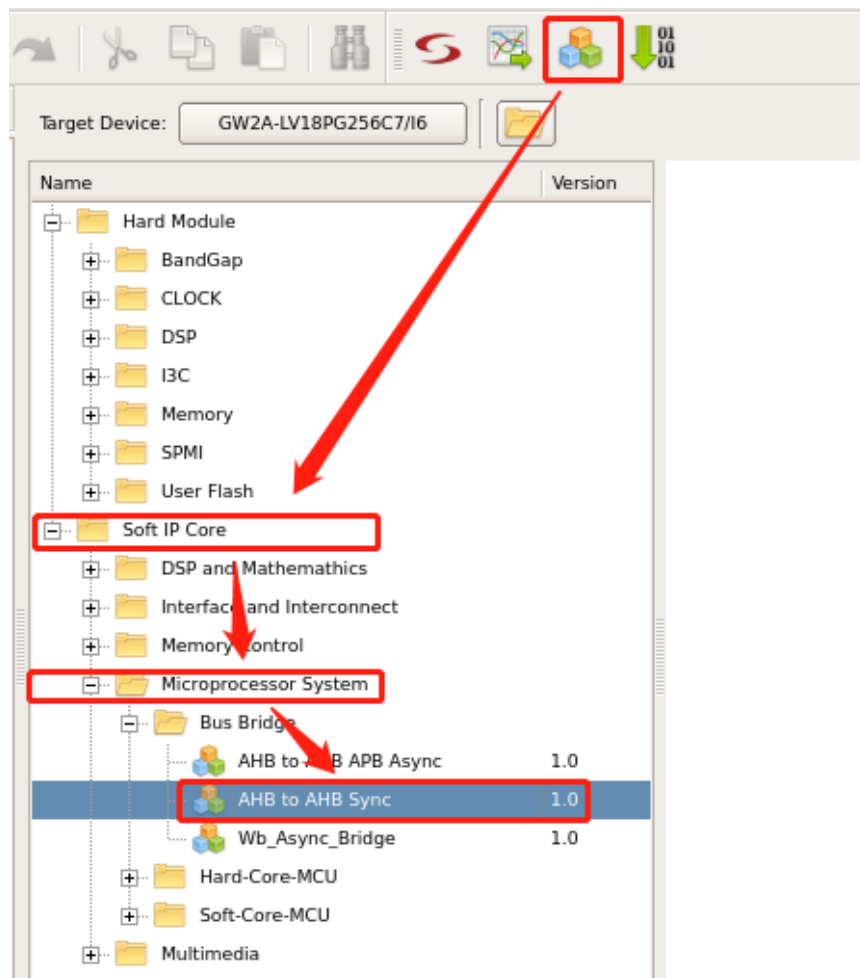
Name	I/O	Bit Width	Description
HWDATAM	Output	32	AHB write data
HBURSTM	Output	3	AHB burst signal
HREADYM	Input	1	The signal is high, indicating the bus transmission completed.
HRESPM	Input	1	Response signal; High, error and low, okay.
HRDATAM	Input	32	AHB read data

5 Call and Configuration

5.1 Gowin AHB to AHB Sync IP Call

Select "Tools > IP Core Generator > Soft IP Core > messenger > Bus Bridge > AHB to AHB APB Async" on the interface of Gowin Yun Yuan software to complete the Gowin AHB to AHB Sync IP call, as shown in Figure 5-1.

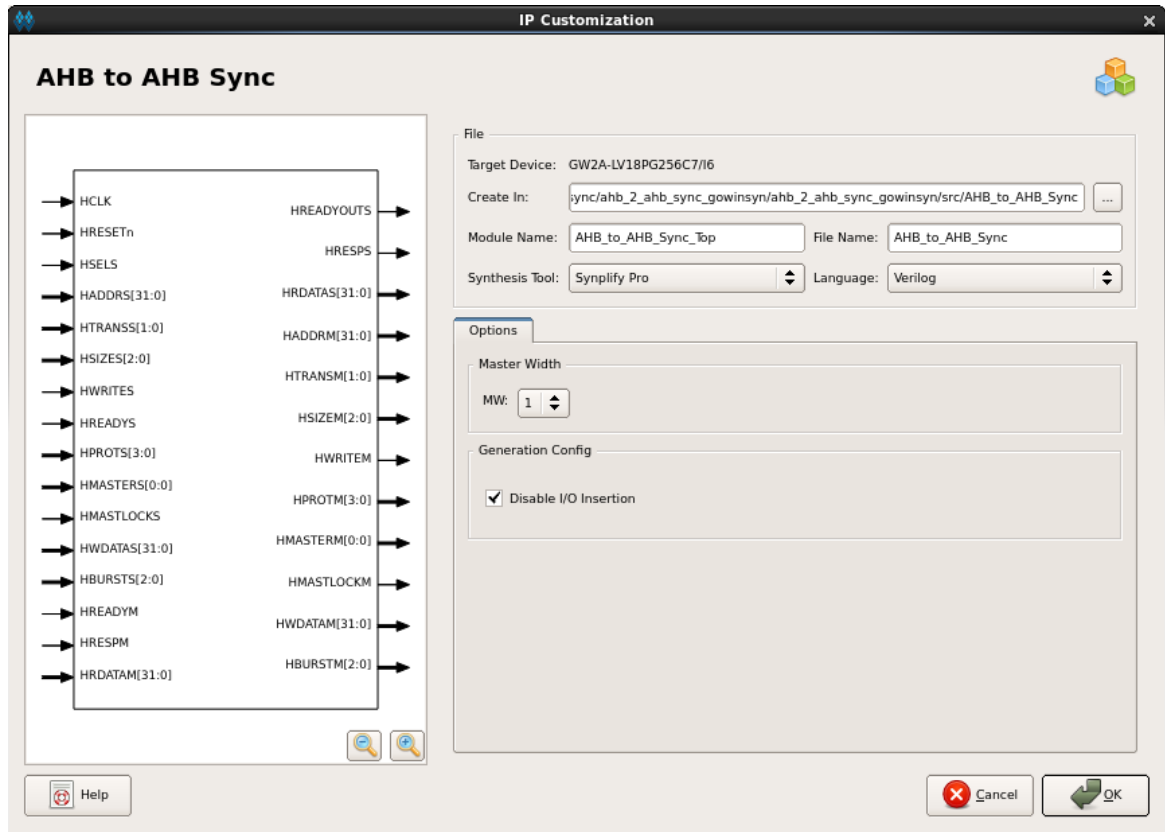
Figure 5-1 Gowin AHB to AHB APB Async IP Call Example



5.2 Gowin AHB to AHB Sync IP Configuration

The configuration interface of Gowin AHB to AHB Sync IP is as shown in Figure 5-2.

Figure 5-2 Gowin AHB to AHB Sync IP Configuration Example



1. Click "Create In" to change the path of the file generated by Gowin AHB to AHB Sync IP.
2. Click "Module Name" to configure the generated top module name of Gowin AHB to AHB Sync IP;
3. Click "File Name" to configure the generated file name of Gowin AHB to AHB Sync IP;
4. Click "Option" to configure the master width: 1,2,3,4.

Note!

Master Width=1 by default.

