Gowin RiscV N25

Release Note

RN528-1.0E, 2019-01-17

Disclaimer

Revision History

Date	Version	Description
1/17/2019	1.0E	● IP Core Generator supports RiscV N25; ● The RiscV N25 reference design released.

Contents

1 About This Release

Gowin RiscV N25 released, and the RiscV N25 soft core can be generated by IP Core Generator.

Gowin RiscV N25 reference design is available at Gowin Website. Specific parameter had been taken as an example for the reference design, which can be used for the overall synthesis, placement and routing after user design. The IP can be reconfigured, and the reference design supports the reconfigured IP to a certain extent. If simulation is required, write the C bin binary program to one SPI Flash model and hook it to the system SPI1 channel. The MCU start address is the 2MB address.

2 Overview

Gowin RiscV N25 IP can be applied to the embedded designs. It supports the CPU core of the min. system and the high performance SOC of the max. system. RiscV N25 provides multiple configurable systems, including high-speed instructions memory system, high-speed data memory system, flexible interrupt system, direct memory access system, system management unit, system clock, real-time clock, and serial bus control system such as GPIO, SPI, UART, etc.

Table 2-1 RiscV N25 Overview

RiscV N25	
IP Core Application	
Supported Devices	GW1N, GW1NR series GW2A, GW2AR series
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Designs	Verilog
TestBench	---
Test and Design Flow	
Synthesis Software	Synplify_Pro
Application Software	GowinYunYuan

3 Documents

This IP release file contains RiscV N25 User Guide, which is listed below.

Documents	Access
Gowin RiscV N25 User Manual.pdf	PDF

4 IP Support

Since the requirements of user design and the highest frequency are different, the reference design does not include associated FPGA specific location (.cst) and timing constraints (.sdc) documents, which the user can determine as required.

Only one pins constraint file specially designed for the demo version of DK-START-GW2A18 V2.0 is provided. Users can design your project pins constraint file on this basis.

Please notice the readme.txt in reference designs.

For the customized IP design and support, please contact Gowin sales and support line.

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