



Gowin_EMPU_M1

Quick Design Reference Manual

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Revision History

Date	Version	Description
2/19/2019	1.0E	Initial version published.

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1 Reference Design

1.1 Gowin_EMPU_M1 Software Reference Design

Gowin provides Gowin_EMPU_M1 software reference design with Keil and GNU software environment: MCU_RefDesign\Keil_RefDesign and GNU_RefDesign

1.2 Gowin_EMPU_M1 Hardware Reference Design

Gowin_EMPU_M1 hardware reference design is provided by Gowin:

- FPGA_RefDesign\Debug_RefDesign and NoDebug_RefDesign
 - The reference design includes two parts:
- Cortex-M1 core
- AHB-Lite interface, extension AHB, and APB peripheral interface

1.2.1 Cortex-M1

The configured functions of Cortex-M1 are shown in the Table 1-1.

Table 1-1 Cortex-M1 Functions of the Reference Design

Function Mode	Configuration
Number of external interrupts	32
Extended operation system	Supported
Data storage format	Little-endian format
MULT	Standard mode
Debugger	Integrated mode, four break points and two observation points
Debug interface	Support JTAG and Serial Wire interfaces
ITCM size	32KB
ITCM Initialization value	Enable
ITCM Initialization path	The itcm0, itcm1, itcm2, and itcm3 path of LED case
ITCM alias	Lower alias
DTCM size	32KB

1.2.2 AHB-Lite

The configured peripheral interfaces of AHB-Lite are shown in Table 1-2.

Table 1-2 The Configuration of AHB-Lite Peripheral Interface

Peripheral Interface	Configuration
UART0	Supported
UART1	Supported
GPIO port 0	Supported
Timer 0	Supported
Timer 1	Supported
Watchdog	Supported

2 Gowin_EMPU_M1 Software Design

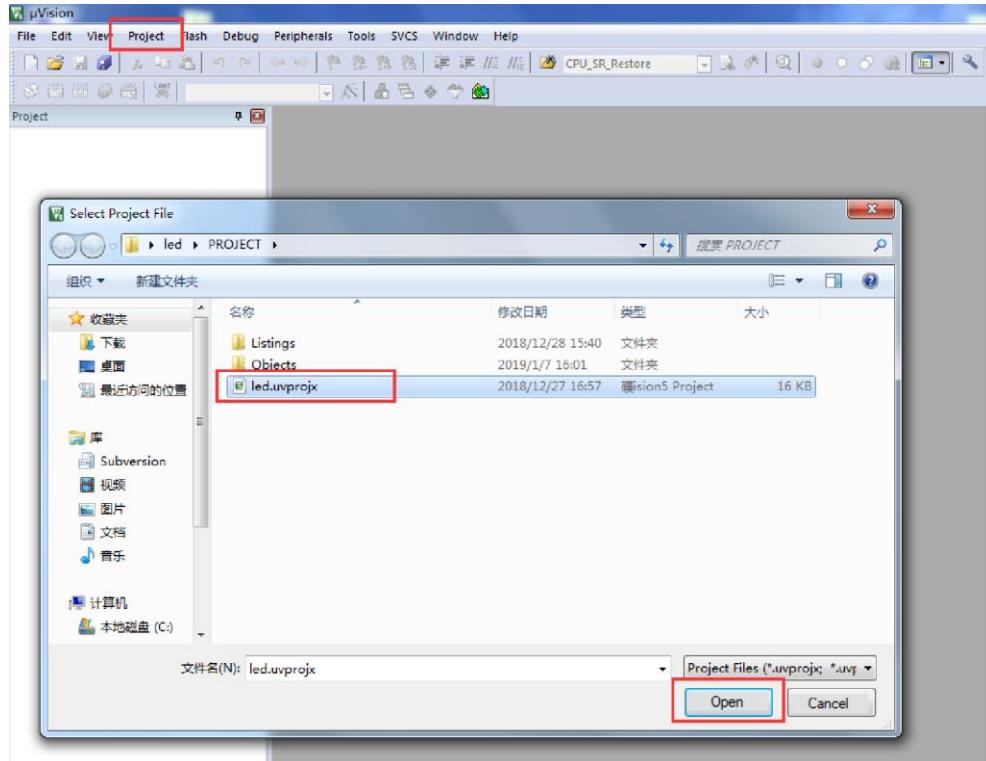
2.1 Software Environment

- ARM Keil MDK
- GNU MCU Eclipse Tool

2.2 Import Software Reference Design

Double click ARM KEIL MDK Tool and select "Project > Open Project..." to import the reference design of led, as shown in Figure 2-1.

Figure 2-1 Import the Reference Design of Led



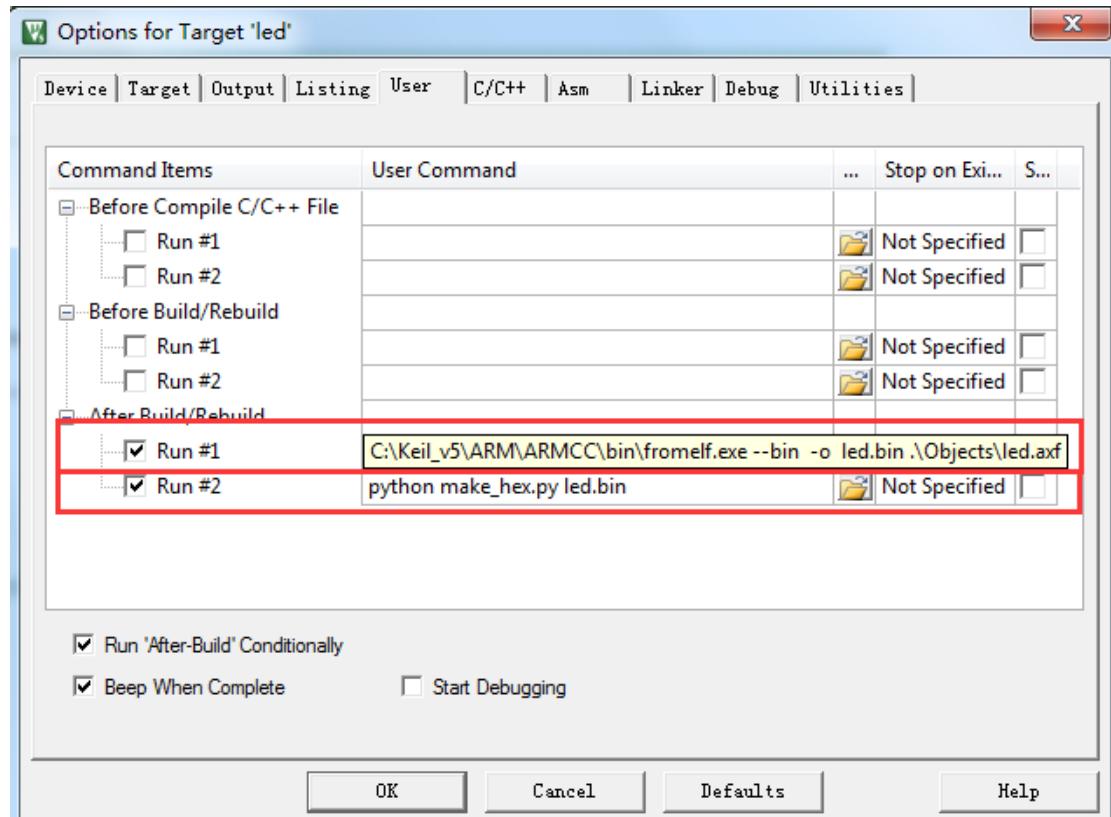
2.3 Modify Configuration Option

If the BIN file is used as the ITCM initialization value, you need to modify the external script tool location of Run #1 and Run #2 according to your local software packet location, such as fromelf.exe and make_hex.py,

as shown in Figure 2-2.

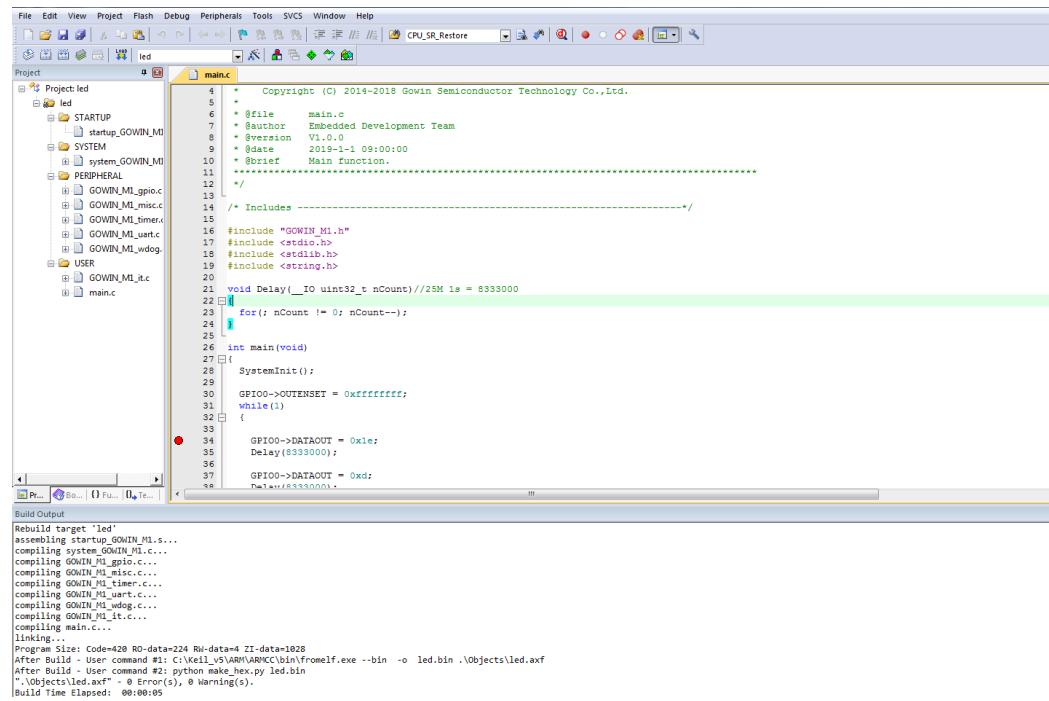
- Run #1
 - fromelf.exe –bin –o bin-file axf-file
- Run #2
 - python make_hex.py bin-file

Figure 2-2 Modify the Script Tool Location



2.4 Compile

Click the compile button on the tool bar to compile the reference design and generate BIN format file and four hex format file of itcm0, itcm1, itcm2, and itcm3, as shown in Figure 2-3.

Figure 2-3 Compiling

2.5 Reference Manual

For Gowin_EMPU_M1 Software Design method, please refer to the following two manuals:

- IPUG533, [Gowin EMPU M1 Software Programming Reference Manual](#)
- IPUG536, [Gowin EMPU M1 IDE Software Reference Manual](#)

3 Gowin_EMPU_M1 Hardware Design

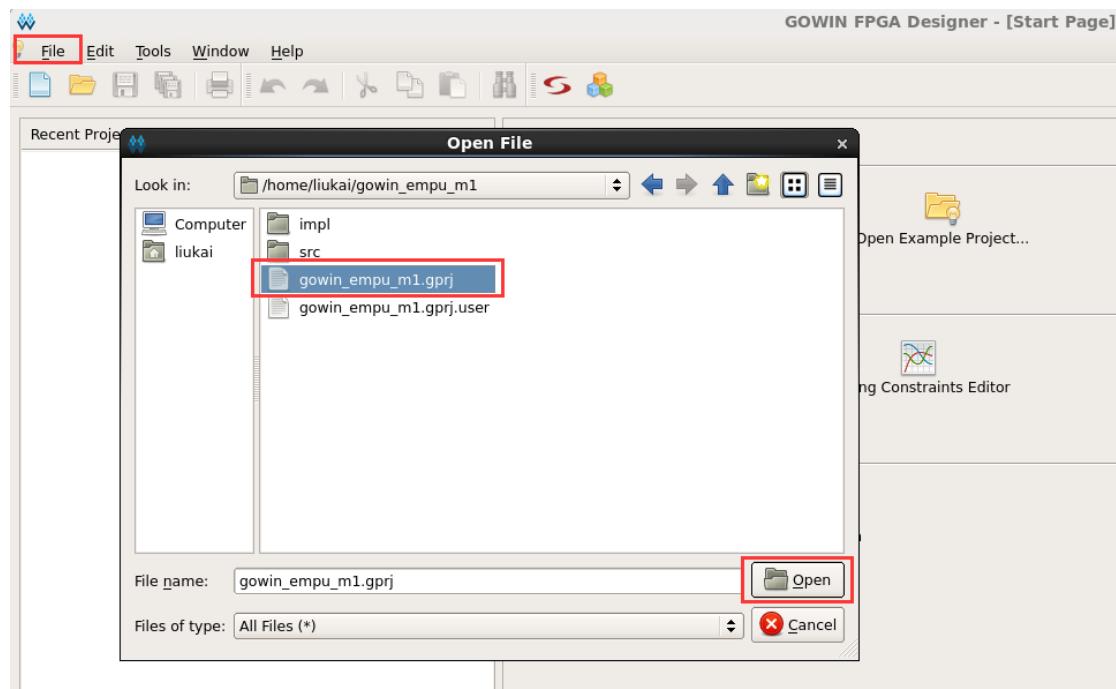
3.1 Hardware Environment

- DK-START-GW2A18 V2.0: GW2A-LV18PG256C8/I7
- EVAL-MIPI-GW1N9 V1.1: GW1N-LV9PG256C6/I5
- EVAL-MIPI-GW1N9 V2.1: GW1N-LV9CM64C6/I5
- GW2A-55K Eval Board Mini: GW2A-LV55PG484C8/I7
- GOWIN FPGA Designer version 1.9.x Beta

3.2 Import Hardware Reference Design

Double click "GOWIN FPGA Designer", select "File > Open", and select Gowin_EMPU_M1 hardware reference design (gowin_empu_m1), as shown in Figure 3-1.

Figure 3-1 Import Gowin_EMPU_M1 Hardware Reference Design



The main project files of the hardware reference design are as shown

in Table 3-1.

Table 3-1 Hardware Reference Design Examples

File	Description
CortexM1DbgIntegration.v	Cortex-M1 soft core with debugging function
CortexM1DbgIntegrationWrapper.v	Top module of Cortex-M1 soft core
cm1_option_defs.v	Parameter configuration of Cortex-M1 soft core
GowinCM1AhbExt.v	AHB-Lite extension bus and peripheral soft core
GowinCM1AhbExtWrapper.v	AHB-Lite extension bus and top module of peripheral soft core
ahb_option_defs.v	AHB-Lite extension bus and parameter configuration of peripheral soft core
gowin_empu_m1.v	Reference design of Cortex-M1 and AHB-Lite instantiation
gowin_empu_m1.cst	Physical Constraints File

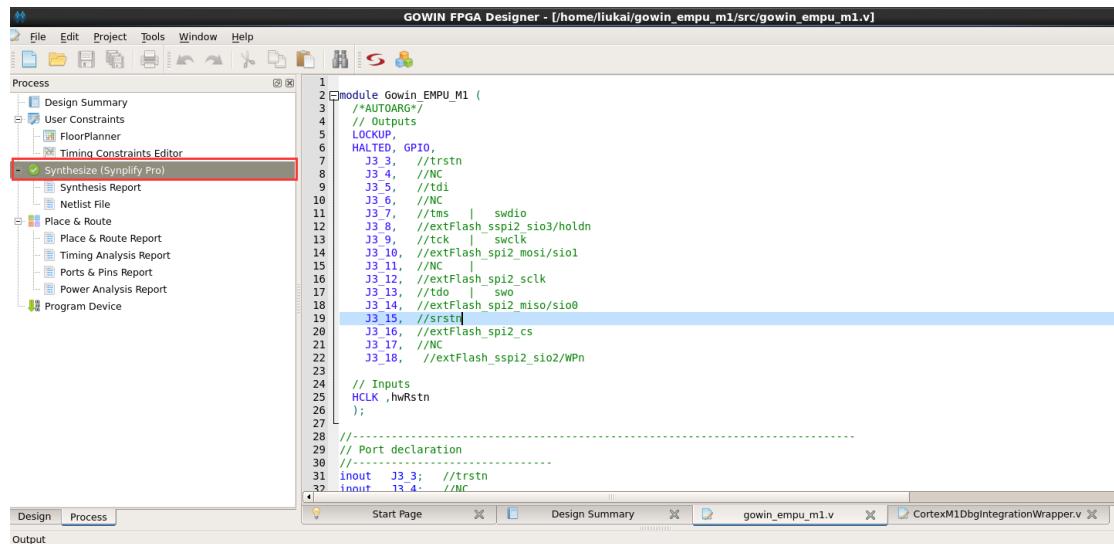
3.3 Modify Configuration Option

Modify the parameters in the file of cm1_option_defs.v.
CM1_ITCM_INIT_PATH is the path of users' local files of itcm0, itcm1, itcm2, and itcm3.

3.4 Synthesize

Run the "Synplify_Pro" synthesis tool to generate the netlist file, as shown in Figure 3-2.

Figure 3-2 Reference Design Synthesis



```

1  module Gowin_EMPU_M1 (
2    /*AUTOARG*/
3    // Outputs
4    // LOCKUP
5    HALTED, GPIO,
6    J3_3, //trstn
7    J3_4, //NC
8    J3_5, //tdi
9    J3_6, //NC
10   J3_7, //tms | swdio
11   J3_8, //extFlash_sspi2_sio3/holdn
12   J3_9, //tck | swclk
13   J3_10, //extFlash_spi2_mosi/siol
14   J3_11, //NC
15   J3_12, //extFlash_spi2_sclk
16   J3_13, //tdo | swo
17   J3_14, //extFlash_spi2_miso/sio0
18   J3_15, //srstn
19   J3_16, //extFlash_spi2_cs
20   J3_17, //NC
21   J3_18, //extFlash_sspi2_sio2/WPn
22
23   // Inputs
24   HCLK ,hwRstn
25   );
26
27
28 //-----
29 // Port declaration
30 //-----
31   inout J3_3; //trstn
32   inout J3_4; //NC

```

Output:

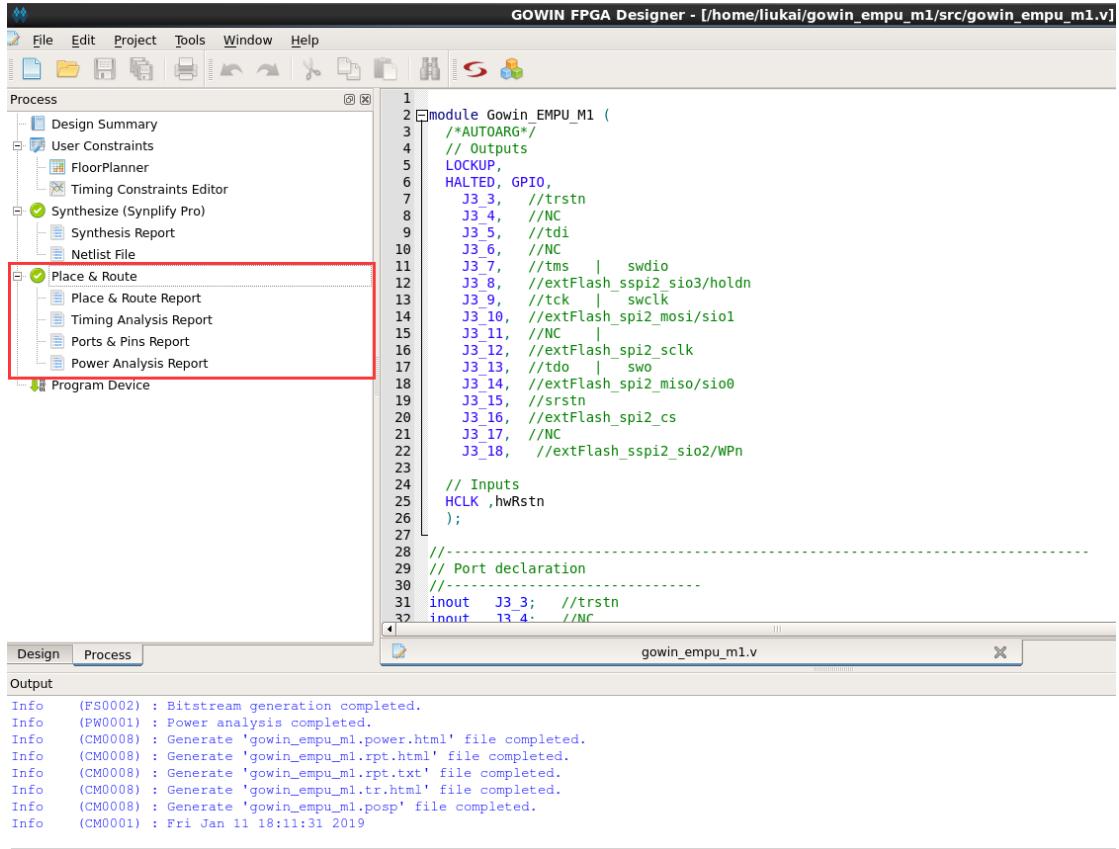
```

ON: FX164 [The option to pack registers in the IOB has not been specified. Please set syn_useioff attribute.
ON: BWL03 [The default time unit for the Synopsys Constraint File (SDC or FDC) is lns.
ON: BWL07 [Synopsys Constraint File capacitance units using default value of 1pF
ON: MT246 :" /home/liukai/gowin_empu_m1/src/cm1_multiplier.v":74:30:74:57]
Blackbox MULT36X36 is missing a user supplied timing model. This may have a negative effect on timing analysis and optimizations (Quality of Results)
ON: MT420 [Found inferred clock Gowin_EMPU_M1/HCLK with period 9.95ns. Please declare a user-defined clock on port HCLK.
ON: MT420 [Found inferred clock Gowin_EMPU_M1/J3_9 with period 5.87ns. Please declare a user-defined clock on port J3_9.
ON: MT320 [This timing report is an estimate of place and route data. For final timing results, use the FPGA vendor place and route report.
ON: MT322 [Clock constraints include only register-to-register paths associated with each individual clock.

```

3.5 Place & Route

After synthesis, run the place&route tool to generate the bitstream files containing software design output and hardware design output, as shown in Figure 3-3.

Figure 3-3 Place & Route

3.6 Reference Manual

Please refer to the following manuals for Gowin_EMPU_M1 hardware design:

- IPU531, [Gowin_EMPU_M1 Hardware Design Reference Manual](#)
- SUG100, [Gowin YunYuan Software User Guide](#)
- SUG101, [Gowin Design Constraints Guide](#)

4 Download

Use Gowin Programmer to download the hardware design and software design bitstream files.

For the further details about Gowin Programmer usage, please refer to SUG502, [Gowin Programmer User Guide](#).

5 Debug

5.1 Gowin_EMPU_M1 Hardware Debugging Method

Use Gowin Analyzer Oscilloscope (GAO) to debug the Gowin_EMPU_M1 FPGA hardware design.

For the further details, please refer to SUG114, [Gowin Analyzer Oscilloscope User Guide](#).

5.2 Gowin_EMPU_M1 Software Debugging Method

Two Gowin_EMPU_M1 software debugging methods are supported:

- Emulator Debugging
- Serial Debugging

5.2.1 Emulator Debugging

Emulator Type

Gowin_EMPU_M1 supports the following emulator to set break points for single-step debugging:

- JLINK emulator
- ULINK emulator

Debug interface

Gowin_EMPU_M1 supports the following debugging interfaces:

- JTAG
- Serial Wire

For the Gowin_EMPU_M1 software debugging method, please refer to IPUG536, [Gowin_EMPU_M1 IDE Software Reference Manual](#).

5.2.2 Serial Debugging

Use serial and serial debugging assistant to track the running status.

For the Gowin_EMPU_M1 serial debugging method, please refer to IPUG535, [Gowin_EMPU_M1 Serial Port Debugging Reference Manual](#).

