Gowin APB SD Host IP

User Guide

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Revision History

Date	Version	Description
2026/02/13	1.0E	Initial version published.
2026/11/13	1.0.1E	● Updated the software programming library. ● Updated the hardware and software programming reference designs.

Contents

Contents i
List of Figures iii
List of Tables iv
1 About This Guide 1
1.1 Purpose 1
1.2 Related Documents 1
1.3 Terminology and Abbreviations 2
1.4 Support and Feedback 2
2 Overview 3
2.1 Introduction 3
2.2 Features 3
2.3 Structure Diagram 4
2.4 Functional Description 4
2.4.1 Clock Generation 4
2.4.2 Interrupt Generation 5
2.5 Resource Utilization 6
3 Signal Description 7
4 Interface Configuration 8
5 Programming Model 9
5.1 Register 9
5.1.1 Register Overview 9
5.1.2 Command Argument Register (0x00) 10
5.1.3 Command Register (0x4) 10
5.1.4 Response 0-3 Registers (0x08–0x14) 11
5.1.5 Data Transfer Timeout Register (0x18) 11
5.1.6 Control Register (0x1C) 11
5.1.7 Command Transfer Timeout Register (0x20) 12
5.1.8 Clock Divider Register (0x24) 12
5.1.9 Software Reset Register (0x28) 12
5.1.10 Command Transaction Event Status Register (0x34) 13
5.1.11 Command Transaction Event Enable Register (0x38) 13
5.1.12 Data Transaction Event Status Register (0x3C) 13
5.1.13 Data Transaction Event Enable Register (0x40) 14
5.1.14 Transfer Block Size Register (0x44) 14
5.1.15 Transfer Block Count Register (0x48) 15

5.1.16 Transmit Data Register (0x4C) 15
5.1.17 Receive Data Register (0x50) 15
5.1.18 FIFO Status Register (0x54) 15
5.2 Driver Function 16
5.2.1 Driver Function Overview 16
5.2.2 apb_sd_host_reset 16
5.2.3 apb_sd_host_clock_config 17
5.2.4 apb_sd_host_bus_width_config 17
5.2.5 apb_sd_host_command_config 18
5.2.6 apb_sd_host_response_get 18
5.2.7 apb_sd_host_data_config 19
5.2.8 apb_sd_host_data_write 19
5.2.9 apb_sd_host_data_read 19
5.2.10 apb_sd_host_interrupt_enable 20
5.2.11 apb_sd_host_interrupt_status_get 20
5.2.12 apb_sd_host_interrupt_status_clear 20
5.2.13 apb_sd_host_fifo_status_get 21
6 TF Card Brands and Types 22
7 Reference Design 23

List of Figures

Figure 2-1 Structure Diagram 4
Figure 2-2 Interrupt Generation Scheme 5
Figure 4-1 Interface Configuration 8

List of Tables

Table 1-1 Terminology and Abbreviations 2
Table 2-1 Gowin APB SD Host IP Overview 3
Table 2-2 Resource Utilization 6
Table 3-1 Signal Description 7
Table 5-1 Register Definition 9
Table 5-2 Command Argument Register 10
Table 5-3 Command Register 10
Table 5-4 Response Register 11
Table 5-5Data Transfer Timeout Register 11
Table 5-6 Status Register 11
Table 5-7 Command Timeout Register 12
Table 5-8 Clock Divider Register 12
Table 5-9 Software Reset Register 12
Table 5-10 Command Transaction Event Status Register 13
Table 5-11 Command Transaction Event Enable Register 13
Table 5-12 Data Transaction Event Status Register 13
Table 5-13 Data Transaction Event Enable Register 14
Table 5-14 Transfer Block Size Register 14
Table 5-15 Transfer Block Count Register 15
Table 5-16 Transmit Data Register 15
Table 5-17 Receive Data Register 15
Table 5-18 FIFO Status Register 15
Table 5-19 Driver Function Definition 16
Table 5-20 apb_sd_host_reset Function Definition 16
Table 5-21 apb_sd_host_clock_config Function Definition 17
Table 5-22 apb_sd_host_bus_width_config Function Definition 17
Table 5-23 apb_sd_host_command_config Function Definition 18
Table 5-24 apb_sd_host_response_get Function Definition 18
Table 5-25 apb_sd_host_data_config Function Definition 19
Table 5-26 apb_sd_host_data_write Function Definition 19
Table 5-27 apb_sd_host_data_read Function Definition 19
Table 5-28 apb_sd_host_interrupt_enable Function Definition 20

Table 5-29 apb_sd_host_interrupt_status_get Function Definition 20
Table 5-30 apb_sd_host_interrupt_status_clear Function Definition 20
Table 5-31 apb_sd_host_fifo_status_get Function Definition 21

1 About This Guide

1.1 Purpose

The purpose of the Gowin APB SD Host IP User Guide is to help you understand the features and operation of the Gowin APB SD Host IP by describing its functions, structures, signals, parameters, interface configuration, programming model, and reference design. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.12.04 (64-bit). As the software is subject to change without notice, some information may become outdated and should be interpreted according to the software version in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can download and view the following documents at www.gowinsemi.com:

- DS961, GW2ANR series of FPGA Products Data Sheet
- DS102, GW2A series of FPGA Products Data Sheet
- DS226, GW2AR series of FPGA Products Data Sheet
- DS971, GW2AN-18X & 9X Data Sheet
- DS976, GW2AN-55 Data Sheet
- DS981, GW5AT series of FPGA Products Data Sheet
- DS1103, GW5A series of FPGA Products Data Sheet
- DS1239, GW5AST series of FPGA Products Data Sheet
- DS1105, GW5AS series of FPGA Products Data Sheet
- DS1108, GW5AR series of FPGA Products Data Sheet
- DS1118, GW5ART series of FPGA Products Data Sheet
- SUG100, Gowin Software User Guide
- SUG549, GMD(GOWIN MCU Designer) User Guide

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
FIFO	First Input First Output
FPGA	Field Programmable Gate Array
IP	Intellectual Property
MCU	Microcontroller Unit
MMC	Multimedia Card
SDC	Secure Digital Card

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Introduction

Gowin APB SD Host IP is an SD/MMC communication controller designed for system-on-chip (SoC), that provides a simple interface for any MCU with an APB bus. The communication between the SD/MMC controller and the SD/MMC card complies with the SD/MMC protocol.

Table 2-1 Gowin APB SD Host IP Overview

Gowin APB SD Host IP	
Logic Resource	See Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.11.02 and above)

Note!

For a list of the supported devices, click here.

2.2 Features

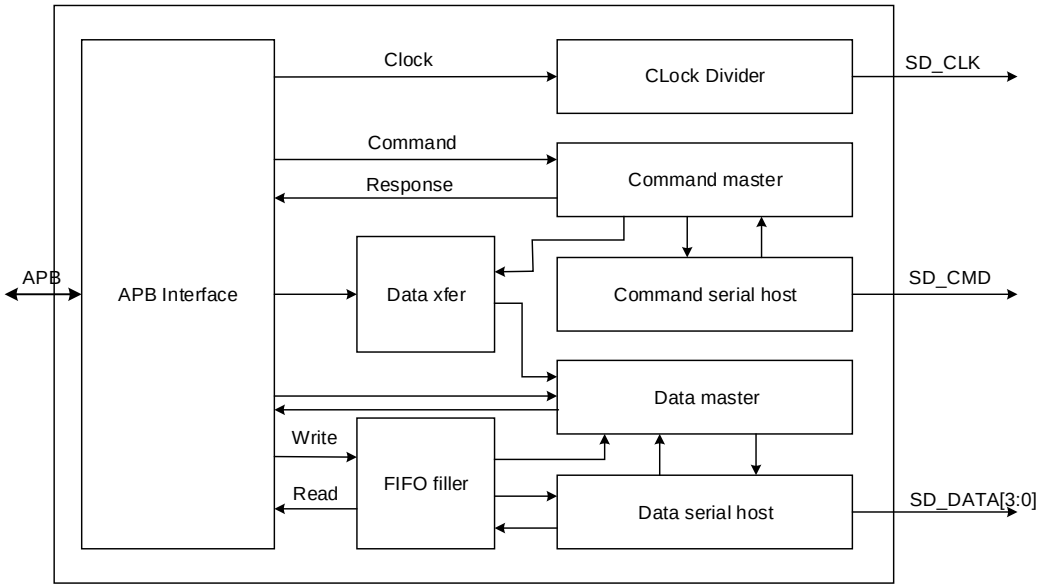
Gowin APB SD Host IP mainly includes the following features:

- Supports 1-bit or 4-bit SD/MMC modes
- Supports 32-bit APB interface
- Interrupt generation upon completion of data or command transactions
- Configurable FIFO depth for read/write operations
- Supports arbitrary command codes (including multi-block data transfers)
- Supports R1, R1b, R2 (136-bit), R3, R6, and R7 response types

2.3 Structure Diagram

The structure diagram of Gowin APB SD Host IP is shown in Figure 2-1.

Figure 2-1 Structure Diagram



2.4 Functional Description

The APB bus interface provides a channel for the CPU to access all registers of the Gowin APB SD Host controller IP and must be connected to the CPU data master. The interrupt signal offers a mechanism to notify the CPU when data and command transfers are completed (interrupts are optional and not mandatory). The SD/MMC card interface is used for communication with an external SD/MMC card and must be connected to the FPGA external pins that are linked to the SD/MMC card connector. Since these external pins are bidirectional, the Gowin APB SD Host IP controller provides input, output, and output-enable signals for these pins.

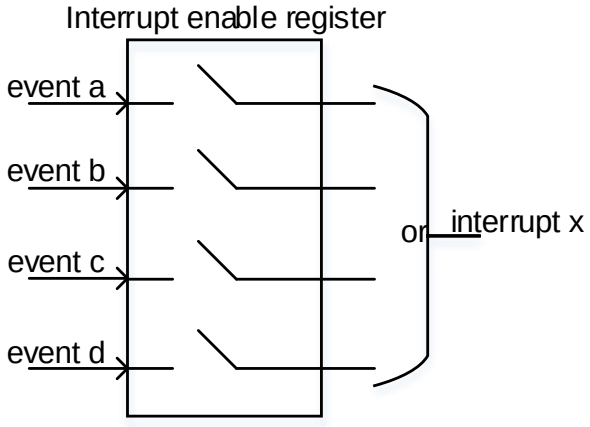
2.4.1 Clock Generation

Gowin APB SD Host IP requires two clock sources. The first clock (pclk) is used for APB bus operation, wtih no special constraints. The second clock (sd_clk_i_pad) is used for SD/MMC interface operations. 刷 sd_clk_i_pad is used to drive the external SD/MMC card clock output (sd_clk_o_pad) generated by the internal clock divider. This clock divider can divide the clock frequency of sd_clk_i_pad by 2, 4, 6, 8…, etc. (i.e. 2*(n+1), where n is in the range of 0 to 255). The clock frequency of sd_clk_o_pad is dependent on the SD/MMC specification, and in order to fully utilize the transmission bandwidth, sd_clk_o_pad should be able to reach a frequency of 25MHz, which requires a minimum frequency of 50MHz for sd_clk_i_pad. The two clock inputs, pclk and sd_clk_i_pad, can use the same clock signal.

2.4.2 Interrupt Generation

Interrupts are important when polling technology is not feasible. Gowin APB SD Host IP has two interrupt sources: One to notify a command of the end of a transaction (int_cmd signal) and one to notify the end of a data transaction (int_data signal). Both interrupts are active high. All interrupt-triggering events can be disabled through mask settings and therefore do not participate in interrupt generation in this case, as shown in Figure 2-2.

Figure 2-2 Interrupt Generation Scheme



2.4.2.1 Command Transaction Event

The command transaction completion interrupt is triggered by the following command transaction events:

- Completion: The transaction completes successfully.
- Error: The transaction ends in an error state (one or more of the following events occur).
- Timeout: A timeout error occurs (the SD card fails to respond in time).
- CRC Error: CRC check error (the CRC calculated from the received response data does not match the CRC field in the response).
- Index Error: Index check error (the response contains an incorrect index field value).

2.4.2.2 Data Transaction Event

The data transaction completion interrupt is triggered by the following data transaction events:

- Completion: The transaction completes successfully.
- CRC error: CRC check error.
  - In write transactions, the CRC received in the response does not match the CRC calculated by the Gowin APB SD Host.
  - In read transactions, the CRC calculated from the received data does not match the CRC field in the data.
- FIFO Error: Internal FIFO error

- In write transactions, the transmit FIFO becomes empty before all data has been sent.
- In read transactions, the receive FIFO becomes full.
- Both conditions may be caused by an APB bus speed that is too low or by the APB bus remaining busy for an extended period of time.

2.5 Resource Utilization

The Gowin APB SD Host IP is implemented in Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW5A series of FPGA as an instance, the resource utilization of the Gowin APB SD Host IP is shown in Table 2-2.

Table 2-2 Resource Utilization

Device	Resource	Resource Utilization	Configuration
GW5A	Logic	2574	FIFO Depth: 4
	Register	2758	
	BSRAM	0	

3 Signal Description

The port descriptions of Gowin APB SD IP are shown in Table 3-1.

Table 3-1 Signal Description

Signal Name	I/O	Width	Description
paddr	input	[7:0]	APB address bus
pclk	input	1	APB clock, used to time all the bus transfers
penable	input	1	APB enable signal
presetn	input	1	APB reset signal (Active-Low)
psel	input	1	APB select signal When set to 1, this signal indicates that the slave device has been selected by the APB bridge and that a data transfer is required.
pwdata	input	[31:0]	APB write data bus
pwrite	input	1	APB transfer direction signal This signal indicates a write access when high and a read access when low.
pstrb	input	[3:0]	APB write strobe signal This signal indicates which byte lanes to update during a write transfer. There is one write strobe for each 8 bits of the write data bus.
prdata	output	[31:0]	APB read data bus
pready	output	1	APB ready signal
pslverr	output	1	APB slave error signal
sd_cmd_dat_i	input	1	Command line input
sd_cmd_out_o	output	1	Command line output
sd_cmd_oe_o	output	1	Command line output enable
sd_dat_dat_i	input	[3:0]	Data line inputs
sd_dat_out_o	output	[3:0]	Data line outputs
sd_dat_oe_o	output	1	Data line outputs enable
sd_clk_o_pad	output	1	Clock for external SD/MMC card
sd_clk_i_pad	input	1	Clock for SD/MMC interface
int_cmd	output	1	Command transaction finished interrupt
int_data	output	1	Data transaction finished interrupt

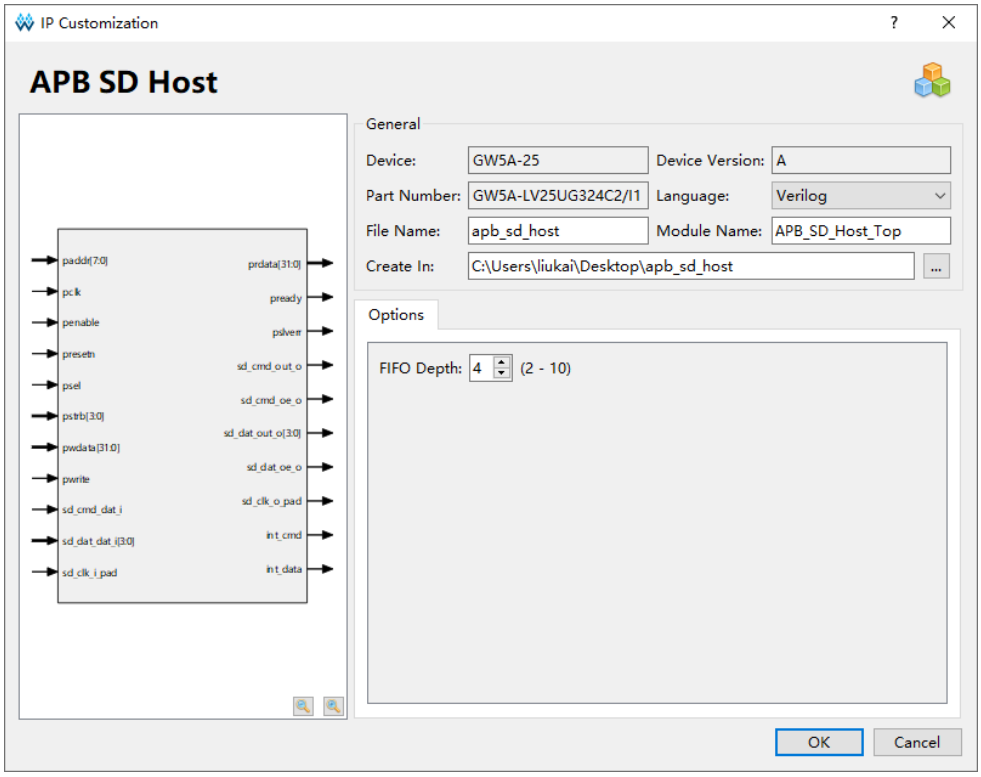
4 Interface Configuration

You can select IP Core Generator Tool in Gowin Software to call and configure Gowin APB SD Host IP.

Select "Tool > IP Core Generator" on the menu bar or click the "" on the tool bar to open IP Core Generator; then select "Soft IP Core > Microprocessor System > Peripheral > AHB SD Host 1.0".

The Gowin APB SD Host IP interface configuration is shown in Figure 4-1.

Figure 4-1 Interface Configuration



The Gowin APB SD Host IP option configuration is described as follows:

FIFO Depth: The FIFO address depth of the Gowin APB SD Host ranges from 2 to 10, with a default value of 4.

5 Programming Model

5.1 Register

5.1.1 Register Overview

The definition of Gowin APB SD Host IP register is shown in Table 5-1. The Gowin APB SD Host IP register definition is located in …\library\lib\apb_sd_host.h.

Table 5-1 Register Definition

Address Offset	Name	Description
0x00	argument	Command argument register
0x04	command	Command register
0x08	response0	Bits [31:0] of the response register
0x0C	response1	Bits [63:32] of the response register
0x10	response2	Bits [95:64] of the response register
0x14	response3	Bits [127:96] of the response register
0x18	data_timeout	Data transfer timeout register
0x1C	control	Control register
0x20	cmd_timeout	Command transfer timeout register
0x24	clock_divider	Clock divider register
0x28	reset	Software reset register
0x2C-0x30	reserved0[2]	Reserved
0x34	cmd_event_status	Command transaction event status register
0x38	cmd_event_enable	Command transaction event enable register
0x3C	data_event_status	Data transaction event status register
0x40	data_event_enable	Data transaction event enable register
0x44	blkock_size	Data block size register
0x48	blkock_count	Data block count register
0x4C	tx_data	Transmit data register
0x50	rx_data	Receive Data Register
0x54	fifo_status	FIFO status register

Address Offset	Name	Description
0x58-0x5C	reserved1[3]	Reserved

The following sections provide a detailed description of the Gowin APB SD Host IP register definitions.

The abbreviations for register types are summarized as follows:

- RO: Read-only
- WO: Write-only
- R/W: Readable and writable

5.1.2 Command Argument Register (0x00)

The command argument register initiates a command transaction when written. Before writing to this register, the command register must be configured first.

The definition of the command argument register is shown in Table 5-2.

Table 5-2 Command Argument Register

Name	Bit	Type	Description	Reset
CmdArg	31:0	R/W	Command argument value	0x0

5.1.3 Command Register (0x4)

The command register is used to configure all information related to the command to be sent.

The definition of the command register is shown in Table 5-3.

Table 5-3 Command Register

Name	Bit	Type	Description	Reset
-	31:14	-	Reserved	-
CmdIdx	13:8	R/W	Command index	0x0
-	7	-	Reserved	-
DataTrans	6:5	R/W	Data transfer specification 0x0: no data transfer 0x1: triggers read data transaction after command transaction 0x2: triggers write data transaction after command transaction	0x0
ChkCmdIdx	4	R/W	Check response for correct command index	0x0
ChkCRC	3	R/W	Check response CRC	0x0
ChkBusySig	2	R/W	Check for busy signal after command transaction (if busy signal will be asserted after command transaction, core will wait for as long as busy signal remains)	0x0
RespChkCfg	1:0	R/W	Response check configuration. 0x0: don’t wait for response	0x0

Name	Bit	Type	Description	Reset
			0x1: wait for short response (48-bits) 0x2: wait for long response (136-bits)	

5.1.4 Response 0-3 Registers (0x08–0x14)

The Response 0-3 registers contain the response data bits after a command transaction is successfully completed (if bits [1:0] of the command register are configured to wait for a response).

The definition of the response register is shown in Table 5-4.

Table 5-4 Response Register

Name	Bit	Type	Description	Reset
RespDataBit	31:0	RO	Response data bits	0x0

5.1.5 Data Transfer Timeout Register (0x18)

The data timeout register is used to configure the watchdog counter for data transactions. If any data transaction lasts longer than the configured timeout period, an interrupt will be generated. The value in the timeout register represents the number of sd_clk_o_pad clock cycles. The register value is calculated using the following formula:

$$REG = \frac{timeout[s] * frequency_{sd_clk_i_pad}[Hz]}{2 * \ (clock_divider \ + \ 1)}$$

The definition of the data transfer timeout register is shown in Table 5-5.

Table 5-5Data Transfer Timeout Register

Name	Bit	Type	Description	Reset
-	31:24	-	Reserved	-
TimeoutVal	23:0	R/W	Timeout value (when it is 0, timeout is disabled)	0x0

5.1.6 Control Register (0x1C)

The definition of the control register is shown in Table 5-6.

Table 5-6 Status Register

Name	Bit	Type	Description	Reset
-	31:1	-	Reserved	-
BusWidth	0	R/W	SD/MMC bus width 0x0: 1-bit operation 0x1: 4-bit operation	0x0

5.1.7 Command Transfer Timeout Register (0x20)

The command timeout register is used to configure the watchdog counter for command transactions. If any command transaction lasts longer than the configured timeout period, an interrupt will be generated. The value in the timeout register represents the number of sd_clk_o_pad clock cycles. The register value is calculated using the following formula:

$$REG = \frac{timeout[s] * frequency_{sd_clk_i_pad}[Hz]}{2 * \ (clock_divider \ + \ 1)}$$

The definition of the command timeout register is shown in Table 5-7.

Table 5-7 Command Timeout Register

Name	Bit	Type	Description	Reset
-	31:24	-	Reserved	-
TimeoutVal	23:0	R/W	Timeout value (when it is 0, timeout is disabled)	0x0

5.1.8 Clock Divider Register (0x24)

The clock divider register is used to control the divided frequency of the sd_clk_i_pad signal. The output of this divider is routed to the SD/MMC interface clock domain. The register value is calculated using the following formula:

$$REG = \frac{frequency_{\text{sd_clk_i_pad}}[Hz]}{2 * frequency_{\text{sd_clk_o_pad}}[Hz]} - 1$$

The definition of the clock divider register is shown in Table 5-8.

Table 5-8 Clock Divider Register

Name	Bit	Type	Description	Reset
-	31:8	-	Reserved	-
DivRatio	7:0	R/W	Divider ratio	0x07

5.1.9 Software Reset Register (0x28)

When the software reset register is set to 1, the Gowin APB SD Host controller will be reset. Clearing the register cancels the reset.

The definition of the software reset register is shown in Table 5-9.

Table 5-9 Software Reset Register

Name	Bit	Type	Description	Reset
-	31:1	-	Reserved	-
Rst	0	R/W	Reset 0x0: not reset 0x1: reset applied	0x0

5.1.10 Command Transaction Event Status Register (0x34)

The command transaction event status register is used to store all pending event flags related to command transactions. Writing to this register clears all the flags.

The definition of the command transaction event status register is shown in Table 5-10.

Table 5-10 Command Transaction Event Status Register

Name	Bit	Type	Description	Reset
-	31:5	-	Reserved	-
IdxErr	4	R/W	Index error event	0x0
CrcErr	3	R/W	CRC error event	0x0
TimeoutErr	2	R/W	Timeout error event	0x0
AllErr	1	R/W	Error event (logic sum of all error events)	0x0
CmdCmpl	0	R/W	Command transaction successful completion event	0x0

5.1.11 Command Transaction Event Enable Register (0x38)

The command transaction event enable register functions as an event mask. To enable a specific event, set the corresponding bit to 1.

The definition of the command transaction event enable register is shown in Table 5-11.

Table 5-11 Command Transaction Event Enable Register

Name	Bit	Type	Description	Reset
-	31:5	-	Reserved	-
EnIdxErr	4	R/W	Enable index error event	0x0
EnCrcErr	3	R/W	Enable CRC error event	0x0
EnTimeoutErr	2	R/W	Enable timeout error event	0x0
EnAllErr	1	R/W	Enable error event	0x0
EnCmdCmpl	0	R/W	Enable command transaction successful completion event	0x0

5.1.12 Data Transaction Event Status Register (0x3C)

The data transaction event status register is used to store all pending event flags related to data transactions. Writing to this register clears all the flags.

The definition of the data transaction event status register is shown in Table 5-12.

Table 5-12 Data Transaction Event Status Register

Name	Bit	Type	Description	Reset
-	31:6	-	Reserved	-
FIFORdFulErr	5	R/W	FIFO read full error event	0x0
FIFOWrEmpErr	4	R/W	FIFO write full empty event	0x0

Name	Bit	Type	Description	Reset
CrcErr	3	R/W	CRC error event	0x0
TimeoutErr	2	R/W	Timeout error event	0x0
AllErr	1	R/W	Error event (logic sum of all error events)	0x0
DataCmpl	0	R/W	Data transaction successful completion event	0x0

5.1.13 Data Transaction Event Enable Register (0x40)

The data transaction event enable register functions as an event mask. To enable a specific event, set the corresponding bit to 1.

The definition of the data transaction event enable register is shown in Table 5-13.

Table 5-13 Data Transaction Event Enable Register

Name	Bit	Type	Description	Reset
-	31:6	-	Reserved	-
EnFIFORdFulErr	5	R/W	Enable FIFO read full error event	0x0
EnFIFOWrEmpErr	4	R/W	Enable FIFO write empty error event	0x0
EnCrcErr	3	R/W	Enable CRC error event	0x0
EnTimeoutErr	2	R/W	Enable timeout error event	0x0
EnAllErr	1	R/W	Enable error event	0x0
EnDataCmpl	0	R/W	Enable data transaction successful completion event	0x0

5.1.14 Transfer Block Size Register (0x44)

The transfer block size register controls the number of bytes to be written or read in a single block. For a data transaction, the total number of bytes transferred equals the block size multiplied by the block count. The register value is calculated using the following formula:

$$REG = size_of_block - 1$$

The definition of the transfer block size register is shown in Table 5-14.

Table 5-14 Transfer Block Size Register

Name	Bit	Type	Description	Reset
-	31:12	-	Reserved	-
ByteNum	11:0	R/W	Number of bytes in a single block minus 1	0x1FF

5.1.15 Transfer Block Count Register (0x48)

The transfer block count register controls the number of bytes to be written or read in a data transaction. For a data transaction, the total number of bytes transferred equals the block count multiplied by the block size. The register value is calculated using the following formula:

$$REG = number_of_blocks - 1$$

The definition of the transfer block count register is shown in Table 5-15.

Table 5-15 Transfer Block Count Register

Name	Bit	Type	Description	Reset
-	31:16	-	Reserved	-
BlkNum	15:0	R/W	Number of blocks in data transaction minus - 1	0x0

5.1.16 Transmit Data Register (0x4C)

The definition of the transmit data register is shown in Table 5-16.

Table 5-16 Transmit Data Register

Name	Bit	Type	Description	Reset
WrData	31:0	WO	Write data	0x0

5.1.17 Receive Data Register (0x50)

The definition of the receive data register is shown in Table 5-17.

Table 5-17 Receive Data Register

Name	Bit	Type	Description	Reset
RdData	31:0	RO	Read data	0x0

5.1.18 FIFO Status Register (0x54)

The FIFO status register contains the empty/full status of the read/write FIFO.

The definition of the FIFO status register is shown in Table 5-18.

Table 5-18 FIFO Status Register

Name	Bit	Type	Description	Reset
-	31:4	-	Reserved	-
WrFIFOEmp	3	RO	FIFO write empty 0x0: not empty 0x1: empty	0x1
WrFIFOFul	2	RO	FIFO write full 0x0: not full 0x1: full	0x0
RdFIFOEmp	1	RO	FIFO read empty 0x0: not empty 0x1: empty	0x1
RdFIFOFul	0	RO	FIFO read full	0x0

Name	Bit	Type	Description	Reset
			0x0: not full 0x1: full	

5.2 Driver Function

5.2.1 Driver Function Overview

The definition of Gowin APB SD Host driver function is shown in Table 5-19. The definition for Gowin APB SD Host driver function is located in …\library\lib\apb_sd_host.h and apb_sd_host.c.

Table 5-19 Driver Function Definition

Driver Function	Description
apb_sd_host_reset	Performs the SD Host software reset
apb_sd_host_clock_config	Configures the SD Host clock division
apb_sd_host_bus_width_config	Configures the SD Host bus width
apb_sd_host_command_config	Configures the SD Host command attributes
apb_sd_host_response_get	Retrieves the SD Host response
apb_sd_host_data_config	Configures the SD Host data attributes
apb_sd_host_data_write	Transmits data via the SD Host interface
apb_sd_host_data_read	Receives data via the SD Host interface
apb_sd_host_interrupt_enable	Enables the SD Host interrupts
apb_sd_host_interrupt_status_get	Retrieves the SD Host interrupt status
apb_sd_host_interrupt_status_clear	Clears the SD Host interrupt status
apb_sd_host_fifo_status_get	Retrieves the SD Host FIFO status

The following sections provide a detailed description of the Gowin APB SD Host driver function definitions.

5.2.2 apb_sd_host_reset

The definition of the apb_sd_host_reset function is shown in Table 5-20.

Table 5-20 apb_sd_host_reset Function Definition

Prototype	void apb_sd_host_reset (APB_SD_Host_RegDef* sd_host, sd_reset_type reset_state)
Description	Performs the SD Host software reset
Parameter	● sd_host: The pointer to APB_SD_Host_RegDef structure ● reset_state: Resets the state – SD_NORESET: No reset – SD_RESET: Reset
Return Value	None

5.2.3 apb_sd_host_clock_config

The definition of the apb_sd_host_clock_config function is shown in Table 5-21.

Table 5-21 apb_sd_host_clock_config Function Definition

Prototype	void apb_sd_host_clock_config(APB_SD_Host_RegDef* sd_host, sd_clk_div_type clk_div)
Description	Configures the SD Host clock division
Parameter	● sd_host: The pointer to APB_SD_Host_RegDef structure ● Clk_div: Clock division value – SD_CLK_DIV6: Divide by 6 – SD_CLK_DIV8: Divide by 8 – SD_CLK_DIV10: Divide by 10 – SD_CLK_DIV12: Divide by 12 – SD_CLK_DIV14: Divide by 14 – SD_CLK_DIV16: Divide by 16 – SD_CLK_DIV18: Divide by 18 – SD_CLK_DIV20: Divide by 20 – SD_CLK_DIV22: Divide by 22 – SD_CLK_DIV24: Divide by 24 – SD_CLK_DIV26: Divide by 26 – SD_CLK_DIV28: Divide by 28 – SD_CLK_DIV30: Divide by 30 – SD_CLK_DIV32: Divide by 32 – SD_CLK_DIV34: Divide by 34 – SD_CLK_DIV36: Divide by 36 – SD_CLK_DIV38: Divide by 38 – SD_CLK_DIV40: Divide by 40 – SD_CLK_DIV42: Divide by 42 – SD_CLK_DIV44: Divide by 44 – SD_CLK_DIV46: Divide by 46 – SD_CLK_DIV48: Divide by 48 – SD_CLK_DIV50: Divide by 50
Return Value	None

5.2.4 apb_sd_host_bus_width_config

The definition of the apb_sd_host_bus_width_config function is shown in Table 5-22.

Table 5-22 apb_sd_host_bus_width_config Function Definition

Prototype	void apb_sd_host_bus_width_config(APB_SD_Host_RegDef* sd_host, sd_bus_width_type width)
Description	Configures the SD Host bus width
Parameter	● sd_host: The pointer to APB_SD_Host_RegDef structure ● width: Bus width – SD_BUS_WIDTH_D1: 1 bit – SD_BUS_WIDTH_D4: 4 bits

Return Value	None

5.2.5 apb_sd_host_command_config

The definition of the apb_sd_host_command_config function is shown in Table 5-23.

Table 5-23 apb_sd_host_command_config Function Definition

Prototype	void apb_sd_host_command_config(APB_SD_Host_RegDef* sd_host, sd_command_struct_type *command_struct)
Description	Configures the SD Host command attributes
Parameter	● sd_host: The pointer to APB_SD_Host_RegDef structure ● command_struct: The pointer to sd_command_struct_type structure Structure Member: ● Argument: Configures the SD Host command arguments ● cmd_index: Configures the SD Host command index ● timeout: Configures the SD Host command timeout threshold ● Index: Checks the current SD Host command index – SD_INDEX_NO: Do not check – SD_INDEX_CHECK: Check ● crc: Checks the CRC of the command response – SD_CRC_NO: Do not check – SD_CRC_CHECK: Check ● rsp_type: Configures the response type – SD_RESPONSE_NO: No response required – SD_RESPONSE_SHORT: Wait for a short response – SD_RESPONSE_NO: Wait for a long response ● wait_type: Specifies whether to wait for the busy signal after command transaction – SD_WAIT_FOR_NO: Do not wait – SD_WAIT_FOR_BUSY: Wait ● transfer_direction: Configures data transfer direction – SD_DATA_NONE: No data transfer – SD_DATA_TRANSFER_TO_CONTROLLER: Read data transfer – SD_DATA_TRANSFER_TO_CARD: Write data transfer
Return Value	None

5.2.6 apb_sd_host_response_get

The definition of the apb_sd_host_response_get function is shown in Table 5-24.

Table 5-24 apb_sd_host_response_get Function Definition

Prototype	unsigned int apb_sd_host_response_get(APB_SD_Host_RegDef* sd_host, sd_rsp_index_type reg_index)
Description	Retrieves the SD Host response
Parameter	● sd_host: The pointer to APB_SD_Host_RegDef structure ● reg_index: Responses register index

	– SD_RSP1_INDEX: Responses register 0 – SD_RSP2_INDEX: Responses register 1 – SD_RSP3_INDEX: Responses register 2 – SD_RSP4_INDEX: Responses register 3
Return Value	Returns the value of the specified response register

5.2.7 apb_sd_host_data_config

The definition of the apb_sd_host_data_config function is shown in Table 5-25.

Table 5-25 apb_sd_host_data_config Function Definition

Prototype	void apb_sd_host_data_config(APB_SD_Host_RegDef* sd_host, sd_data_struct_type *data_struct)
Description	Configures the SD Host data attributes
Parameter	● sd_host: The pointer to APB_SD_Host_RegDef structure ● data_struct: Pointer to the sd_data_struct_type structure Structure Member: ● timeout: Configures the SD Host data timeout threshold ● block_size: Configures the transfer block size (in bytes) – SDIO_DATA_BLOCK_SIZE_512B: 512 bytes ● block_cnt: Configures the number of transfer blocks
Return Value	None

5.2.8 apb_sd_host_data_write

The definition of the apb_sd_host_data_write function is shown in Table 5-26.

Table 5-26 apb_sd_host_data_write Function Definition

Prototype	void apb_sd_host_data_write(APB_SD_Host_RegDef* sd_host, unsigned int *w_data)
Description	Transmits data via the SD Host interface
Parameter	● sd_host: The pointer to APB_SD_Host_RegDef structure ● w_data: The pointer to the data to be transmitted
Return Value	None

5.2.9 apb_sd_host_data_read

The definition of the apb_sd_host_data_read function is shown in Table 5-27.

Table 5-27 apb_sd_host_data_read Function Definition

Prototype	void apb_sd_host_data_read(APB_SD_Host_RegDef* sd_host, unsigned int *r_data)
Description	Receives data via the SD Host interface
Parameter	● sd_host: The pointer to APB_SD_Host_RegDef structure ● r_data: The pointer to the data to be received
Return Value	None

5.2.10 apb_sd_host_interrupt_enable

The definition of the apb_sd_host_interrupt_enable function is shown in Table 5-28.

Table 5-28 apb_sd_host_interrupt_enable Function Definition

Prototype	void apb_sd_host_interrupt_enable(APB_SD_Host_RegDef* sd_host, sd_interrupt_type type, unsigned int int_opt, unsigned int new_state)
Description	Enables the SD Host interrupts
Parameter	● sd_host: The pointer to APB_SD_Host_RegDef structure ● type: Interrupt type – SD_CMD_INT: Command interrupt – SD_DATA_INT: Data interrupt ● int_opt: Interrupt sub-type ● new_state: Interrupt enable state
Return Value	None

5.2.11 apb_sd_host_interrupt_status_get

The definition of the apb_sd_host_interrupt_status_get function is shown in Table 5-29.

Table 5-29 apb_sd_host_interrupt_status_get Function Definition

Prototype	unsigned char apb_sd_host_interrupt_status_get(APB_SD_Host_RegDef* sd_host, sd_interrupt_type type, unsigned int flag)
Description	Retrieves the SD Host interrupt status
Parameter	sd_host: The pointer to APB_SD_Host_RegDef structure type: Interrupt type SD_CMD_INT: Command interrupt SD_DATA_INT: Data interrupt flag: Interrupt sub-type
Return Value	Returns the status of the specified interrupt type

5.2.12 apb_sd_host_interrupt_status_clear

The definition of the apb_sd_host_interrupt_status_clear function is shown in Table 5-30.

Table 5-30 apb_sd_host_interrupt_status_clear Function Definition

Prototype	void apb_sd_host_interrupt_status_clear(APB_SD_Host_RegDef* sd_host, sd_interrupt_type type, unsigned int flag)
Description	Clears the SD Host interrupt status
Parameter	● sd_host: The pointer to APB_SD_Host_RegDef structure ● type: Interrupt type – SD_CMD_INT: Command interrupt – SD_DATA_INT: Data interrupt ● flag: Interrupt sub-type
Return Value	None

5.2.13 apb_sd_host_fifo_status_get

The definition of the apb_sd_host_fifo_status_get function is shown in Table 5-31.

Table 5-31 apb_sd_host_fifo_status_get Function Definition

Prototype	unsigned char apb_sd_host_fifo_status_get(APB_SD_Host_RegDef* sd_host, sd_fifo_type fifo_type)
Description	Retrieves the SD Host FIFO status
Parameter	● sd_host: The pointer to APB_SD_Host_RegDef structure ● fifo_type: – SD_W_FIFO_FULL: Writes FIFO full – SD_W_FIFO_EMPTY: Writes FIFO empty – SD_R_FIFO_FULL: Reads FIFO full – SD_R_FIFO_EMPTY: Reads FIFO empty
Return Value	Returns the status of the specified FIFO

6 TF Card Brands and Types

It is recommended to use Class 10 or higher 8–32GB SDHC cards. The brands that have been tested include SanDisk and aigo.

Examples of tested SD cards:

- SanDisk 32GB TF (MicroSD) Card, A1 U1 C10 Extreme High-Speed Mobile Storage Edition “”.
- aigo 32GB TF (MicroSD) Card, U1 A1 C10 4K Ultra HD / High-Speed Transfer Storage Card “”.

7 Reference Design

Please refer to the Gowin APB SD Host IP Reference Design for details at Gowinsemi website.

- Hardware Reference Design:
  …\ref_design\FPGA_RefDesign\EVAL_XXX_GW5AST138_V1.0\apb_sd_host
- Software Reference Design:
  …\ref_design\MCU_RefDesign\apb_sd_host


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