



DK_START_GW5A-LV25LQ144_V1.0

Development Board

User Guide

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Revision History

Date	Version	Description
02/13/2026	1.0E	Initial version published.
03/27/2026	1.0.1E	“Figure 3-4 Connection Diagram of LVDS Interface Schematic” and “Table 3-4 LVDS-TX Interface (J23) Pin Assignment” updated.
04/24/2026/	1.0.2E	● Note regarding the orientation of the DIP switches added to “Figure 3-9 Connection Diagram of DIP Switch”. ● “Table 3-4 LVDS-TX Interface (J23) Pin Assignment”, “Table 3-5 LVDS_RX Interface (J21) Pin Assignment”, “Table 3-6 LVDS-TX Interface (J28) Pin Assignment”, and “Table 3-7 LVDS_RX Interface (J26) Pin Assignment” updated: correcting the descriptions of certain signals.

Contents

Contents	i
List of Figures	iii
List of Tables	iv
1 About This Guide	1
1.1 Purpose	1
1.2 Related Documents	1
1.3 Terminology and Abbreviations	2
1.4 Support and Feedback	2
2 Development Board Introduction	3
2.1 Overview	3
2.2 A Development Board Kit	4
2.3 PCB Components	5
2.4 System Block Diagram	5
2.5 Features	6
3 Development Board Circuit	7
3.1 FPGA	7
3.2 Power Supply	7
3.2.1 Introduction	7
3.2.2 Power Assignment	8
3.3 Download Module	8
3.3.1 Introduction	8
3.3.2 Pin Assignment	9
3.4 Clock	9
3.4.1 Introduction	9
3.4.2 Pin Assignment	10

3.5 LVDS Interface (FPC)	10
3.5.1 Introduction	10
3.5.2 Pin Assignment	11
3.6 LVDS Interface (PH)	13
3.6.1 Introduction	13
3.6.2 Pin Assignment	13
3.7 GPIO	15
3.7.1 Introduction	15
3.7.2 Pin Assignment	15
3.8 LED & Key & DIP Switch	17
3.8.1 Introduction	17
3.8.2 Pin Assignment	18

List of Figures

Figure 2-1 DK_START_GW5A-LV25LQ144_V1.0 Development Board	3
Figure 2-2 A Development Board Kit	4
Figure 2-3 PCB Components.....	5
Figure 2-4 System Block Diagram	5
Figure 3-1 Power Assignment Diagram.....	8
Figure 3-2 Connection Diagram of Download	8
Figure 3-3 Clock Connection Diagram	9
Figure 3-4 Connection Diagram of LVDS Interface Schematic	10
Figure 3-5 Connection Diagram of LVDS Interface Schematic	13
Figure 3-6 Schematic Connection Diagram of GPIO	15
Figure 3-7 Connection Diagram of LED	17
Figure 3-8 Connection Diagram of Key	17
Figure 3-9 Connection Diagram of DIP Switch	18

List of Tables

Table 1-1 Terminology and Abbreviations	2
Table 3-1 JTAG Pin Assignment	9
Table 3-2 FLASH SPI Interface Pin Assignment	9
Table 3-3 Clock Pin Assignment	10
Table 3-4 LVDS-TX Interface (J23) Pin Assignment.....	11
Table 3-5 LVDS_RX Interface (J21) Pin Assignment	12
Table 3-6 LVDS-TX Interface (J28) Pin Assignment.....	13
Table 3-7 LVDS_RX Interface (J26) Pin Assignment	14
Table 3-8 GPIO Pin Assignment	15
Table 3-9 Pin Assignment	18

1 About This Guide

1.1 Purpose

The DK_START_GW5A-LV25LQ144_V1.0 development board (hereinafter referred to as “the development board”) user guide consists of following three parts:

- A brief introduction to the features of the development board.
- An introduction to the development board system architecture and hardware resources.
- An introduction to the hardware circuits, functions and pin assignment.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [UG985, GW5A-25 Pinout](#)
- [UG1101, GW5A series of FPGA Products Package and Pinout User Guide](#)
- [UG987, GW5A series of FPGA Products Schematic Manual](#)
- [UG714, Arora V 25K FPGA Products Programming and Configuration User Guide](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
LDO	Low Dropout Regulator
LVDS	Low-Voltage Differential Signaling
JTAG	Joint Test Action Group

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Development Board Introduction

2.1 Overview

Figure 2-1 DK_START_GW5A-LV25LQ144_V1.0 Development Board



The DK_START_GW5A-LV25LQ144_V1.0 development board reserves interfaces such as LVDS and GPIO to meet a wide range of application requirements including signal control, data transmission, and software learning and debugging.

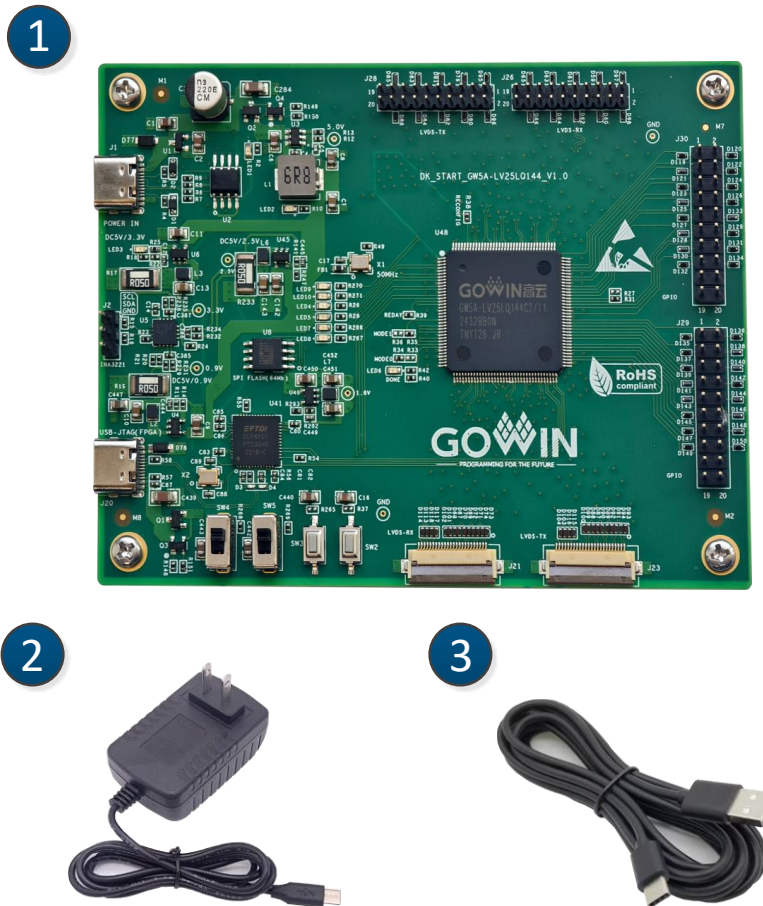
The development board adopts Gowin GW5A-LV25LQ144 FPGA device. For the internal resources of the chip, see [DS1103, GW5A series of FPGA Products Data Sheet](#).

2.2 A Development Board Kit

The development board kit includes the following items:

1. DK_START_GW5A-LV25LQ144_V1.0 development board
2. 12V input Type-C power adapter (Input: AC 100-240V~50/60Hz 0.6A, output: DC12V 2A)
3. Type-A to Type-C interface data cable

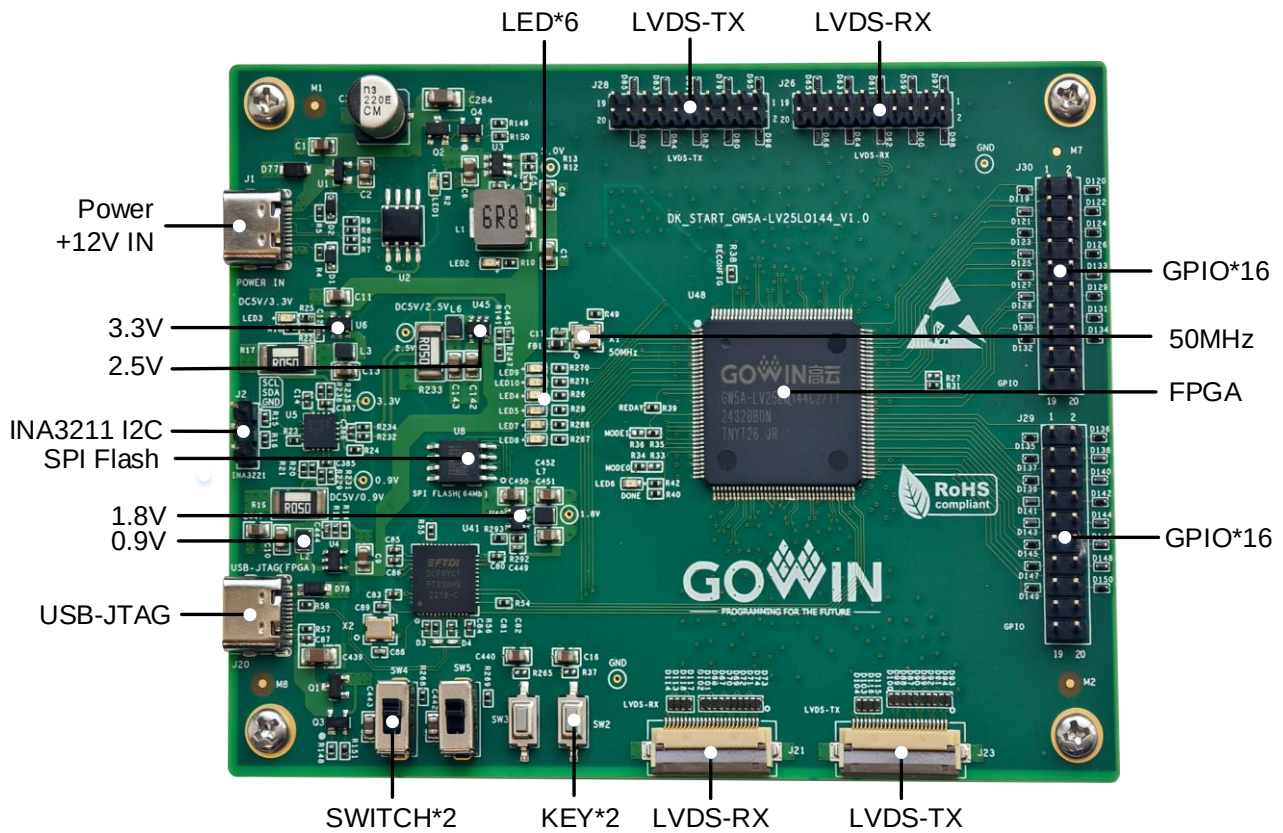
Figure 2-2 A Development Board Kit



- ① DK_START_GW5A-LV25LQ144_V1.0 development board
- ② 12V input Type-C power adapter
- ③ Type-A to Type-C interface data cable

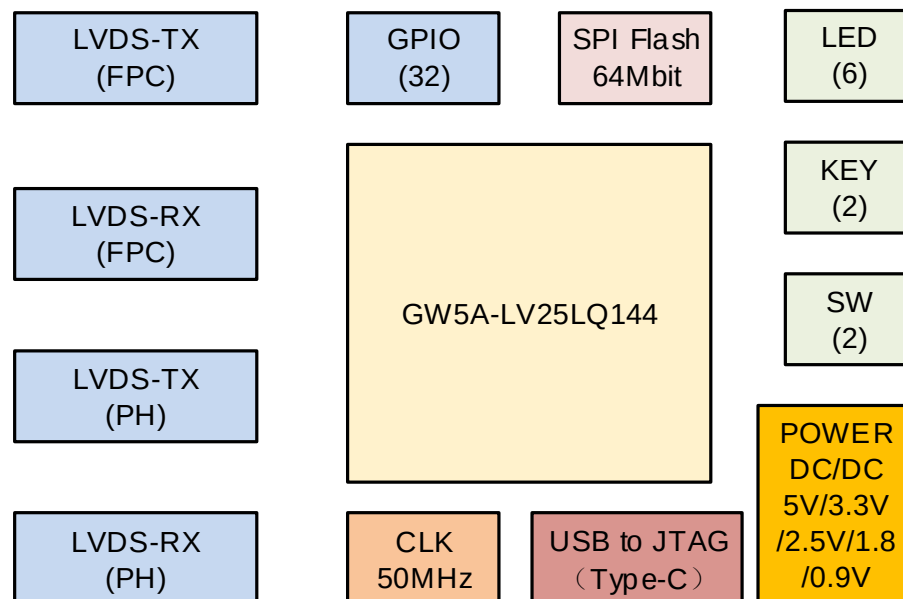
2.3 PCB Components

Figure 2-3 PCB Components



2.4 System Block Diagram

Figure 2-4 System Block Diagram



2.5 Features

The key features are as follows:

- **FPGA Device**
 - The development board adopts GW5A-LV25LQ144 FPGA of Arora V series devices, which is the 5 series products of Gowin Arora family.
- **Download and Boot**
 - Integrates USB download circuit on the development board, download through Type- C interface
 - External SPI flash boot
 - The DONE light is on after loading
- **Power**
 - External DC12V/2A power, Type-C interface
 - The Power light is on after power on.
 - The board generates 0.9V, 1.8V, 2.5V, 3.3V, and 5V power.
- **System clock**
 - 50MHz clock
- **Memory device**
 - 64Mbit Quad SPI Flash Memory
- **LVDS Interface**
 - LVDS_TX interface with dual channels, each channel includes 4 data + 1 clk
 - LVDS_RX interface with dual channels, each channel includes 4 data + 1 clk
- **Keys & LEDs & dip switches**
 - 2 keys
 - 6 LEDs
 - 2 dip switches
- **GPIO interface**
 - 32 GPIOs

3 Development Board Circuit

3.1 FPGA

Overview

For the resources of GW5A series of FPGA Products, refer to [*DS1103, GW5A series of FPGA products*](#).

I/O BANK Introduction

For the I/O BANK, package, and pinout information, see [*UG1101, GW5A Series of FPGA Products Package and Pinout User Guide*](#) for more details.

3.2 Power Supply

3.2.1 Introduction

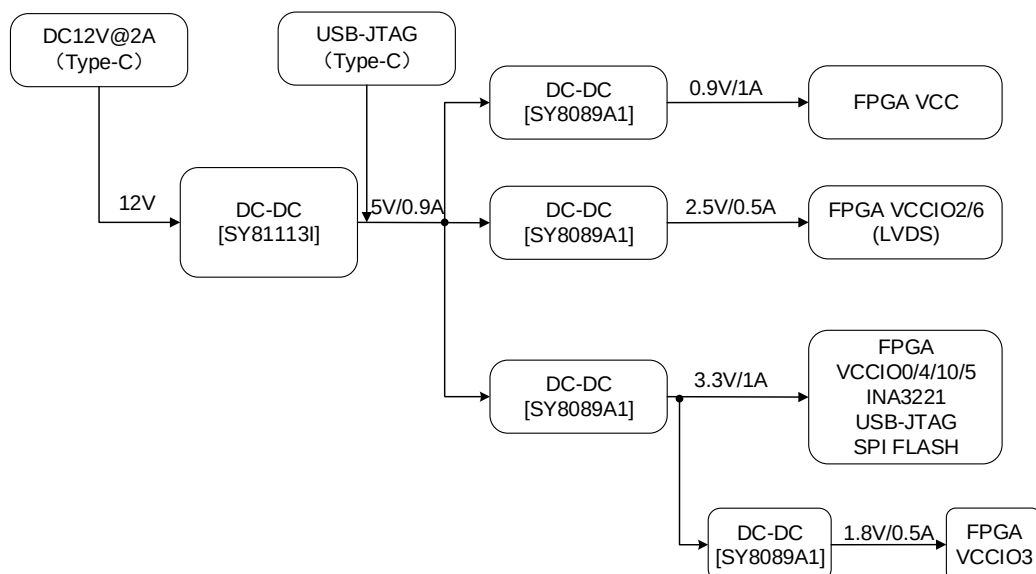
The development board needs to be powered by a 12V power adapter.

The input parameter of the adapter is AC 100-240V~50/60MHz 0.6A, and the output parameter is DC 12V 2A.

The input 12V power is regulated by the PMIC on the development board to generate 0.9V, 1.8V, 2.5V, 3.3V, and 5V power supplies, thus meeting the power supply requirements of the development board.

3.2.2 Power Assignment

Figure 3-1 Power Assignment Diagram



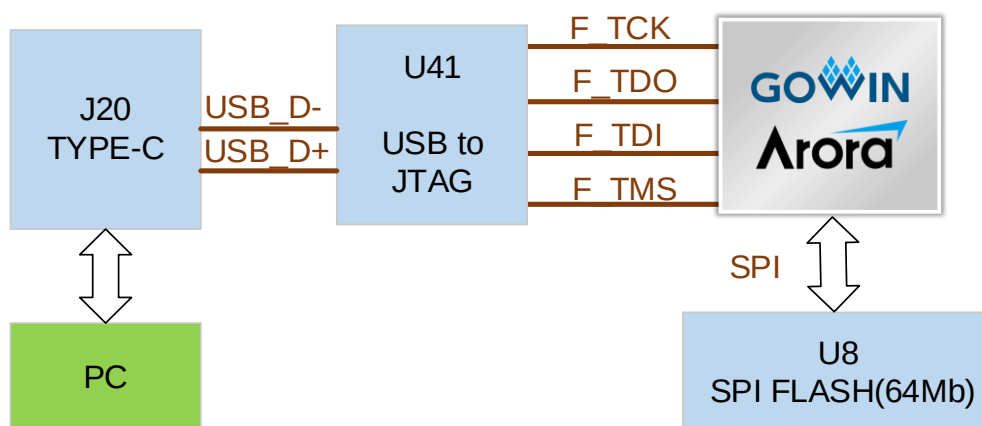
3.3 Download Module

3.3.1 Introduction

The development board provides a Type-C download port (J20) and a USB-JTAG chip (U41, FTDI232). Through this interface, programs can be downloaded to the external SPI Flash (U8, 64 Mbit capacity) or to the FPGA internal SRAM.

The download connection diagram is shown in Figure 3-2.

Figure 3-2 Connection Diagram of Download



3.3.2 Pin Assignment

Table 3-1 JTAG Pin Assignment

Signal Name	FPGA (U48) Pin No.	BANK	I/O Level	Description
F_TCK	71	10	3.3V	JTAG signal
F_TDO	69	10	3.3V	
F_TDI	72	10	3.3V	
F_TMS	68	10	3.3V	

Table 3-2 FLASH SPI Interface Pin Assignment

Signal Name	FPGA(U48) Pin No.	BANK	I/O Level	Description
QSPI_CS_N	16	4	3.3V	SPI FLASH and FPGA interface signals
QSPI_CLK	28	4	3.3V	
QSPI_IO0	27	4	3.3V	
QSPI_IO1	25	4	3.3V	
QSPI_IO2	23	4	3.3V	
QSPI_IO3	24	4	3.3V	

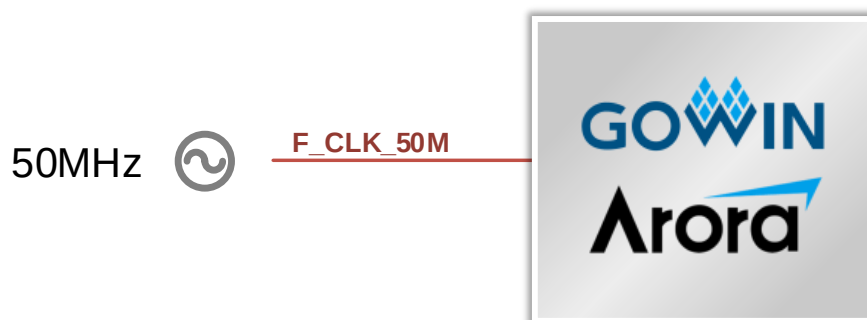
3.4 Clock

3.4.1 Introduction

The clock sources provided on the development board for the FPGA include one 50 MHz single-ended clock, which is connected to the FPGA's dedicated PLL input pin.

The clock pin assignment is shown in Table 3-3.

Figure 3-3 Clock Connection Diagram



3.4.2 Pin Assignment

Table 3-3 Clock Pin Assignment

Signal Name	FPGA (U48) Pin No.	BANK	I/O Level	Description
F_CLK_50M	6	5	3.3V	Frequency 50MHz

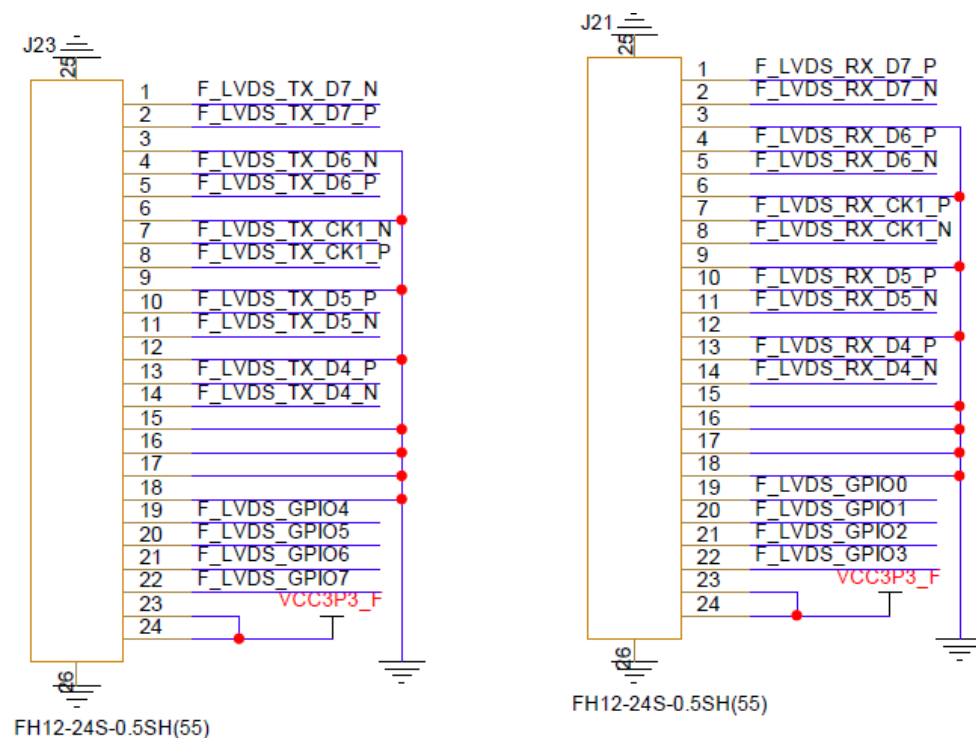
3.5 LVDS Interface (FPC)

3.5.1 Introduction

The DK_START_GW5A-LV25LQ144_V1.0 development board includes FPC-connector LVDS interfaces.

- J23 is an LVDS-TX interface, consisting of 4 data lanes + 1 clock lane.
- J21 is an LVDS-RX interface, consisting of 4 data lanes + 1 clock lane.

Figure 3-4 Connection Diagram of LVDS Interface Schematic



3.5.2 Pin Assignment

Table 3-4 LVDS-TX Interface (J23) Pin Assignment

J23 Pin No.	Signal Name	FPGA (U48) Pin No.	BANK	I/O Level	Description
1	F_LVDS_TX_D7_N	67	2	2.5V	LVDS data
2	F_LVDS_TX_D7_P	66	2	2.5V	LVDS data
3	GND	-	-	-	GND
4	F_LVDS_TX_D6_N	65	2	2.5V	LVDS data
5	F_LVDS_TX_D6_P	64	2	2.5V	LVDS data
6	GND	-	-	-	GND
7	F_LVDS_TX_CK1_N	62	2	2.5V	LVDS clock
8	F_LVDS_TX_CK1_P	61	2	2.5V	LVDS clock
9	GND	-	-	-	GND
10	F_LVDS_TX_D5_P	60	2	2.5V	LVDS data
11	F_LVDS_TX_D5_N	59	2	2.5V	LVDS data
12	GND	-	-	-	GND
13	F_LVDS_TX_D4_P	58	2	2.5V	LVDS data
14	F_LVDS_TX_D4_N	57	2	2.5V	LVDS data
15	GND	-	-	-	GND
16	GND	-	-	-	GND
17	GND	-	-	-	GND
18	GND	-	-	-	GND
19	F_LVDS_GPIO4	56	2		GPIO
20	F_LVDS_GPIO5	54	2		GPIO
21	F_LVDS_GPIO6	52	2		GPIO
22	F_LVDS_GPIO7	50	2		GPIO
23	3.3V	-	-	-	3.3V
24	3.3V	-	-	-	3.3V
25	GND	-	-	-	GND
26	GND	-	-	-	GND

Table 3-5 LVDS_RX Interface (J21) Pin Assignment

J21 Pin No.	Signal Name	FPGA (U48) Pin No.	BANK	I/O Level	Description
1	F_LVDS_RX_D7_P	49	2	2.5V	LVDS data
2	F_LVDS_RX_D7_N	48	2	2.5V	LVDS data
3	GND	-	-	-	GND
4	F_LVDS_RX_D6_P	47	2	2.5V	LVDS data
5	F_LVDS_RX_D6_N	46	2	2.5V	LVDS data
6	GND	-	-	-	GND
7	F_LVDS_RX_CK1_P	41	2	2.5V	LVDS clock
8	F_LVDS_RX_CK1_N	39	2	2.5V	LVDS clock
9	GND	-	-	-	GND
10	F_LVDS_RX_D5_P	45	2	2.5V	LVDS data
11	F_LVDS_RX_D5_N	44	2	2.5V	LVDS data
12	GND	-	-	-	GND
13	F_LVDS_RX_D4_P	43	2	2.5V	LVDS data
14	F_LVDS_RX_D4_N	42	2	2.5V	LVDS data
15	GND	-	-	-	GND
16	GND	-	-	-	GND
17	GND	-	-	-	GND
18	GND	-	-	-	GND
19	F_LVDS_GPIO0	122	6		GPIO
20	F_LVDS_GPIO1	123	6		GPIO
21	F_LVDS_GPIO2	124	6		GPIO
22	F_LVDS_GPIO3	125	6		GPIO
23	3.3V	-	-	-	3.3V
24	3.3V	-	-	-	3.3V
25	GND	-	-	-	GND
26	GND	-	-	-	GND

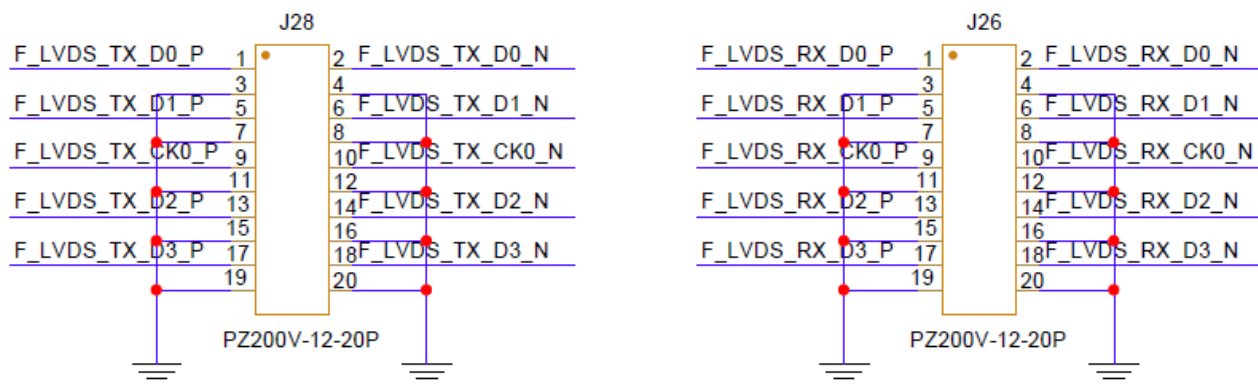
3.6 LVDS Interface (PH)

3.6.1 Introduction

The DK_START_GW5A-LV25LQ144_V1.0 development board includes PH-connector LVDS interfaces with 2.0 mm pitch header.

- J28 is an LVDS-TX interface, consisting of 4 data lanes + 1 clock lane.
- J26 is an LVDS-RX interface, consisting of 4 data lanes + 1 clock lane.

Figure 3-5 Connection Diagram of LVDS Interface Schematic



3.6.2 Pin Assignment

Table 3-6 LVDS-TX Interface (J28) Pin Assignment

J28 Pin No.	Signal Name	FPGA (U48) Pin No.	BANK	I/O Level	Description
1	F_LVDS_TX_D0_P	126	6	2.5V	LVDS data
2	F_LVDS_TX_D0_N	128	6	2.5V	LVDS data
3	GND	-	-	-	GND
4	GND	-	-	-	GND
5	F_LVDS_TX_D1_P	129	6	2.5V	LVDS data
6	F_LVDS_TX_D1_N	130	6	2.5V	LVDS data
7	GND	-	-	-	GND
8	GND	-	-	-	GND
9	F_LVDS_TX_CK0_P	131	6	2.5V	LVDS clock
10	F_LVDS_TX_CK0_N	134	6	2.5V	LVDS clock
11	GND	-	-	-	GND
12	GND	-	-	-	GND
13	F_LVDS_TX_D2_P	133	6	2.5V	LVDS data

J28 Pin No.	Signal Name	FPGA (U48) Pin No.	BANK	I/O Level	Description
14	F_LVDS_TX_D2_N	135	6	2.5V	LVDS data
15	GND	-	-	-	GND
16	GND	-	-	-	GND
17	F_LVDS_TX_D3_P	136	6	2.5V	LVDS data
18	F_LVDS_TX_D3_N	137	6	2.5V	LVDS data
19	GND	-	-	-	GND
20	GND	-	-	-	GND

Table 3-7 LVDS_RX Interface (J26) Pin Assignment

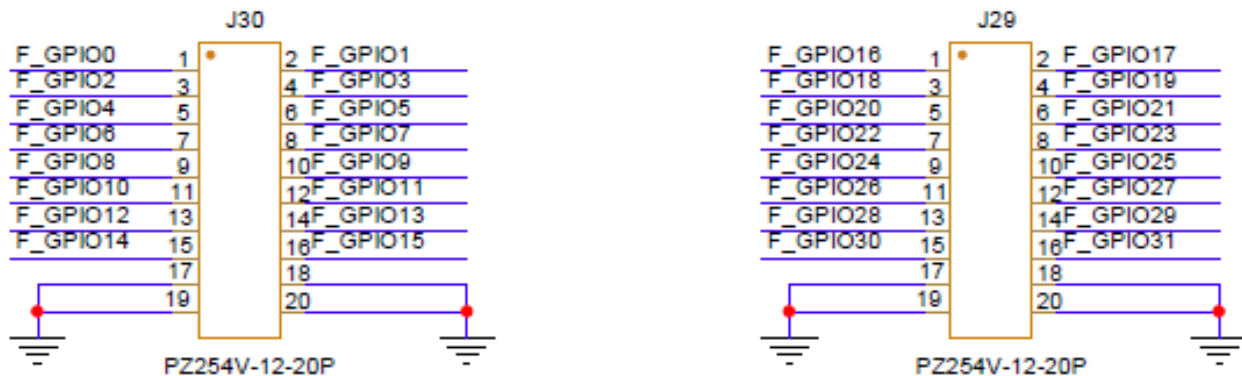
J26 Pin No.	Signal Name	FPGA (U48) Pin No.	BANK	I/O Level	Description
1	F_LVDS_RX_D0_P	112	6	2.5V	LVDS data
2	F_LVDS_RX_D0_N	110	6	2.5V	LVDS data
3	GND	-	-	-	GND
4	GND	-	-	-	GND
5	F_LVDS_RX_D1_P	116	6	2.5V	LVDS data
6	F_LVDS_RX_D1_N	115	6	2.5V	LVDS data
7	GND	-	-	-	GND
8	GND	-	-	-	GND
9	F_LVDS_RX_CK0_P	114	6	2.5V	LVDS clock
10	F_LVDS_RX_CK0_N	113	6	2.5V	LVDS clock
11	GND	-	-	-	GND
12	GND	-	-	-	GND
13	F_LVDS_RX_D2_P	118	6	2.5V	LVDS data
14	F_LVDS_RX_D2_N	119	6	2.5V	LVDS data
15	GND	-	-	-	GND
16	GND	-	-	-	GND
17	F_LVDS_RX_D3_P	120	6	2.5V	LVDS data
18	F_LVDS_RX_D3_N	121	6	2.5V	LVDS data
19	GND	-	-	-	GND
20	GND	-	-	-	GND

3.7 GPIO

3.7.1 Introduction

The DK_START_GW5A-LV25LQ144_V1.0 development board routes out 32 GPIOs through the double-row pin header with 2.54mm pitch.

Figure 3-6 Schematic Connection Diagram of GPIO



3.7.2 Pin Assignment

Table 3-8 GPIO Pin Assignment

Signal Name	FPGA (U48) Pin No.	BANK	IO Level
F_GPIO0	140	5	3.3V
F_GPIO1	106	7	3.3V
F_GPIO2	105	7	3.3V
F_GPIO3	104	7	3.3V
F_GPIO4	102	7	3.3V
F_GPIO5	101	7	3.3V
F_GPIO6	99	7	3.3V
F_GPIO7	98	7	3.3V
F_GPIO8	97	7	3.3V
F_GPIO9	96	7	3.3V
F_GPIO10	94	0	3.3V
F_GPIO11	93	0	3.3V
F_GPIO12	92	0	3.3V
F_GPIO13	90	0	3.3V

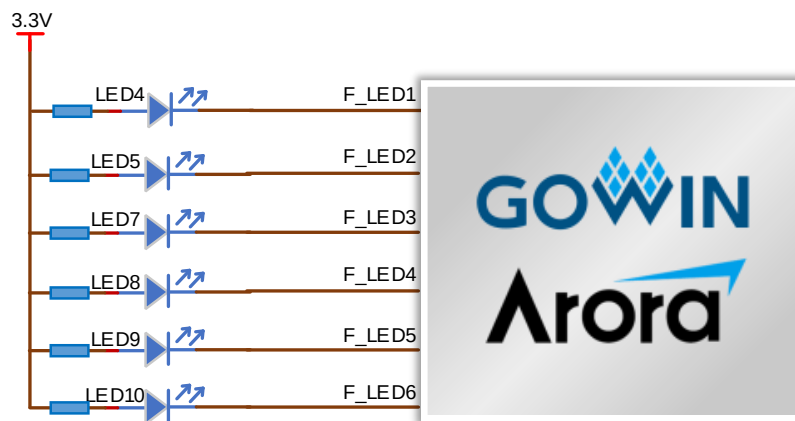
Signal Name	FPGA (U48) Pin No.	BANK	IO Level
F_GPIO14	19	4	3.3V
F_GPIO15	20	4	3.3V
F_GPIO16	22	4	3.3V
F_GPIO17	88	0	3.3V
F_GPIO18	87	0	3.3V
F_GPIO19	86	0	3.3V
F_GPIO20	85	0	3.3V
F_GPIO21	84	0	3.3V
F_GPIO22	83	1	3.3V
F_GPIO23	82	1	3.3V
F_GPIO24	80	1	3.3V
F_GPIO25	79	1	3.3V
F_GPIO26	78	1	3.3V
F_GPIO27	32	3	1.8V
F_GPIO28	76	1	3.3V
F_GPIO29	75	1	3.3V
F_GPIO30	34	3	1.8V
F_GPIO31	35	3	1.8V

3.8 LED & Key & DIP Switch

3.8.1 Introduction

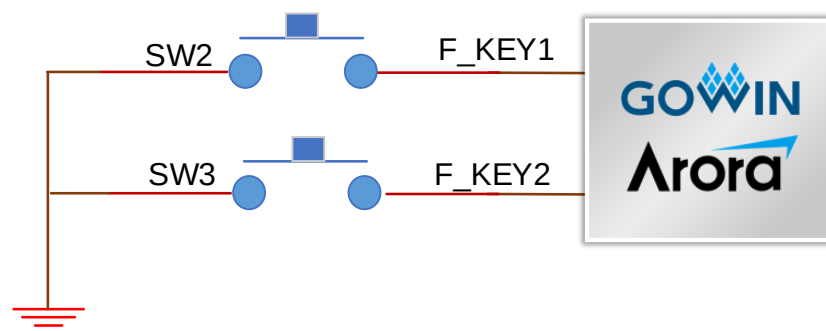
The DK_START_GW5A-LV25LQ144_V1.0 development board includes six LEDs. The LEDs are connected to the IO of FPGA BANK5 and can be switched on and off via the program. The LEDs will be on when the IO voltage is low. The user LEDs will be off when the IO voltage is high. The connection diagram is shown in Figure 3-7.

Figure 3-7 Connection Diagram of LED



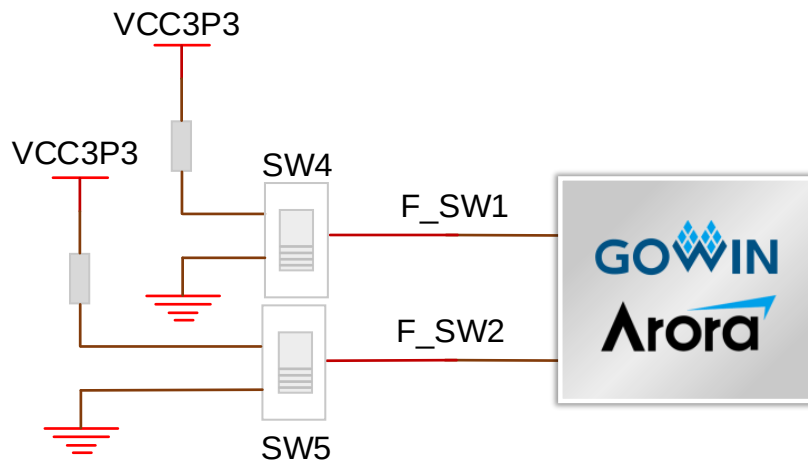
There are two keys on the development board. The keys are respectively connected to the general IOs of FPGA BANK4. The corresponding IO input voltage of the FPGA is low when the key is pressed. The connection diagram is shown in Figure 3-8.

Figure 3-8 Connection Diagram of Key



There are two DIP switches on the development board. The DIP switches are respectively connected to the general IOs of FPGA BANK4. The connection diagram is as follows.

Figure 3-9 Connection Diagram of DIP Switch

**Note!**

The pins of the DIP switches on the side closest to the board edge are connected to ground (GND).

3.8.2 Pin Assignment

Table 3-9 Pin Assignment

Signal Name	FPGA (U48) Pin No.	BANK	I/O Level	Description
F_LED1	3	5	3.3V	LED
F_LED2	4	5	3.3V	LED
F_LED3	7	5	3.3V	LED
F_LED4	8	5	3.3V	LED
F_LED5	143	5	3.3V	LED
F_LED6	144	5	3.3V	LED
F_KEY1	10	4	3.3V	Key
F_KEY2	11	4	3.3V	Key
F_SW1	13	4	3.3V	Dip switch
F_SW2	14	4	3.3V	Dip switch

