



Gowin TDC IP User Guide

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1 About This Guide

1.1 Purpose

Gowin TDC IP user guide aims to help users quickly learn the functions, features, and usage of Gowin TDC IP. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.11.02. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at www.gowinsemi.com:

- *DS100, GW1N series of FPGA Products Data Sheet*
- *DS117, GW1NR series of FPGA Products Data Sheet*
- *DS821, GW1NS series of FPGA Products Data Sheet*
- *DS861, GW1NSR series of FPGA Products Data Sheet*
- *DS841, GW1NZ series of FPGA Products Data Sheet*
- *DS961, GW2ANR series of FPGA Products Data Sheet*
- *DS102, GW2A series of FPGA Products Data Sheet*
- *DS226, GW2AR series of FPGA Products Data Sheet*
- *DS971, GW2AN-18X &9X Data Sheet*
- *DS976, GW2AN-55 Data Sheet*
- *DS981, GW5AT series of FPGA Products Data Sheet*
- *DS1103, GW5A series of FPGA Products Data Sheet*
- *DS1239, GW5AST series of FPGA Products Data Sheet*
- *DS1105, GW5AS series of FPGA Products Data Sheet*

- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1118, GW5ART series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in [Table 1-1](#).

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
IP	Intellectual Property
LUT	Look-up Table
TDC	Time-to-Digital Converter

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

Gowin TDC IP can achieve the function of measuring the pulse width of the input signals.

Table 2-1 Gowin TDC IP Overview

Gowin TDC IP	
Logic Resource	See Table 3-1 .
Delivered Doc.	
Design Files	Verilog (encryption)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.11.02 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

3 Features and Performance

3.1 Features

- Low resource utilization
- Precision up to nanosecond level
- Maximum measurement range is configurable via parameters

3.2 Operating Frequency

The operating frequency of Gowin TDC IP depends on the precision required by the IP, as detailed in [4.1 Clock](#).

3.3 Resource Utilization

[Table 3-1](#) shows the resource utilization under a certain configuration. The resource utilization varies with different configurations, and an assessment needs to be made based on the actual situation.

Table 3-1 Resource Utilization

LUTs	REGs	Device Series	Speed Level
64	36	GW1N-9	C6/I5

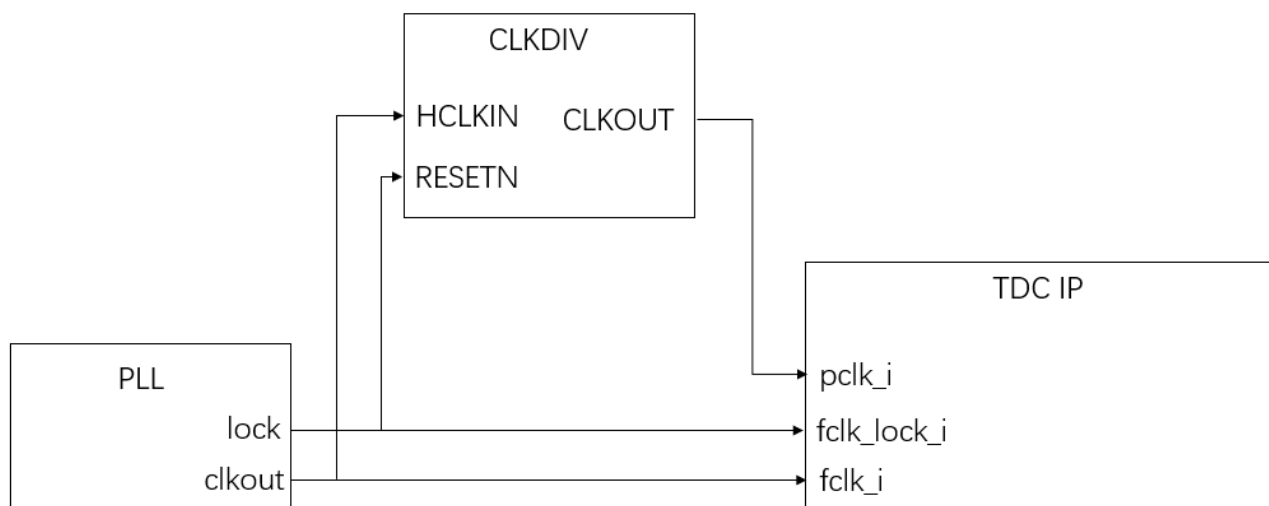
4 Functional Description

4.1 Clock

When using the IP, users must provide the correct clock topology as shown in the diagram below to ensure proper operation of the IP. The division factor for CLKDIV must be configured as "4".

If multiple Gowin TDC IPs are instantiated with the same precision, the pclk_i, fclk_i, and fclk_lock_i signals can be shared among them. The frequency of pclk is equal to the PLL output clock frequency divided by 4.

Figure 4-1 Clock Block Diagram



4.2 Precision

The TDC precision refers to the minimum resolution that the TDC can measure. It is calculated using the following formula:

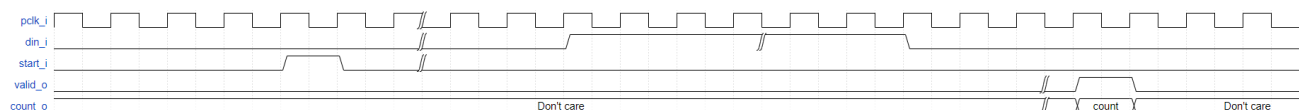
$$\text{Precision} = 1/(\text{fclk} \times 2)$$

And the fclk is the frequency of the PLL output clock.

4.3 Measurement

Gowin TDC IP begins a measurement when the start_i signal transitions from 0 to 1. When a high level is detected on din_i, the IP starts recording the duration of the high pulse and stops recording when din_i transitions to low. Afterward, the IP outputs the measurement result. When valid_o is 1, the output value on count_o is the valid measurement result.

Figure 4-2 Measurement Timing Diagram



As shown in the figure above, users must assert start_i before the din_i pulse occurs to enable the IP to monitor the arrival of pulse. After the pulse ends, valid_o outputs a high level for one clock cycle, during which count_o outputs the valid measurement result. The measurement result is calculated as: $\text{count_o}/(\text{fclk} \times 2)$, and the fclk is the frequency of the PLL output clock.

5 Port List

The IO port of Gowin TDC IP is shown in [Table 5-1](#).

Table 5-1 Gowin TDC IP IO Port List

Signal	I/O	Data Width	Description
Clock input			
fclk_i	input	1	High-speed clock input, typically generated by the PLL. The clock frequency determines the TDC precision.
pclk_i	input	1	Low-speed clock input, typically generated by CLKDIV. The frequency is 1/4 of fclk.
Control signal			
fclk_lock_i	input	1	Lock lock indicator for fclk_i 1: Unlocked 0: Unlocked
rstn_i	input	1	Reset signal input, active-low.
Measurement signal			
din_i	input	1	Measurement signal input
start_i	input	1	Measurement start signal. When this input transitions from 0 to 1, the IP begins monitoring and measuring the input pulse signals.
Measurement results			
count_o	output	Count Width	Measurement result output; it is valid when valid_o is high.
valid_o	output	1	Indicates a valid measurement result. Outputs a high level for one cycle after each measurement; and high level indicates count_o is valid.

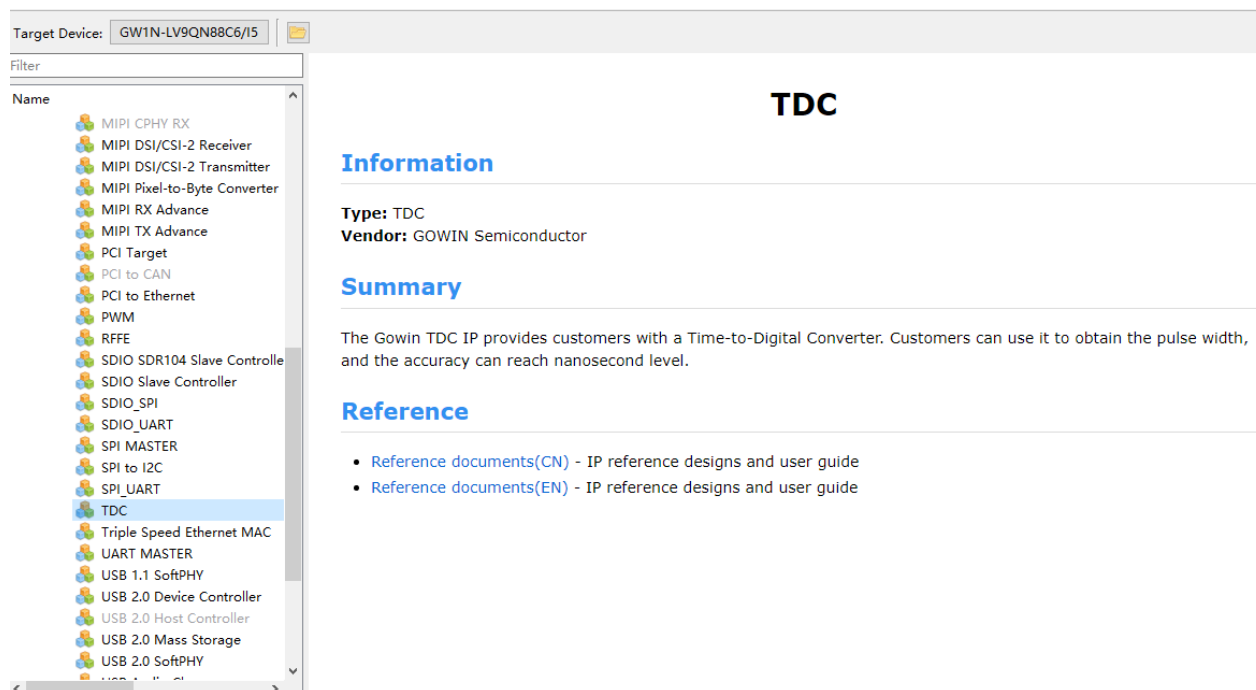
6 Interface Configuration

You can invoke and configure Gowin TDC IP using the IP Core Generator tool in the IDE. This section will introduce the configuration interface, the configuration process, and the configuration options.

1. Open IP Core Generator.

After creating the project, click the "Tools" tab in the upper left, click "IP Core Generator" from the drop-down list to open Gowin IP Core Generator, and select "TDC", as shown in Figure 6-1.

Figure 6-1 Select TDC



2. Open TDC configuration interface.

The left of the configuration interface displays Gowin TDC IP ports diagram, and the right displays the IP configuration options, as shown in Figure 6-2.

Figure 6-2 Gowin TDC IP Configuration Interface

TDC

General

Device: GW1N-9 Device Version: C

Part Number: GW1N-LV9QN88C6/I5 Language: Verilog

File Name: tdc Module Name: TDC_Top

Create In: [Browse]

Options

Count Width: 8 (2~32)

OK Cancel

The descriptions of parameter configuration of Gowin TDC IP are as follows.

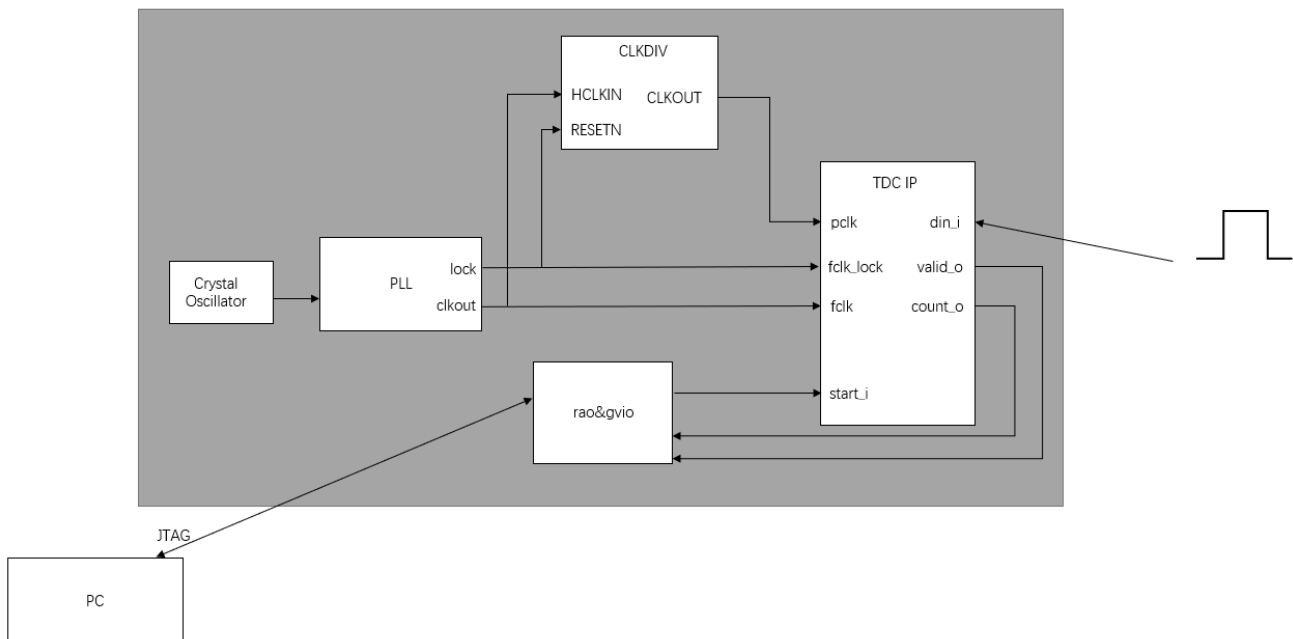
Count Width: The bit width of the measurement output, with a range of 2 to 32. This parameter affects the maximum range of the IP, and is calculated as follows:

Suppose the maximum expected measurement pulse duration is T , and the frequency of $fclk$ is F . The value of this parameter is the integer part of $\lceil \log_2(2 \cdot F \cdot T) + 1 \rceil$.

7 Reference Design

For more information, please see Gowin TDC IP [reference design](#) at Gowin website.

Figure 7-1 Reference Design Block Diagram



As shown in the figure above, Gowin TDC IP is instantiated in the reference design and the PLL and CLKDIV modules are invoked to provide the necessary clocks and signals for the IP. Meanwhile, an external signal to be measured must be provided by the user and input to the `din_i` input of the IP. In this design, the RAO tool is used to observe the measurement results from the IP, while the GVIO tool is used to drive the control signals of Gowin TDC IP. Users can dynamically configure Gowin TDC IP by modifying the GVIO signal values through Gowin IDE via JTAG.

The operation steps are as follows:

1. Download the fs to the development board.
2. Open Gowin Analyzer Oscilloscope tool in Gowin IDE.



3. Click Gvio Core “” button to enable the GVIO tool.

4. Use GVIO to set `tdc_rstn = 1` to release the IP reset.



5. Click Analyzer Oscilloscope “” button to start signal capture.

6. Use GVIO to set `tdc_start = 1` to initiate a measurement.

7. Generate an external input pulse signal externally. At this point, the Analyzer Oscilloscope will trigger once. The user can then read the value of `count_o` to calculate IP's measurement result of the pulse width.

