



Gowin AHB to APB Sync Down IP User Guide

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Revision History

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1 About This Guide

1.1 Purpose

The purpose of Gowin AHB to APB Sync Down IP User Guide is to help you learn the features and usage of Gowin AHB to APB Sync Down IP by providing the descriptions of the functions, signals, parameters, and reference design, etc. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.11.01 (64-bit). As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- [SUG100, Gowin Software User Guide](#)
- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS821, GW1NS series of FPGA Products Data Sheet](#)
- [DS861, GW1NSR series of FPGA Products Data Sheet](#)
- [DS841, GW1NZ series of FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS971, GW2AN-18X & 9X Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)

- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1118, GW5ART series of FPGA Products Data Sheet](#)

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
FPGAs	Field Programmable Gate Array
IP	Intellectual Property

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Introduction

Gowin AHB to APB Sync Down IP is a protocol converter that is used to convert the AMBA AHB protocol to the AMBA APB protocol, enabling AHB masters to access APB slaves.

Table 2-1 Gowin AHB to APB Sync Down IP Overview

Gowin AHB to APB Sync Down IP	
Logic Resource	Please refer to Table 2-2 .
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.11.01 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features

Gowin AHB to APB Sync Down IP includes the following features:

- Supports APB2, APB3, and APB4 protocols.
- Operates the APB interface in a semi-synchronous manner, running at a lower speed than the AHB interface.

2.3 Resource Utilization

Gowin AHB to APB Sync Down IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW5AT series of FPGA as an instance, the resource utilization of Gowin AHB to APB Sync Down IP is as shown in [Table 2-2](#).

Table 2-2 Resource Utilization

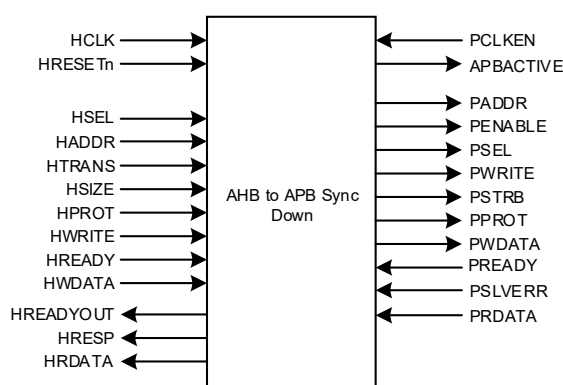
Device	Resource	Resource Utilization	Configuration
GW5AT	Logic	59	Address Width: 64KB
	Register	57	
	BSRAM	0	

3 Functional Description

Structure Diagram

The structure diagram of Gowin AHB to APB Sync Down IP is shown in [Figure 3-1](#).

Figure 3-1 Structure Diagram



The AHB-to-APB bridge has an output signal called APBACTIVE, which is used to control the clock gating unit to generate a PCLK clock gate, referred to as PCLKG. When there are no APB transfers, the APBACTIVE signal remains low, stopping PCLKG. Peripherals designed with independent clock pins for bus logic and peripheral operations can use PCLK clock gating to reduce power consumption.

The AHB to APB Sync Down requires an APB clock synchronized with HCLK. Through the PCLKEN signal, PCLK can either remain equal to HCLK or be a divided version of HCLK.

When the system follows the AMBA 2.0 protocol, the PSLVERR signal can be set to low, and the PREADY signal can be set to high.

For APB2 and APB3 peripheral systems, the PPROT[2] and PSTRB[3:0] signals can be ignored.

In systems where HCLK is equal to PCLK, if the APB slave device does not generate an error response, the minimum cycle for each read/write operation is three HCLK cycles.

If PCLKEN is set to high, then PCLK equals HCLK. If PCLKEN toggles every HCLK cycle, then PCLK is a divided version of HCLK.

4 Signal Descriptions

The port descriptions of Gowin AHB to APB Sync Down IP are as shown in [Table 4-1](#).

Table 4-1 Signal Descriptions

Signal	I/O	Data Width	Description
HCLK	input	1	System bus clock
HRESETn	input	1	System bus reset
PCLKEN	input	1	APB clock enable
HSEL	input	1	Device selection
HADDR	input	[ADDRWIDTH ^[1] - 1:0]	Address
HTRANS	input	[1:0]	Transfer control
HSIZE	input	[2:0]	Transfer size
HPROT	input	[3:0]	Protection control
HWRITE	input	1	Write control
HREADY	input	1	Transmission done
HWDATA	input	[31:0]	Write data
HREADYOUT	output	1	Device ready
HRDATA	output	[31:0]	Read data
HRESP	output	1	Device response
PADDR	output	[ADDRWIDTH ^[1] - 1:0]	APB address
PENABLE	output	1	APB enable
PWRITE	output	1	APB write
PSTRB	output	[3:0]	APB byte strobe
PPROT	output	[2:0]	APB protection
PWDATA	output	[31:0]	APB write data
PSEL	output	1	APB selection

Signal	I/O	Data Width	Description
APBACTIVE	output	1	APB bus activity status, used for APB bus clock gating.
PRDATA	input	[31:0]	Read data of each APB slave device
PREADY	input	1	Ready signal of each APB slave device
PSLVERR	input	1	Error status of each APB slave device

Note!

^[1]ADDRWIDTH is the value of the Address Width option.

5 Parameter Description

The parameter descriptions of Gowin AHB to APB Sync Down IP are as shown in [Table 5-1](#).

Table 5-1 Parameter Description

Name	Description	Value	Default
Address Width	Address bus width	1KB - 256MB	64KB

6 Interface Configuration

You can select IP Core Generator Tool in Gowin Software to call and configure Gowin AHB to APB Sync Down IP.

Select "Tools > IP Core Generator" on the menu bar or click the " " on the tool bar to open IP Core Generator; then select "Soft IP Core > Microprocessor System > Bus Interconnect > AHB to APB Sync Down 1.0".

Gowin AHB to APB Sync Down IP interface configuration is as shown in [Figure 6-1](#).

Figure 6-1 Interface Configuration

The screenshot shows the 'IP Customization' window for the 'AHB to APB Sync Down' IP core. The window is divided into several sections:

- General Section:** Contains fields for Device (GW5AT-60), Device Version (ES), Part Number (GW5AT-LV60UG225ES), Language (Verilog), File Name (ahb_to_apb_sync_down), Module Name (AHB_to_APB_Sync_Down_Top), and Create In (C:\Users\liukai\Desktop\fpga_project\src\ahb_to_apb_sync_down).
- Options Section:** Contains a dropdown for Address Width, currently set to 64KB.
- Port Diagram:** A schematic diagram on the left showing the input and output ports of the IP core. Inputs include HCLK, HRESETn, PC LKEN, HSEL, HADDR[15:0], HTRANS[1:0], HSIZE[2:0], HPROT[3:0], HWRITE, HREADY, HWDATA[31:0], PRDATA[31:0], PREADY, and PSU/ERR. Outputs include HREADYOUT, HRDATA[31:0], HRESP, PADDR[15:0], PENABLE, PWRITE, PTRB[3:0], PPROT[2:0], PWDATA[31:0], PSEL, and APBACT/IE.

At the bottom right, there are 'OK' and 'Cancel' buttons.

The option configuration includes Address Width, which defines the width of the address bus. The available range is 1KB - 256MB, with a default value of 64KB.

7 Reference Design

See Gowin AHB to APB Sync Down IP [Reference Design](#) for details at Gowinsemi website.

- Hardware Reference Design:

...

`\ref_design\FPGA_RefDesign\DK_START_GW5AST138_V1.0\ahb_to_apb_sync_down`

- Software Reference Design:

`...\ref_design\MCU_RefDesign\ahb_to_apb_sync_down`

