



Gowin SDI Decoder IP User Guide

IPUG1204-1.4E, 01/16/2026

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Revision History

Date	Version	Description
04/11/2025	1.0E	Initial version published.
05/14/2025	1.1E	● Audio supported. ● Hot-plugging supported.
07/25/2025	1.2E	● 3G Level B DS decoding supported. ● Automatic rate detection between HD-SDI/3G-SDI supported. ● IP port diagram and corresponding port descriptions updated.
09/12/2025	1.3E	● Level B DL function added. ● The output value of the O_level_b_ds_rate register modified: changed from 1 to 2 under Level B DS condition.
01/16/2026	1.4E	● i and psf resolutions supported. ● Modified the O_level register output values to level a = 0, level b ds = 1, and level b dl = 2.

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1 About This Guide

1.1 Purpose

The purpose of Gowin SDI Decoder IP is to help you learn the features and usage of Gowin SDI Decoder IP by providing the descriptions of features, functions, ports, timing, GUI and reference design, etc. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.12.01 (64-bit). As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at www.gowinsemi.com:

- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1118, GW5ART series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
DE	Data Enable
FPGA	Field Programmable Gate Array
HS	Horizontal Sync
IP	Intellectual Property
SDI	Serial Digital Interface

Terminology and Abbreviations	Meaning
SerDes	Serializer/Deserializer
SMPTE	Society of Motion Picture and Television Engineers
VESA	Video Electronics Standards Association
VS	Vertical Sync

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Overview

The Serial Digital Interface (SDI) is a member of the digital video interface family and is used for transmitting digital video signals. Gowin SDI Decoder IP can be operated under HD or 3G rate standards defined by the Society of Motion Picture and Television Engineers (SMPTE), converting SDI signals into video signals.

Table 2-1 Gowin SDI Decoder IP Overview

Gowin SDI Decoder IP	
Logic Resource	Please refer to Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.11 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features

- Operates with 1 lane
- Supports link rates of 1.485/2.97 Gbps per lane
- Supports HD-SDI and 3G-SDI
- Supports audio
- Supports hot-plugging
- Supports Level B DS
- Supports automatic rate detection between HD-SDI/3G-SDI
- Supports Level B DL

2.3 Resource Utilization

Gowin SDI Decoder IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW5AT series of FPGA as an instance, the resource utilization of Gowin SDI Decoder IP is as shown in Table 2-2.

Table 2-2 Gowin SDI Decoder IP Resource Utilization

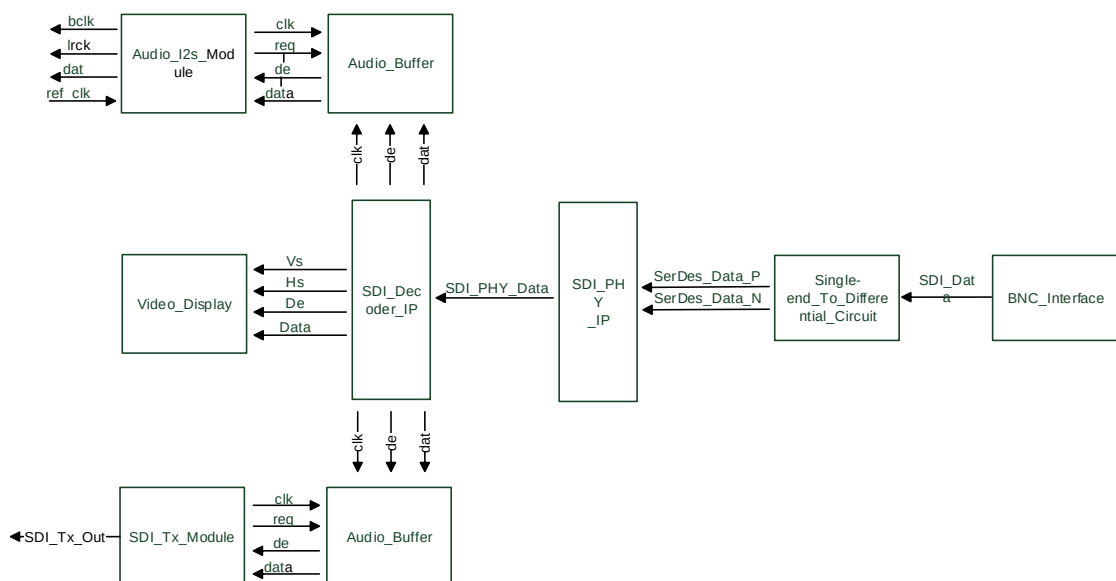
Device	GW5AT-60
Register	1326
LUT	1004
BSRAM	14

3 Functional Description

3.1 System Block Diagram

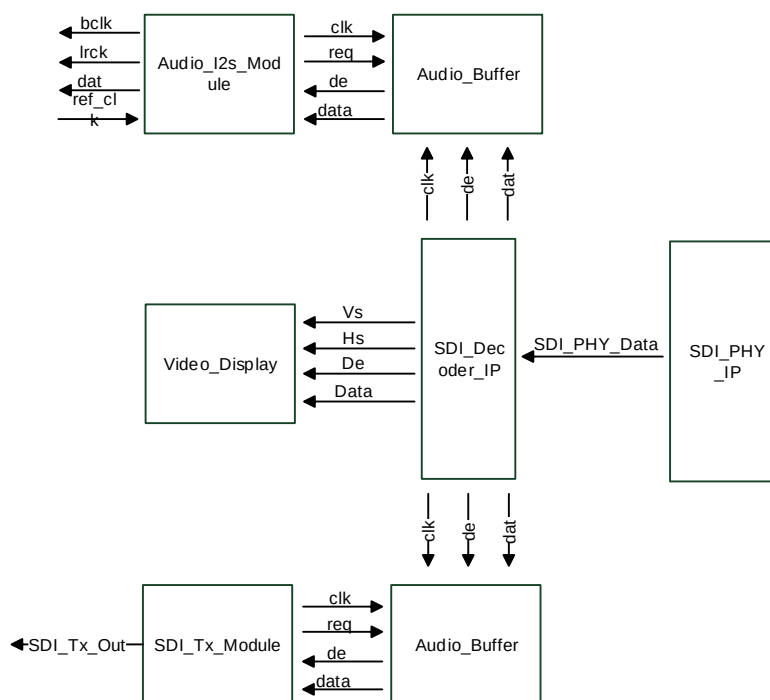
Gowin SDI Decoder IP can receive data from Gowin SDI PHY IP and convert it into video data. The block diagram of Gowin SDI Decoder IP is as shown in Figure 3-1.

Figure 3-1 Gowin SDI Decoder IP Block Diagram



3.2 Function Module

Figure 3-2 Gowin SDI Decoder IP Structure Diagram



As shown in the diagram above, Gowin SDI Decoder IP receives data from Gowin SDI PHY IP and decodes it into video data.

3.3 Supported Format

Table 3-1 shows the formats supported by Gowin SDI Decoder IP.

Table 3-1 Formats Supported by Gowin SDI Decoder IP

Standard	HD-SDI and Level B DS					3G-SDI	
Hor Addr Pixel	1280	1280	1920	1920	1920	1920	1920
Ver Addr Line	720	720	1080	1080	1080	1080	1080
Hor Total Pixel	1650	1980	2200	2640	2750	2200	2640
Ver Total Line	750	750	1125	1125	1125	1125	1125
Scan Mode	P	P	P,PSF,I	P,PSF,I	P,PSF	P	P
Frame Rate	60P 59.94P	50P	30P/PSF 60I 29.97P/PSF 59.94I	25P/PSF 50I	24P/PSF 23.98P/PSF	60P 59.94P	50P
Bit Per Word	20	20	20	20	20	20	20
Word Rate(Mhz)	74.25	74.25	74.25	74.25	74.25	148.5	148.5
Pixel Sample Rate(Mhz)	74.25	74.25	74.25	74.25	74.25	148.5	148.5

Standard	HD-SDI and Level B DS					3G-SDI	
Structure	YC4:2:2	YC4:2:2	YC4:2:2	YC4:2:2	YC4:2:2	YC4:2:2	YC4:2:2
Pixel Depth	10	10	10	10	10	10	10

3.4 Port List

The IO ports vary slightly depending on the parameters.

The details of IO port of Gowin SDI Decoder IP are shown in Table 3-2.

Table 3-2 I/O List of Gowin SDI Decoder IP

Signal Name	Direction	Width	Description
I_rst_n	I	1	Reset signal, active low.
I_drp_clk	I	1	DRP port configuration clock
I_q_sel	I	1	SerDes Q selection 0: Q0 1: Q1
I_lane_mask	I	4	SerDes Lane enable: 4'b0001: lane 0 enable 4'b0010: lane 1 enable 4'b0100: lane 2 enable 4'b1000: lane 3 enable
O_drp_wren	O	1	DRP port write enable (connect according to the reference design; no user operation required).
O_drp_addr	O	24	DRP port write address (connect according to the reference design; no user operation required).
O_drp_wrdata	O	32	DRP port write data (connect according to the reference design; no user operation required).
O_drp_rden	O	1	DRP port read enable (connect according to the reference design; no user operation required).
I_drp_rddata	I	32	DRP port read data ((connect according to the reference design; no user operation required).
I_drp_rdvld	I	1	DRP port read valid (connect according to the reference design; no user operation required).
I_drp_ready	I	1	DRP port read ready (connect according to the reference design; no user operation required).
I_fix_rate_en	I	1	Reserved
I_fix_rate	I	3	Reserved
I_fix_mfactor	I	1	Reserved
I_clk	I	1	Clock input
I_data	I	88	Data input
I_clk_half	I	1	Clock input at half the frequency of I_clk, used for Level B DS.
O_locked	O	1	SerDes lock status: 0: Not locked 1: Locked
O_level	O	2	Level output:

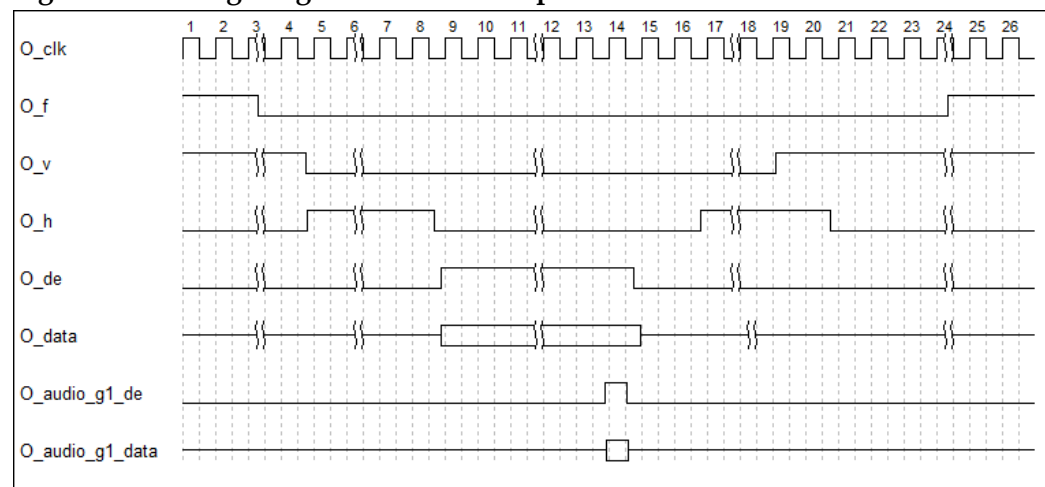
Signal Name	Direction	Width	Description
			0: Level A 1: Level B DS 2: Level B DL 3: Reserved
O_clk	O	1	Receive clock output
O_interlace_trans	O	1	Transmission mode output: 0: Interlaced transmission (I) 1: Progressive transmission (P)
O_interlace	O	1	Scanned image output: 0: Interlaced image (I) 1: Progressive image (P)
O_rate	O	3	Rate output: 0: Reserved 1: HD-SDI 2: 3G-SDI 3-7: Reserved
O_mfactor	O	1	Rate factor: 0: m = standard rate/1 1: m = standard rate/1.001
O_hres	O	16	Horizontal resolution output
O_vres	O	16	Vertical resolution output
O_hcnt	O	16	Horizontal count output
O_vcnt	O	16	Vertical count output
O_f	O	1	Video field output (odd/even)
O_v	O	1	Video VS (vertical sync) output
O_h	O	1	Video HS (horizontal sync) output
O_de	O	1	Video DE (data enable) output
O_data	O	20	Video data output
O_audio_g1_de	O	1	Audio DE output, 48 KHz.
O_audio_g1_data	O	96	Audio data output
O_level_b_ds_clk	O	1	Level B DS receive clock output
O_level_b_ds_interlace_trans	O	1	Transmission mode output: 0: Interlaced transmission (I) 1: Progressive transmission (P)
O_level_b_ds_interlace	O	1	Level B DS transmission type: 0: Interlaced (I) 1: Progressive (P)
O_level_b_ds_rate	O	3	Level B DS rate output: 0: Reserved 1: HD-SDI 2: 3G-SDI 3-7: Reserved
O_level_b_ds_mfactor	O	1	Rate factor: 0: m = standard rate/1

Signal Name	Direction	Width	Description
			1: m = standard rate/1.001
O_level_b_ds_hres	O	16	Level B DS horizontal resolution output
O_level_b_ds_vres	O	16	Level B DS vertical resolution output
O_level_b_ds_hcnt	O	16	Level B DS horizontal count output
O_level_b_ds_vcnc	O	16	Level B DS horizontal count output
O_level_b_ds_f	O	1	Level B DS video field output (odd/even)
O_level_b_ds_v	O	1	Level B DS video VS (vertical sync) output
O_level_b_ds_h	O	1	Level B DS video HS (horizontal sync) output
O_level_b_ds_de	O	1	Level B DS video DE (data enable) output
O_level_b_ds_data	O	40	Level B DS video data output
O_level_b_ds_audio_g1_de	O	1	Level B DS audio DE output, 48 KHz.
O_level_b_ds_audio_g1_data	O	96	Level B DS audio data output

3.5 Timing Description

The timing diagram of Gowin SDI Decoder IP is shown in Figure 3-3. This diagram illustrates the interface timing after the data is output from Gowin SDI PHY IP and decoded by Gowin SDI Decoder IP. The signal descriptions are provided in Table 3-2.

Figure 3-3 Timing Diagram of Video Output Interface



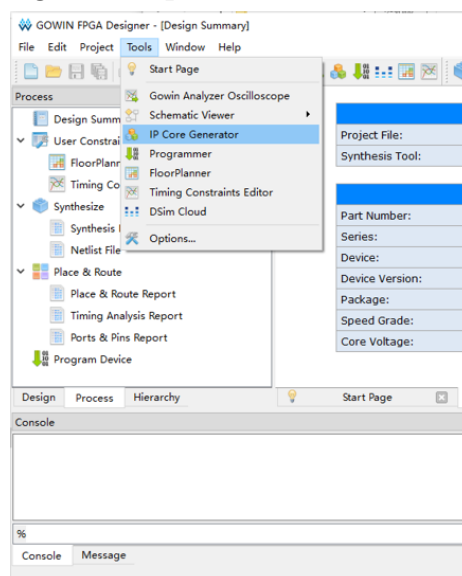
4 Interface Configuration

You can use IP core generator tool in Gowin Software to call and configure Gowin SDI Decoder IP.

1. Open IP Core Generator

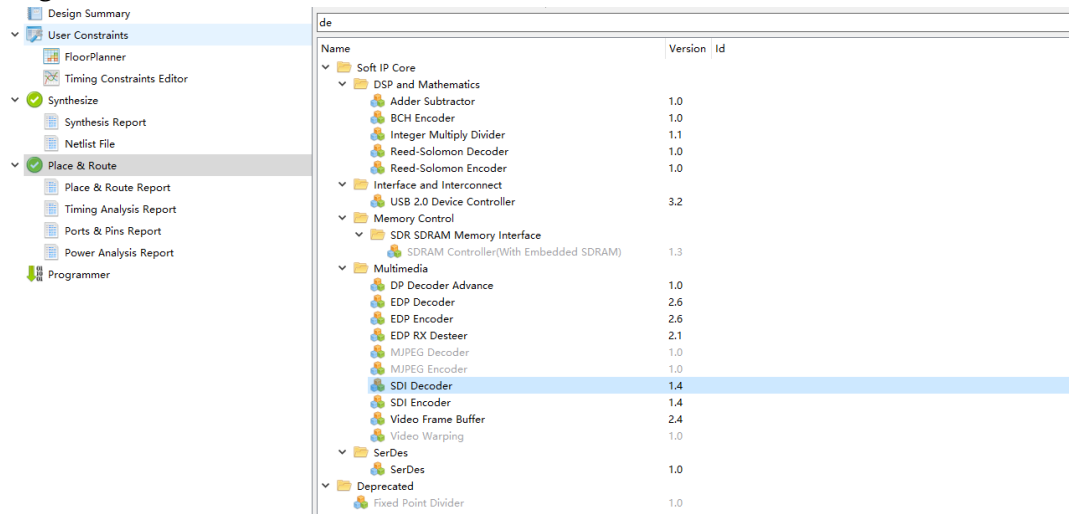
After creating the project, click the "Tools" tab in the upper left, click "IP Core Generator" from the drop-down list to open Gowin IP Core Generator, as shown in Figure 4-1.

Figure 4-1 Open IP Core Generator



2. Select SDI Decoder IP.

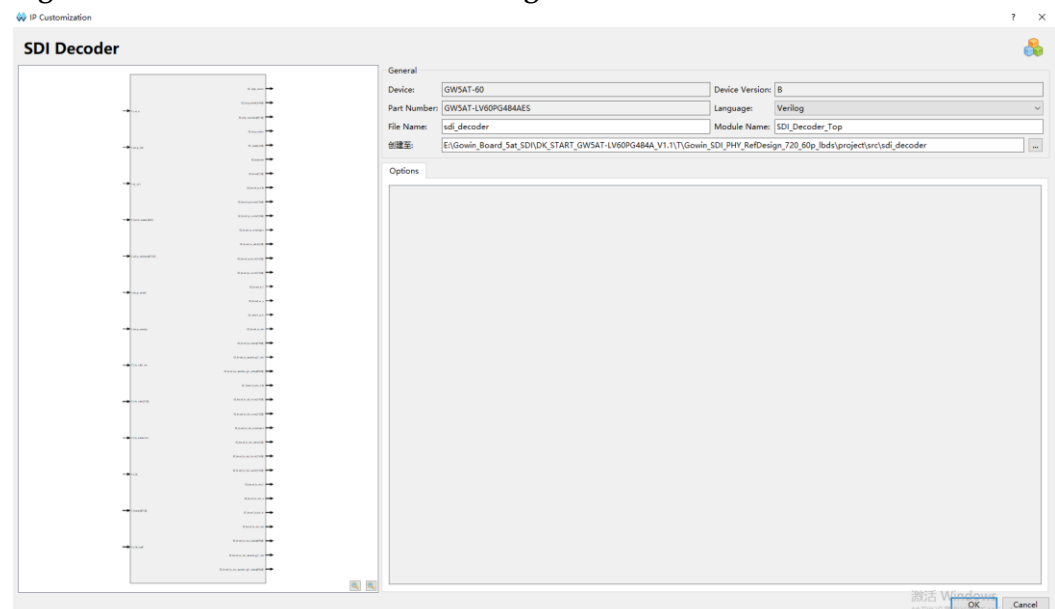
Double Click "Multimedia" and select SDI Decoder to open SDI Decoder IP configuration interface, as shown in Figure 4-2.

Figure 4-2 Select SDI Decoder IP

3. Gowin SDI Decoder IP configuration interface is as shown in Figure 4-3.

First configure "General" tab in the SDI Decoder IP interface.

- Device, Device Version, Part Number: Part number settings, determined by the current project, and the user can not configure it.
- Language: Supports Verilog and VHDL; choose the language as requirements, and the default is Verilog.
- File Name, Module Name, Create In: Displays SerDes file name, module name and the generated file path.

Figure 4-3 Gowin SDI Decoder IP Configuration Interface

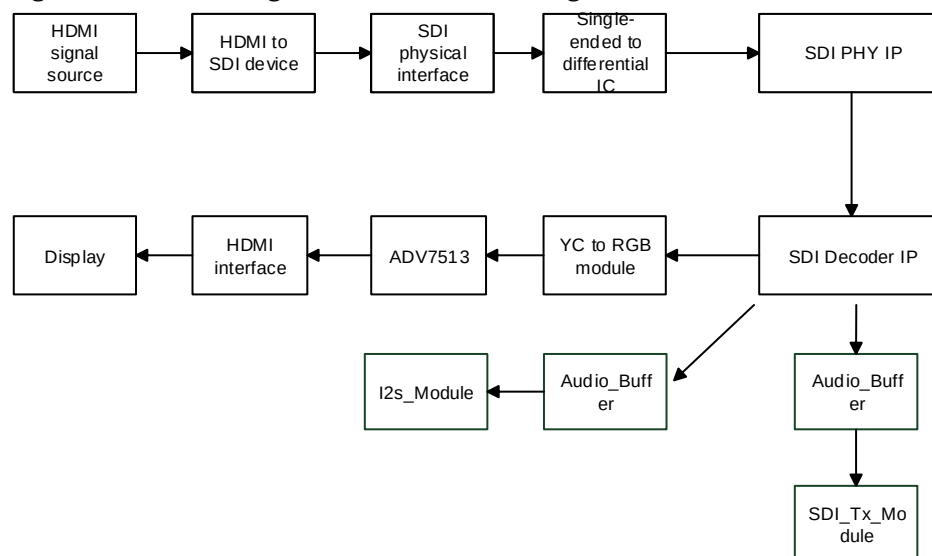
4. Click "OK" directly to generate the IP.

5 Reference Design

This chapter is intended to introduce the usage and structure of the [reference design](#) of Gowin SDI Decoder IP. Please see the SDI PHY IP Reference Design for details at Gowinsemi website.

This reference design takes DK_START_GW5AT-LV60PG484A_V1.1 development board as an example. For more information about DK_START_GW5AT-LV60PG484A_V1.1 development board, please refer to Gowinsemi website. The block diagram of reference design is shown in Figure 5-1.

Figure 5-1 Block Diagram of Reference Design



6 File Delivery

The file delivery for Gowin SDI Decoder IP includes the documentation, the design source code, and the reference design.

6.1 Documentation

Table 6-1 Document List

Name	Description
IPUG1024, Gowin SDI Encoder IP User Guide	Gowin SDI Decoder IP User Guide, i.e., this manual.

6.2 Design Source Code (Encryption)

The encrypted code folder contains encrypted RTL code for Gowin SDI Decoder IP. This code is intended for use with GUI to generate the IP core as needed.

Table 6-2 File List of Gowin SDI Decoder IP

Name	Description
sdi_decoder.v	SDI Decoder IP File, encrypted.

6.3 Reference Design

The RefDesign folder contains the netlist files, user reference designs, constraints files, top-level files, and project files for Gowin SDI PHY IP, Gowin SDI Encoder IP, and Gowin SDI Decoder IP.

Table 6-3 Gowin SDI Decoder IP RefDesign Folder Content List

Name	Description
video_top.v	The top module of reference design
testpattern.v	Test pattern generation module
dk_video.cst	Project physical constraints file
dk_video.sdc	Project timing constraints file
key_debounceN.v	Key debouncing
adv7513_iic_init.v	adv7513 configuration file
yc_to_rgb	yc_to_rgb folder
rgb_to_yc	rgb_to_yc folder
i2c_master	I2c_master folder, encrypted.

Name	Description
sdi_decoder	sdi_decoder folder, encrypted.
sdi_encoder	sdi_decoder folder, encrypted.
serdes	SerDes project folder, encrypted.
gowin_pll	gowin_pll folder
sdi_audio_buffer_pro	sdi_audio_buffer_pro folder
i2s_interface	i2s_interface folder

