



Gowin FP Exponential IP User Guide

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Revision History

Date	Version	Description
03/07/2025	1.0	Initial version published.

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1 About This Guide

1.1 Purpose

The purpose of Gowin FP Exponential IP User Guide is to help you learn the features and usage of Gowin FP Exponential IP by providing the descriptions of functions, ports, timing, GUI and reference design, etc. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.11. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [DS971, GW2AN-18X & 9X Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1118, GW5ART series of FPGA Products Data Sheet](#)

- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in [Table 1-1](#).

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
ALU	Arithmetic Logical Unit
FP	Floating Point
FPGAs	Field Programmable Gate Array
IP	Intellectual Property
LUT	Look-up Table
Register	Register

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

Gowin FP Exponential IP is designed to perform the exponential function for single-precision floating-point numbers with less logic resource utilization.

Table 2-1 Gowin FP Exponential IP Overview

Gowin FP Exponential IP	
Logic Resource	Please refer to Table 3-1
Delivered Doc.	
Design Files	Verilog
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.11 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

3 Features and Performance

3.1 Features

- Implements the exponential function for single-precision floating-point numbers.
- Supports NaN, zero, overflow, and underflow on the output ports.

3.2 Max. Frequency

The max. frequency of Gowin FP Exponential IP is mainly determined by speed grade of the selected devices.

3.3 Latency

The latency of Gowin FP Exponential IP is determined by the configuration parameters.

3.4 Resource Utilization

Gowin FP Exponential IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW5A-25 series of FPGA as an example, the resource utilization is shown in [Table 3-1](#). For application verification on other Gowin FPGA, please stay tuned for updates in future releases.

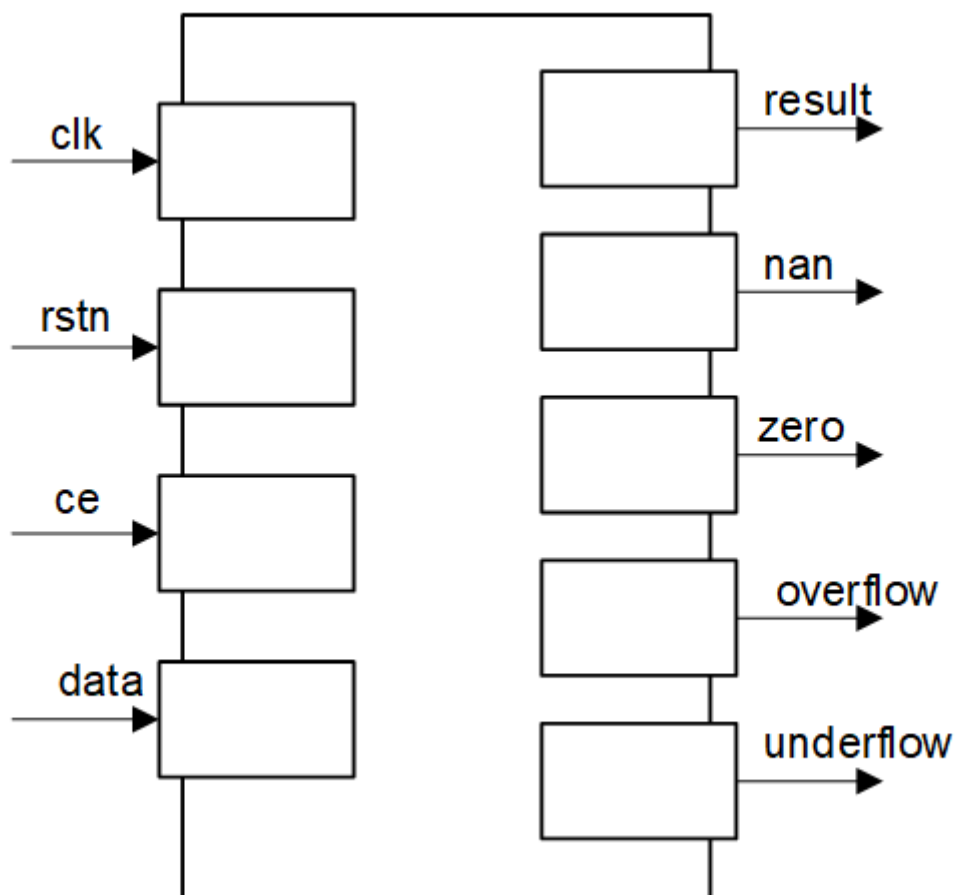
Table 3-1 Resource Utilization

Device	Speed Grade	Resource Name	Resource Utilization
GW5A-25	ES	LUTs	1176
		ALUs	1452
		Registers	1972
		I/O Buf	71

4 Functional Description

Gowin FP Exponential IP is designed to provide users with the capability to perform exponential function calculations on single-precision floating-point numbers, outputting the exponential result along with NaN, zero, overflow, and underflow. Users can configure parameters as needed when generating this module, and the block diagram is as shown in [Figure 4-1](#).

Figure 4-1 Implementation Diagram of Gowin FP Exponential IP



5 Port Description

The IO port of Gowin FP Exponential IP is shown in [Table 5-1](#).

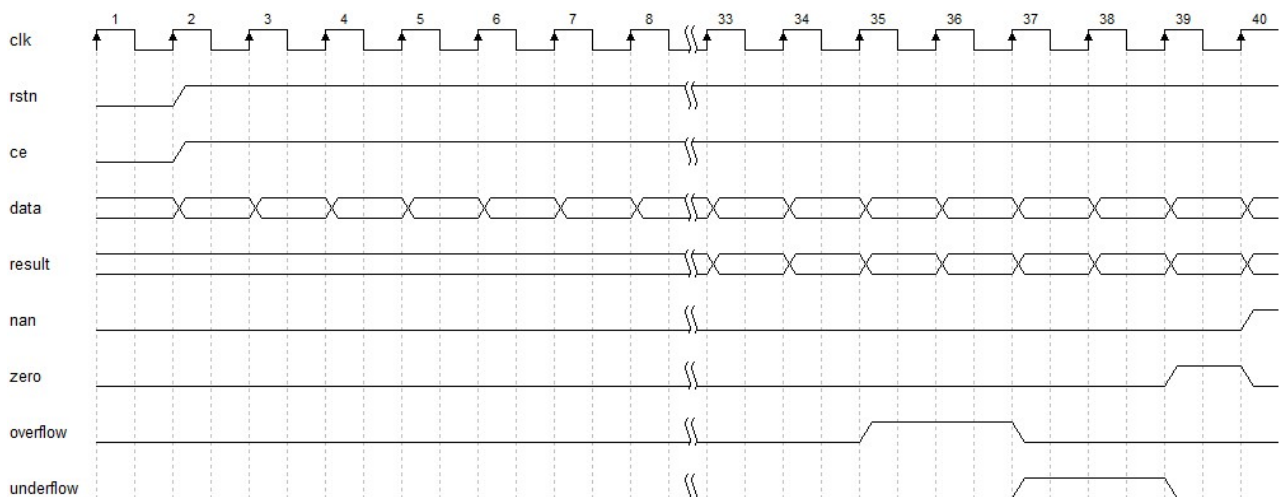
Table 5-1 IO List of Gowin FP Exponential IP

Name	I/O	Data Width	Description
clk	I	1	Input clock signal
rstn	I	1	Reset signal, active-low
ce	I	1	Clock enable signal, active-high
data	I	32	Input signal
result	O	32	Output result
nan	O	1	NaN
zero	O	1	Zero
overflow	O	1	Overflow
underflow	O	1	Underflow

6 Timing Description

This chapter describes the timing of Gowin FP Exponential IP. The signal timing of Gowin FP Exponential IP is as shown in [Figure 6-1](#).

Figure 6-1 Gowin FP Exponential IP Signal Timing



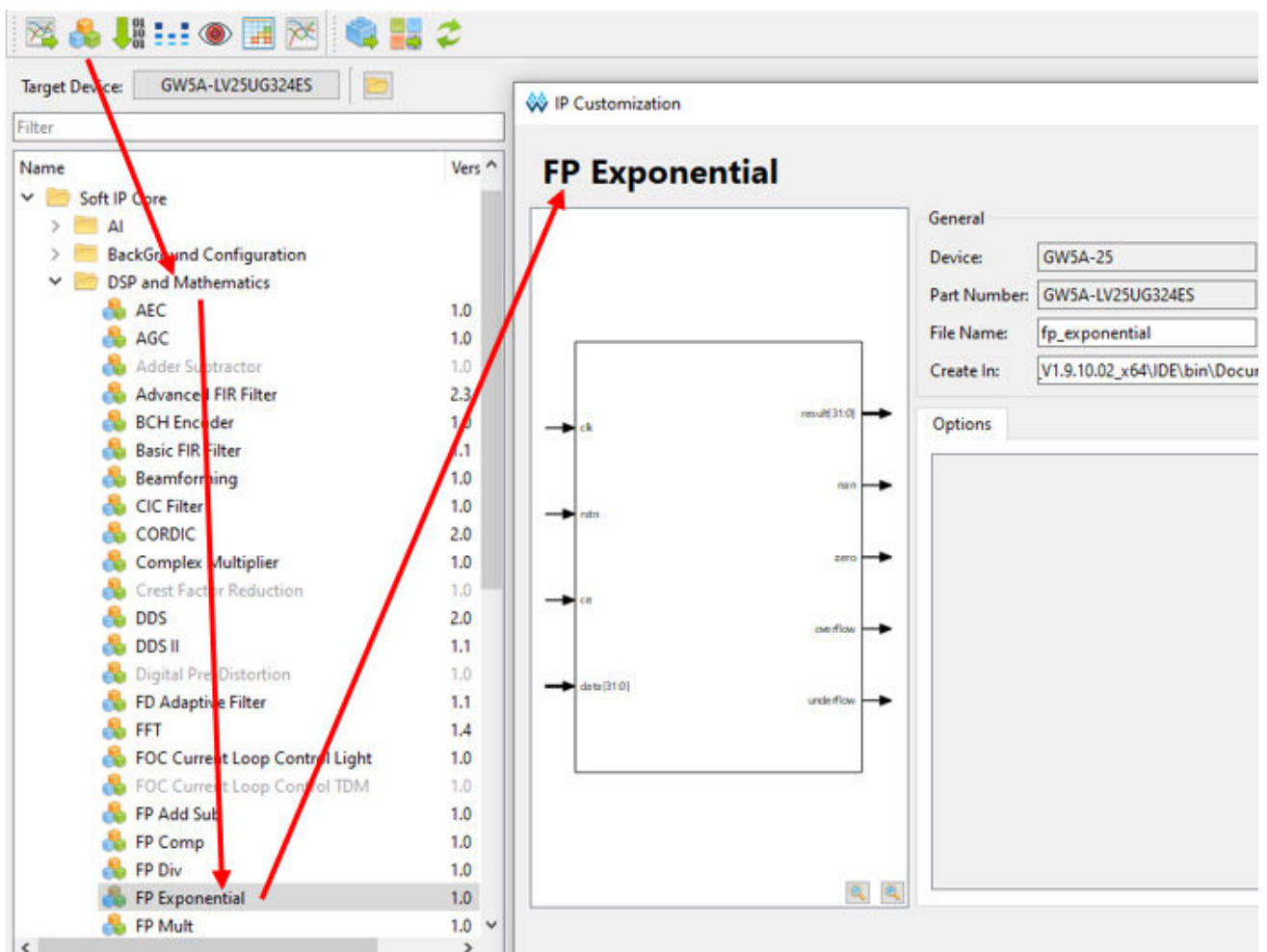
As shown in the figure above, after inputting the first single-precision floating-point data, the exponential output result, along with NaN, zero, and overflow, is obtained after 31 clock cycles.

7 GUI Configuration

7.1 Instructions for Calling IP

Click "Tools > IP Core Generator > DSP and Mathematics" to call and configure FP Exponential; toolbar icon is also available to open the IP as shown in [Figure 7-1](#).

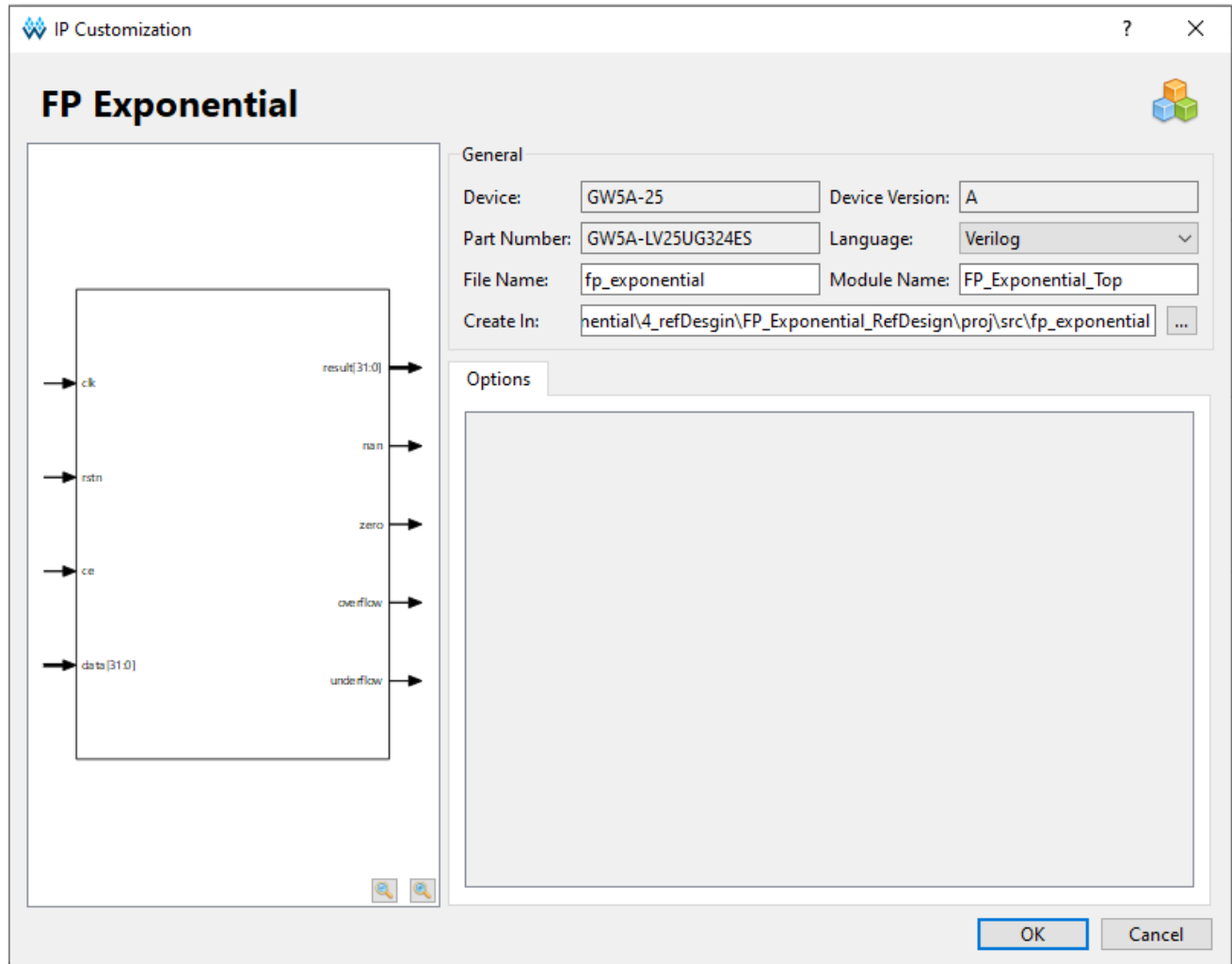
Figure 7-1 Open the IP via Toolbar Icon



7.2 Configuration Interface

The FP Exponential configuration interface is shown in [Figure 7-2](#).

Figure 7-2 FP Exponential Configuration Interface



This manual takes GW5A-25 device and GW5A-LV25UG324ES part number as an example.

- You can configure the path of generated IP core folder in the "Create In" text box.
- You can configure the generated IP file name in the "File Name" text box.
- You can configure the generated IP module name in the "Module Name" text box.

8 Reference Design

Please refer to the related test cases in Gowin FP Exponential IP [RefDesign](#).

9 Documents Delivered

The delivery file of Gowin FP Exponential IP includes documentation and reference design.

9.1 Document

The folder contains the user guide in PDF version.

Table 9-1 Gowin FP Exponential IP Doc. List

Name	Description
IPUG1199, Gowin FP Exponential IP User Guide	Gowin FP Exponential IP User Guide, namely this one.

9.2 Design Source Code (Encryption)

The encrypted code file contains the RTL encrypted code of Gowin FP Exponential IP for use with the GUI in order to cooperate with Gowin Software to generate the IP core required by users.

Table 9-2 Gowin FP Exponential IP Design Source Code List

Name	Description
fp_exponential.v	The top-level file of the IP core, which provides users with interface information, encrypted.

9.3 Reference Design

The Ref. Design folder contains the netlist file for Gowin FP Exponential IP, user reference design, constraints file, top-level file and the project file, etc.

Table 9-3 Gowin FP Exponential IP RefDesign Folder Content List

Name	Description
top.v	The top module of reference design

Name	Description
fp_exponential.cst	Project physical constraints file
fp_exponential.sdc	Project timing constraints file
fp_exponential	FP Exponential IP project file
fp_exponential.v	Generates FP Exponential IP top-level file, encrypted.
fp_exponential.vo	Generate FP Exponential IP netlist file

