



DK_USB_GW5ART-LV15MG132P_V1.1

User Guide

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Revision History

Date	Version	Description
01/17/2025	1.0E	Initial version published.
03/13/2026	1.0.1E	The description of DDR3 in “2.1 Overview” optimized.

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1 About This Guide

1.1 Purpose

The DK_USB_GW5ART-LV15MG132P_V1.1 development board (hereinafter referred to as “the development board”) user guide consists of following three parts:

- A brief introduction to the features of the development board
- An introduction to the development board system architecture and hardware resources
- An introduction to the hardware circuits, functions and pin distribution

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- [DS1118, GW5ART series of FPGA Products Data Sheet](#)
- [UG1120, GW5ART-15 Pinout](#)
- [UG1233, GW5ART series of FPGA Products Package and Pinout User Guide](#)
- [UG720, Arora V 15K FPGA Products Programming and Configuration User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
HDMI	High Definition Multimedia Interface
JTAG	Joint Test Action Group
LDO	Low Dropout Regulator
MIPI	Mobile Industry Processor Interface
SDI	Serial Digital Interface
SMA	SubMiniature version A Connector
SPI	Serial Peripheral Interface

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

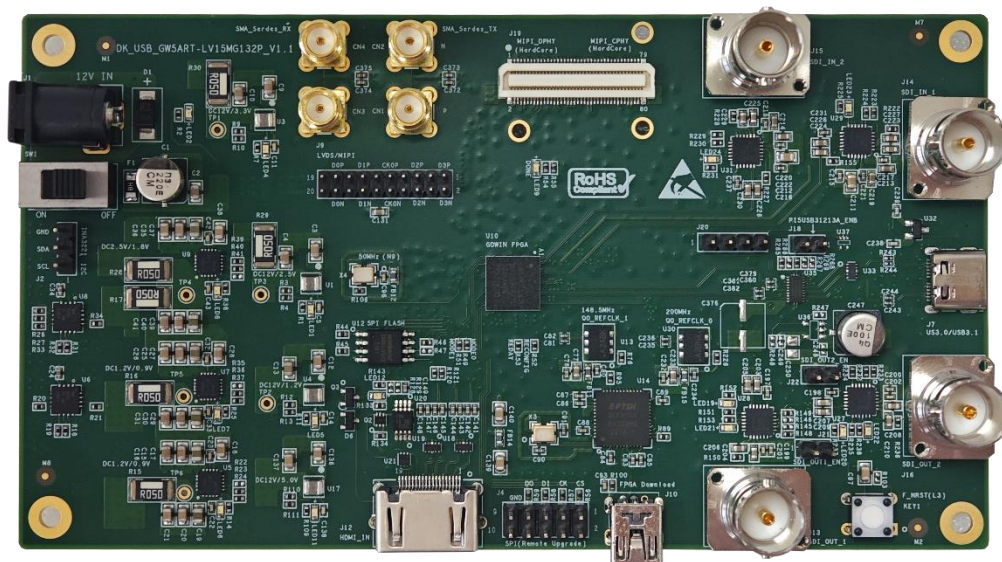
Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Development Board Introduction

2.1 Overview

Figure 2-1 DK_USB_GW5ART-LV15MG132P_V1.1 Development Board



Gowin GW5ART series of FPGA products are the 5 series products of Arora family, with abundant internal resources, high-performance DSP with a new architecture that supports AI operations, high-speed LVDS interface and abundant BSRAM resources. At the same time, it supports self-developed DDR3 and SerDes supporting multiple protocols and provides a variety of packages. It is suitable for applications such as low power, high performance, and compatibility design.

DK_USB_GW5ART-LV15MG132P_V1.1 development board applies to MIPI high-speed communication and SDI video communication, integrates Type-C, MIPI, and SDI interfaces, supporting FPGA's MIPI C-PHY, MIPI D-PHY, USB 3.0, and SDI function evaluation, hardware

verification, and software learning and debugging, etc.

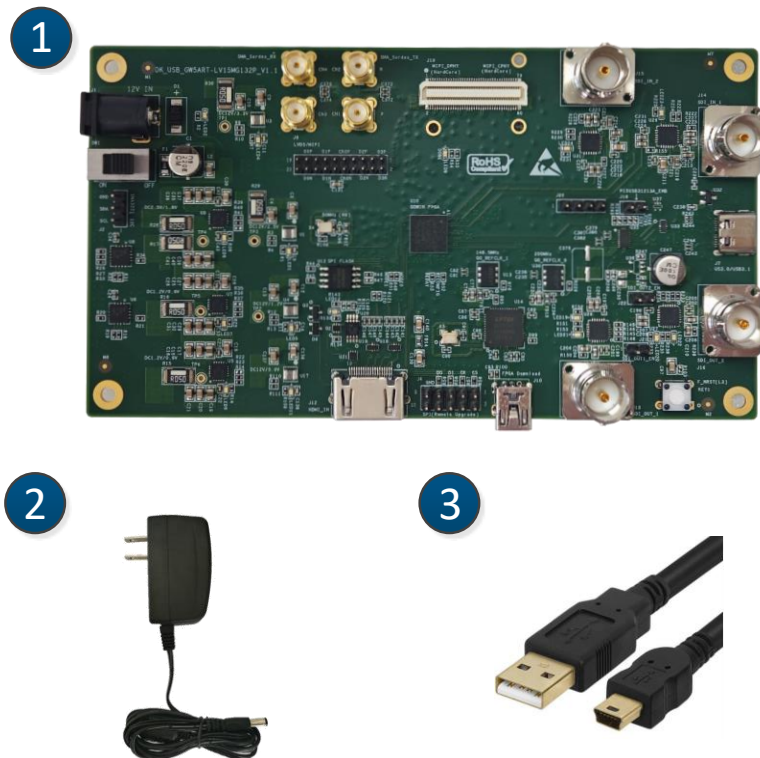
The development board adopts Gowin GW5ART-LV15MG132P FPGA device. For the internal resources of the chip, see [DS1118, GW5ART series of FPGA Products Data Sheet](#).

2.2 A Development Board Kit

The development board kit includes the following items:

1. DK_USB_GW5ART-LV15MG132P_V1.1 development board
2. 12V power (Input: AC 100-240V~50/60Hz 0.6A, output: DC12V 2A)
3. Mini USB-B download cable

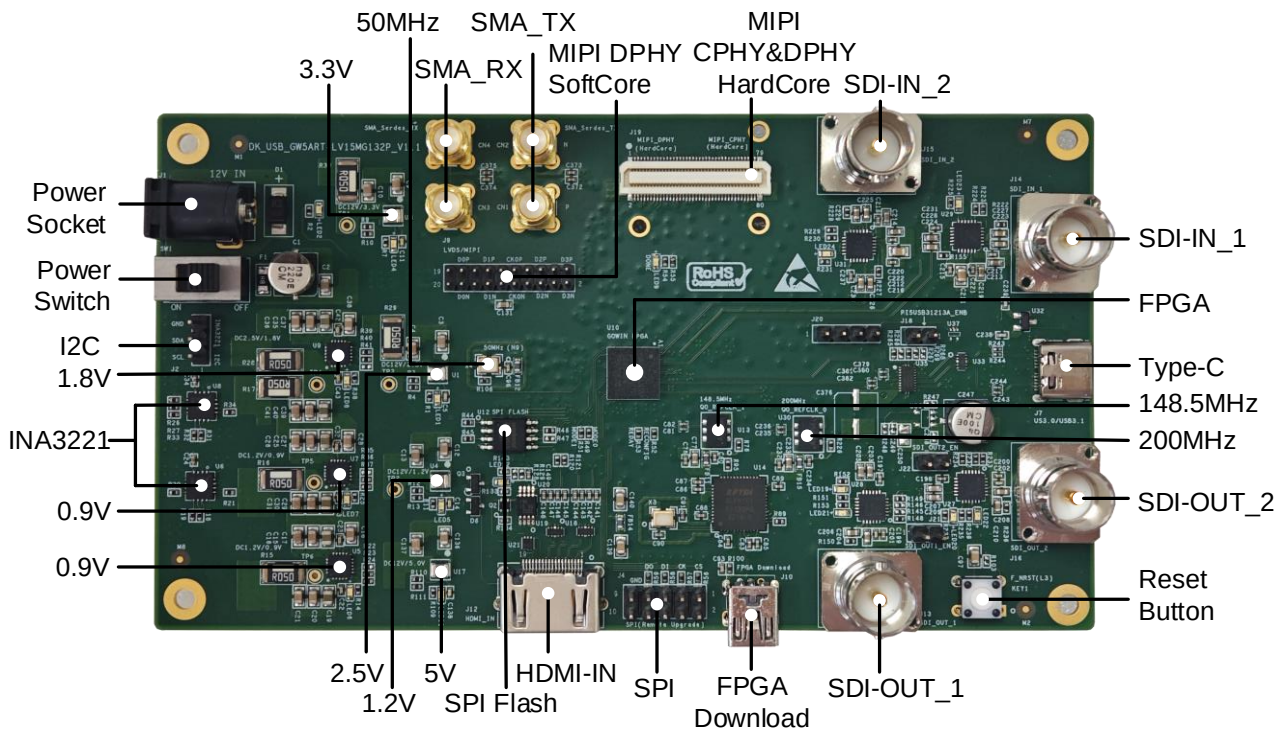
Figure 2-2 A Development Board Kit



- ① DK_USB_GW5ART-LV15MG132P_V1.1 development board
- ② 12V power supply adapter
- ③ Mini USB-B Cable

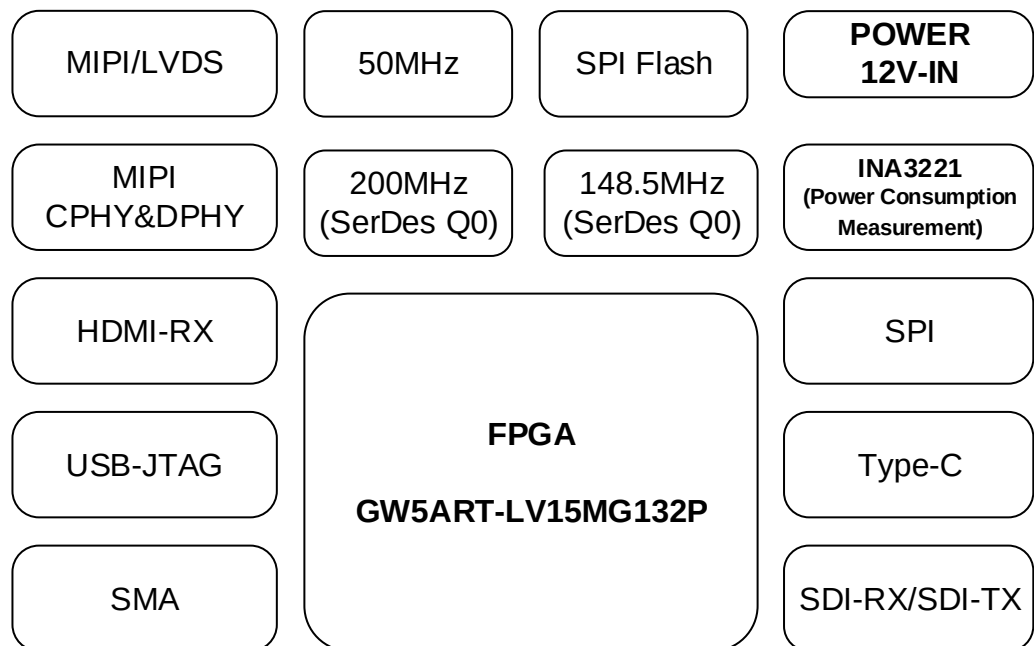
2.3 PCB Components

Figure 2-3 PCB Components



2.4 System Block Diagram

Figure 2-4 System Block Diagram



2.5 Features

The key features are as follows:

- **FPGA Device**
 - Gowin GW5ART-LV15MG132P FPGA
- **Download and Boot**
 - Integrate USB download circuit on the development board, download through Mini USB-B interface
 - External SPI Flash for storing FPGA configuration file
- **Power**
 - External DC 12V 2A Power
 - The Power light is on after power on.
 - The board generates 5V, 3.3V, 2.5V, 1.8V, 1.2V, 0.9V power.
- **Clock System**
 - 50MHz clock
 - 148.5 MHz SerDes clock
 - 200 MHz SerDes clock
- **Memory Device**
 - 64Mbit NOR Flash
- **SDI Interface**
 - Two SDI-TX interfaces
 - Two SDI-RX interfaces
 - 3G SDI interface, supporting 2.97Gbps SDI data transfer
- **Type-C Interface**
 - Support USB 3.0 protocol
- **MIPI Interface**
 - One CPHY hard core interface, including 3 lanes
 - One DPHY hard core interface, including 4 lanes (data) + 1 lane (clk)
 - One DPHY soft core interface with dual channels, each channel including 4 lanes (data) + 1 lane (clk), can also be used for LVDS receiving.
- **HDMI Interface**
 - One HDMI-RX interface
- **SPI Interface**
 - One SPI interface
 - Support remote upgrades
- **SMA Interface**
 - Four SMA interfaces

- Lead out 1-lane SerDes signal
- I2C Interface
 - One I2C interface
- Key
 - 1 low-level reset key

3 Development Board Circuit

3.1 FPGA

3.1.1 Overview

For the resources of GW5ART series of FPGA Products, refer to [*DS1118, GW5ART series of FPGA Products Data Sheet*](#).

3.1.2 I/O BANK Introduction

For the I/O BANK, package, and pinout information, see [*UG1233, GW5ART series of FPGA Products Package and Pinout User Guide*](#) for more details.

3.2 Power Supply

3.2.1 Introduction

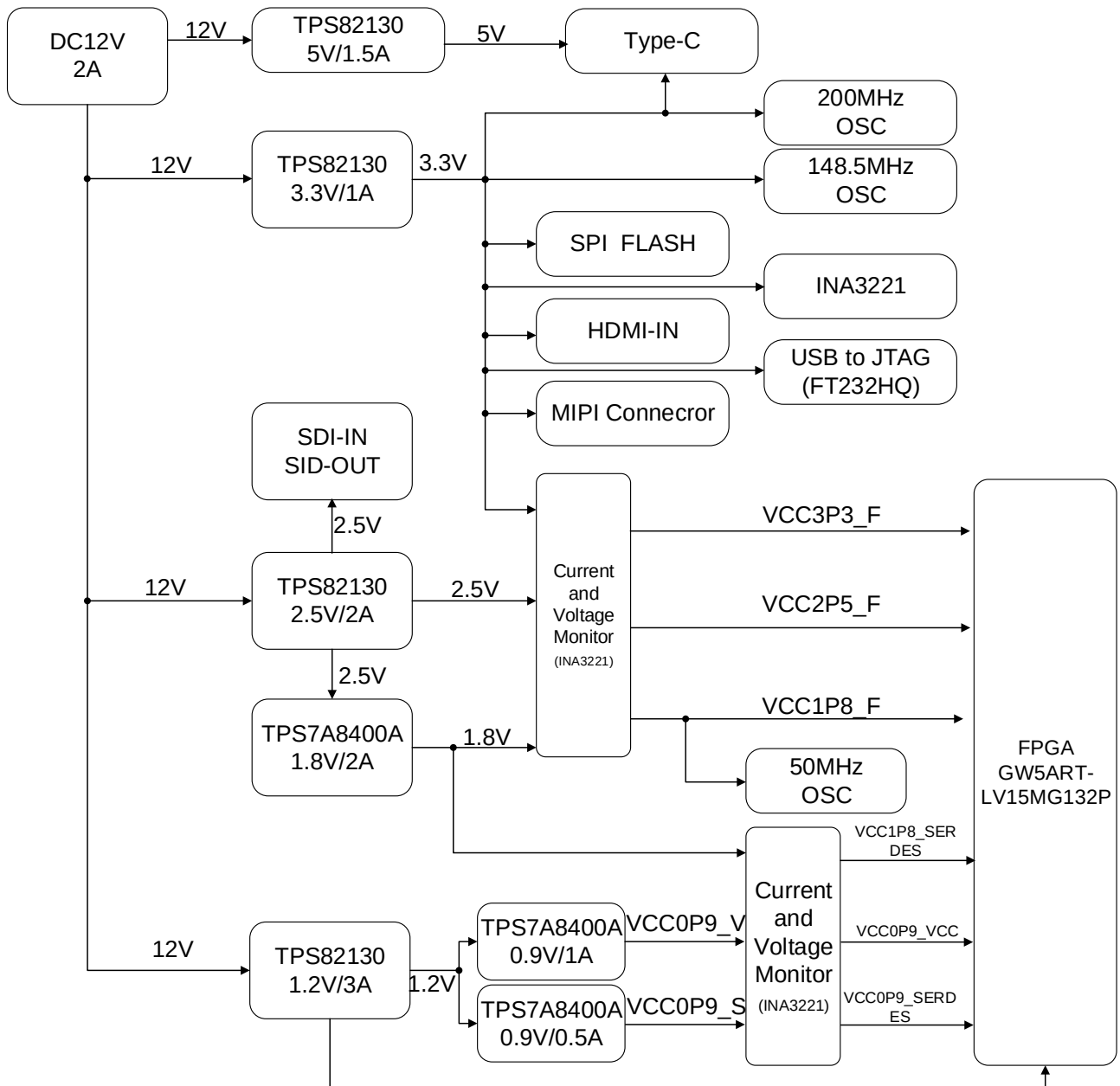
The development board needs to be powered by a 12V power adapter.

The input parameter of the adapter is AC 100-240V~50/60MHz 0.6A, and the output parameter is DC 12V 2A.

The input 12V power is regulated by the PMIC on the development board to generate 5.0V, 3.3V, 2.5V, 1.8V, 1.2V, and 0.9V power supplies.

3.2.2 Power Distribution

Figure 3-1 Power Distribution Diagram



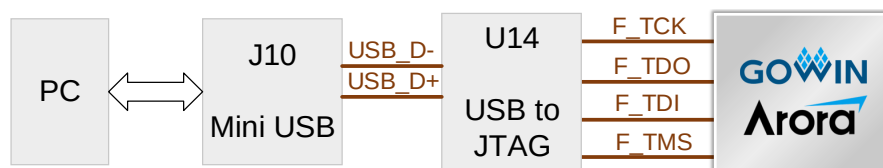
3.3 Download Module

3.3.1 Introduction

The development board includes a Mini USB-B download port (J10) designed to program the programs to external SPI FLASH or SRAM.

The download connection diagram is show in Figure 3-2.

Figure 3-2 Connection Diagram of Download



3.3.2 Pin Distribution

Table 3-1 JTAG Pin Distribution

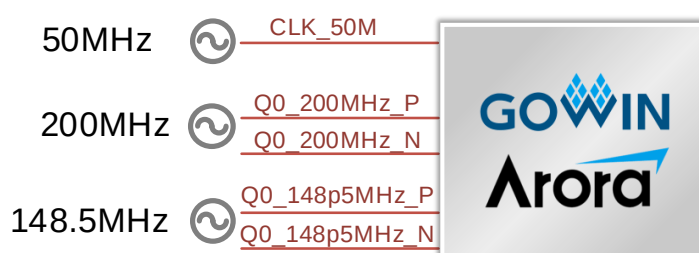
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_TCK	G2	4	3.3V	JTAG signal
F_TDO	J2	4	3.3V	
F_TDI	J3	4	3.3V	
F_TMS	G3	4	3.3V	

3.4 Clock

3.4.1 Introduction

The development board includes multiple FPGA clock sources, including one 50 MHz single-ended clock, one 200 MHz SerDes differential clock, and one 148.5 MHz SerDes differential clock. The 200 MHz and 148.5 MHz clocks are connected to the FPGA's SerDes clock pin. The clock pin distribution is shown in Figure 3-3.

Figure 3-3 Clock Connection Diagram



3.4.2 Pin Distribution

Table 3-2 Clock Pin Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
CLK_50M	N9	1	1.8V	50 MHz single-ended clock
Q0_200MHz_P	A8	Q0	-	200 MHz differential clock
Q0_200MHz_N	A7	Q0	-	200 MHz differential clock
Q0_148p5MHz_P	C10	Q0	-	148.5 MHz differential clock
Q0_148p5MHz_N	B10	Q0	-	148.5 MHz differential clock

3.5 I2C Interface

3.5.1 Introduction

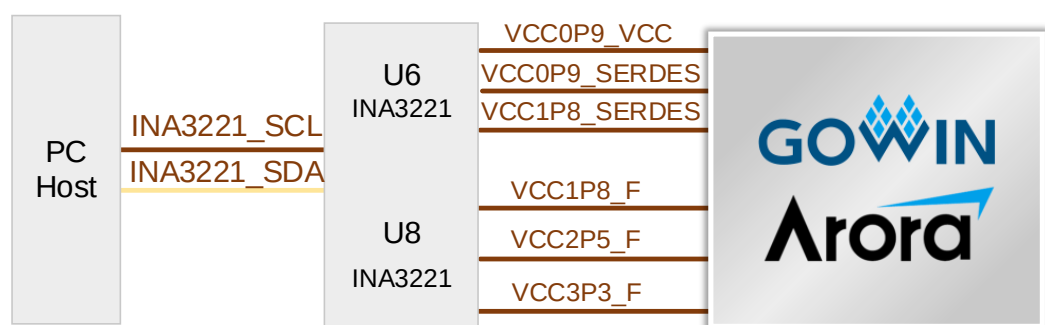
The development board includes one I2C interface as the host communication interface. The host can monitor the power consumption of FPGA VCC, SerDes, and BANK through this interface.

The first channel of U6 is VCC0P9_VCC; the second is VCC0P9_SERDES; and the third is VCC1P8_SERDES. The I2C address is 0x40.

The first channel of U8 is VCC1P8_F; the second channel is VCC2P5_F; the third channel is VCC3P3_F; the I2C address is 0x41.

The connection diagram of I2C interface is shown in Figure 3-4.

Figure 3-4 Connection Diagram of I2C Interface



3.5.2 Pin Distribution

Table 3-3 Pin Distribution of I2C Interface

J2 Pin No.	Signal Name	I/O Level	Description
1	INA3221_SCL	3.3V	Serial bus clock line
2	INA3221_SDA	3.3V	Serial bus data line
3	GND	-	GND

3.6 MIPI Interface

3.6.1 Introduction

The development board provides one MIPI CPHY hard core interface, one MIPI DPHY hard core interface, and one MIPI DPHY soft core interface from the FPGA. The MIPI CPHY hard core interface and MIPI DPHY hard core interface are led to 80P AXK580147YG connectors with 0.5 mm pitch. The MIPI DPHY soft core interface is led to one 2*10P pin header with 2.0 mm pitch. The MIPI DPHY soft core interfaces can be used for LVDS receiving. The connection diagram of MIPI is as follows.

Figure 3-5 Connection Diagram of MIPI CPHY & DPHY Hard Core Interfaces

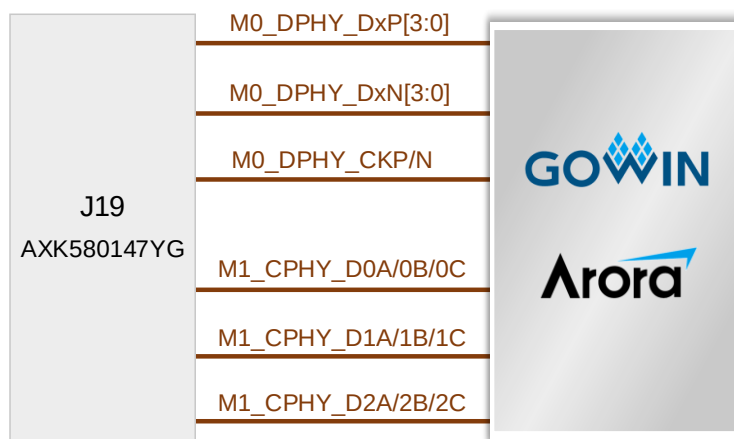


Figure 3-6 Connection Diagram of MIPI DPHY Soft Core/LVDS Interface



3.6.2 Pin Distribution

Table 3-4 Pin Distribution of MIPI CPHY & DPHY Hard core Interface

J19 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	M0_DPHY_D0N	P7	MIPI	-	MIPI DPHY data signal
2	VCC1P2	-	-	1.2V	Power
3	M0_DPHY_D0P	N7	MIPI	-	MIPI DPHY data signal
4	VCC1P2	-	-	1.2V	Power
5	GND	-	-	-	GND
6	GND	-	-	-	GND
7	M0_DPHY_D1N	P6	MIPI	-	MIPI DPHY data signal
8	GND	-	-	-	GND
9	M0_DPHY_D1P	N6	MIPI	-	MIPI DPHY data signal
10	GND	-	-	-	GND
11	GND	-	-	-	GND
12	NC	-	-	-	Floating
13	M0_DPHY_CKN	P5	MIPI	-	MIPI DPHY clock signal
14	NC	-	-	-	Floating
15	M0_DPHY_CKP	N5	MIPI	-	MIPI DPHY clock signal
16	GND	-	-	-	GND
17	GND	-	-	-	GND
18	GND	-	-	-	GND
19	M0_DPHY_D2N	P4	MIPI	-	MIPI DPHY data signal
20	GND	-	-	-	GND
21	M0_DPHY_D2P	N4	MIPI	-	MIPI DPHY data signal
22	NC	-	-	-	Floating
23	GND	-	-	-	GND
24	NC	-	-	-	Floating
25	M0_DPHY_D3N	P3	MIPI	-	MIPI DPHY data signal

J19 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
26	NC	-	-	-	Floating
27	M0_DPHY_D3P	N3	MIPI	-	MIPI DPHY data signal
28	GND	-	-	-	GND
29	GND	-	-	-	GND
30	GND	-	-	-	GND
31	GND	-	-	-	GND
32	NC	-	-	-	Floating
33	GND	-	-	-	GND
34	NC	-	-	-	Floating
35	GND	-	-	-	GND
36	GND	-	-	-	GND
37	GND	-	-	-	GND
38	GND	-	-	-	GND
39	GND	-	-	-	GND
40	GND	-	-	-	GND
41	M1_CPHY_D1A	L1	MIPI	-	MIPI CPHY data signal
42	NC	-	-	-	Floating
43	M1_CPHY_D1B	K1	MIPI	-	MIPI CPHY data signal
44	NC	-	-	-	Floating
45	M1_CPHY_D1C	J1	MIPI	-	MIPI CPHY data signal
46	GND	-	-	-	GND
47	GND	-	-	-	GND
48	GND	-	-	-	GND
49	GND	-	-	-	GND
50	GND	-	-	-	GND
51	M1_CPHY_D0A	F2	MIPI	-	MIPI CPHY data signal
52	NC	-	-	-	Floating
53	M1_CPHY_D0B	F1	MIPI	-	MIPI CPHY data signal
54	NC	-	-	-	Floating

J19 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
55	M1_CPHY_D0C	G1	MIPI	-	MIPI CPHY data signal
56	NC	-	-	-	Floating
57	GND	-	-	-	GND
58	NC	-	-	-	Floating
59	GND	-	-	-	GND
60	GND	-	-	-	GND
61	M1_CPHY_D2A	C1	MIPI	-	MIPI CPHY data signal
62	NC	-	-	-	Floating
63	M1_CPHY_D2B	D2	MIPI	-	MIPI CPHY data signal
64	NC	-	-	-	Floating
65	M1_CPHY_D2C	D1	MIPI	-	MIPI CPHY data signal
66	GND	-	-	-	GND
67	GND	-	-	-	GND
68	NC	-	-	-	Floating
69	GND	-	-	-	GND
70	NC	-	-	-	Floating
71	GND	-	-	-	GND
72	GND	-	-	-	GND
73	GND	-	-	-	GND
74	GND	-	-	-	GND
75	GND	-	-	-	GND
76	VCC3P3	-	-	3.3V	Power
77	GND	-	-	-	GND
78	VCC3P3	-	-	3.3V	Power
79	GND	-	-	-	GND
80	VCC3P3	-	-	3.3V	Power

Table 3-5 Pin Distribution of MIPI DPHY Soft Core/LVDS Interface

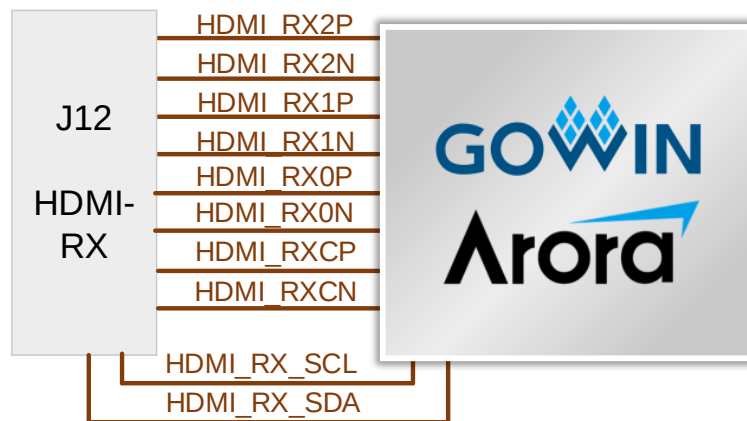
J9 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	DPHY_LVDS_D3P	N8	1	1.8V	MIPI/LVDS data
2	DPHY_LVDS_D3N	P8	1	1.8V	MIPI/LVDS data
3	GND	-	-	-	GND
4	GND	-	-	-	GND
5	DPHY_LVDS_D2P	P10	1	1.8V	MIPI/LVDS data
6	DPHY_LVDS_D2N	N10	1	1.8V	MIPI/LVDS data
7	GND	-	-	-	GND
8	GND	-	-	-	GND
9	DPHY_LVDS_CK0 P	N11	1	1.8V	MIPI/LVDS clock
10	DPHY_LVDS_CK0 N	P11	1	1.8V	MIPI/LVDS clock
11	GND	-	-	-	GND
12	GND	-	-	-	GND
13	DPHY_LVDS_D1P	N12	1	1.8V	MIPI/LVDS data
14	DPHY_LVDS_D1N	P12	1	1.8V	MIPI/LVDS data
15	GND	-	-	-	GND
16	GND	-	-	-	GND
17	DPHY_LVDS_D0P	P13	1	1.8V	MIPI/LVDS data
18	DPHY_LVDS_D0N	N13	1	1.8V	MIPI/LVDS data
19	GND	-	-	-	GND
20	GND	-	-	-	GND

3.7 HDMI Interface

3.7.1 Introduction

The development board provides an HDMI input interface, enabling HDMI signal reception through an internal FPGA IP. The interface connection diagram is shown in Figure 3-7.

Figure 3-7 Connection Diagram of HDMI-RX Interface



3.7.2 Pin Distribution

Table 3-6 Pin Distribution of HDMI-RX

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
HDMI_RXCP	M2	3	2.5V	HDMI differential clock
HDMI_RXCN	M1	3	2.5V	HDMI differential clock
HDMI_RX0P	P2	3	2.5V	HDMI receive data
HDMI_RX0N	P1	3	2.5V	HDMI receive data
HDMI_RX1P	H3	4	2.5V	HDMI receive data
HDMI_RX1N	H2	4	2.5V	HDMI receive data
HDMI_RX2P	K3	4	2.5V	HDMI receive data
HDMI_RX2N	K2	4	2.5V	HDMI receive data
HDMI_RX_SCL	N2	3	2.5V	I2C serial clock, multiplexed with the MODE1 pin
HDMI_RX_SDA	N1	3	2.5V	I2C serial clock, multiplexed with the MODE1 pin

3.8 SPI Interface

3.8.1 Introduction

The development board provides an SPI interface for remote upgrades. The connection diagram is shown in Figure 3-8.

Figure 3-8 Connection Diagram of SPI Interface



3.8.2 Pin Distribution

Table 3-7 Pin Distribution of SPI Interface

J4 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	SPI_CS	P14	1	1.8V	Chip select signal
3	SPI_CK	M8	1	1.8V	Clock signal
5	SPI_DI	N14	1	1.8V	Data input to FPGA
7	SPI_DO	P9	1	1.8V	Data output from FPGA

3.9 Type-C Interface

3.9.1 Introduction

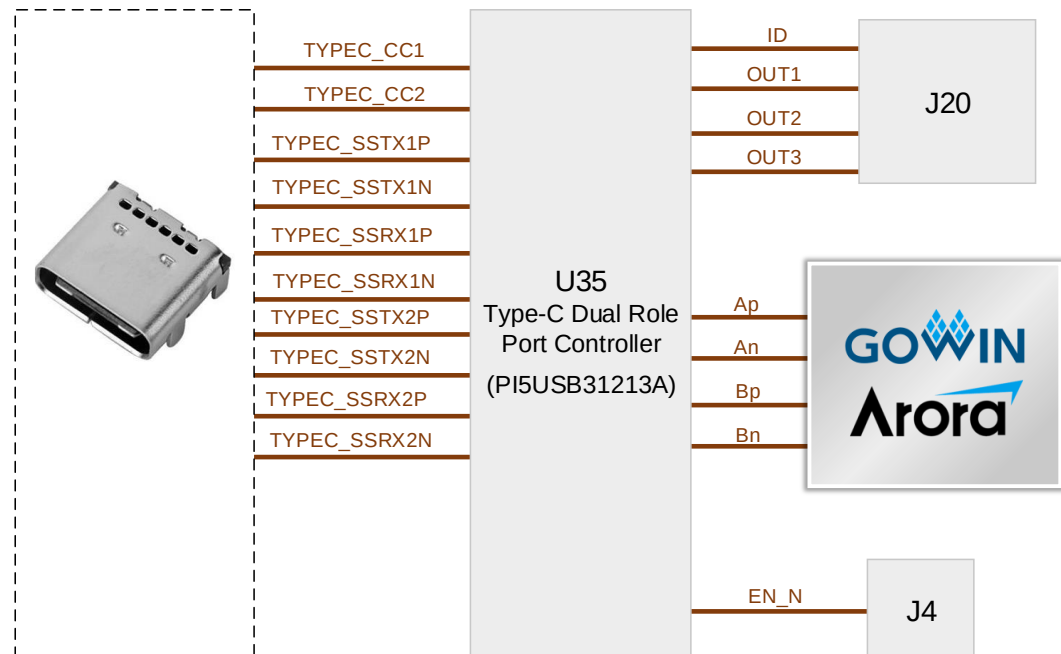
The development board provides a Type-C interface, supporting USB 3.0 data transmission, which can meet the requirements for USB 3.0 performance evaluation.

The Type-C interface on the development board connects a SerDes signal to the FPGA through a Type-C dual-role port controller, which handles the switching of high-speed differential lines. USB 3.0 is implemented using the Gowin USB 3.0 PHY IP solution.

The management interface of the Type-C dual-role port controller is led out via J20 and can be jumpered to the SPI interface (J4) to enable

data interaction between the FPGA and the Type-C dual-role port controller. The enable signal (EN_N) for the Type-C dual-role port controller is multiplexed with the SPI clock signal (SPI_CK).

Figure 3-9 Connection Diagram of Type-C Interface



3.9.2 Pin Distribution

Table 3-8 Pin Distribution of Type-C Interface

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
TYPEC_SSTXP	B8	SerDes Q0	-	Type-C TX+
TYPEC_SSTXN	C8	SerDes Q0	-	Type-C TX-
TYPEC_SSRXP	A10	SerDes Q0	-	Type-C RX+
TYPEC_SSRXN	A11	SerDes Q0	-	Type-C RX-

3.10 SDI Interface

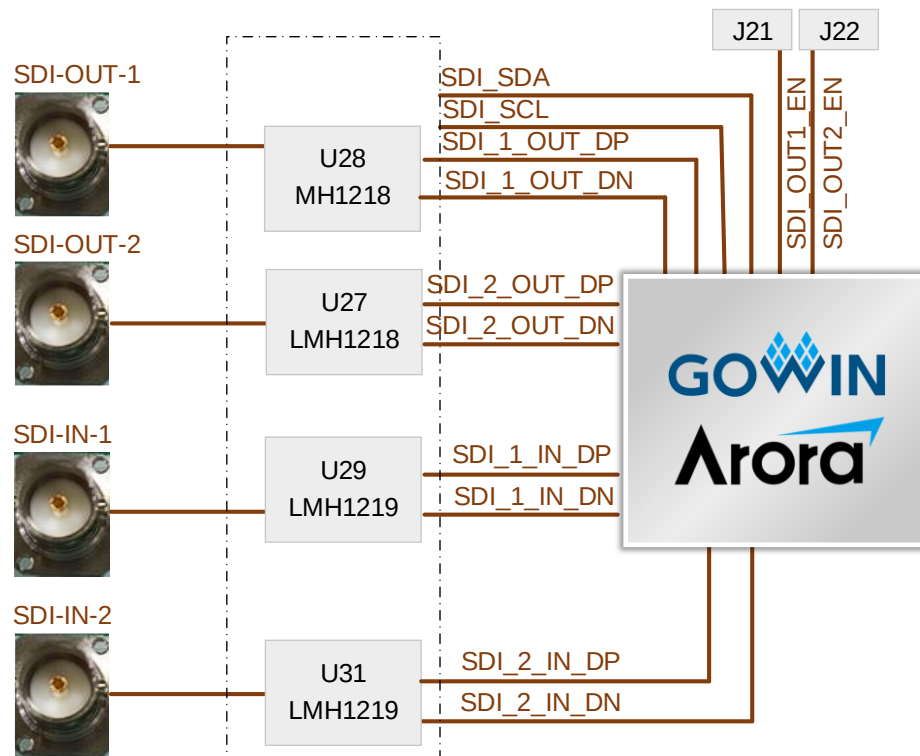
3.10.1 Introduction

The development board includes two SDI-IN interfaces and two SDI-OUT interfaces, and the interface connectors are BNC, which can meet the performance evaluation needs of the 3G SDI interfaces.

The output of the SDI-OUT-1 channel can be disabled by installing a jumper cap on J21, and the output of the SDI-OUT-2 channel can be disabled by installing a jumper cap on J22.

The connection diagram of SDI interface is shown in Figure 3-10.

Figure 3-10 Connection Diagram of SDI Interface



3.10.2 Pin Distribution

Table 3-9 Pin Distribution of SDI Interface

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
SDI_OUT1_EN	-	-	-	U28 (LMH1218) output enable
SDI_OUT2_EN	-	-	-	U27 (LMH1218) output enable
SDI_SDA	N14	3	2.5V	I2C control signal of LMH1218/LMH1219, SDA is multiplexed with the SPI_DO signal, and SCL is multiplexed with the SPI_DI signal, connected via jumper caps.
SDI_SCL	P9	2	2.5V	
SDI_2_OUT_P	B3	SerDes Q0	-	LMH1218 IN0+
SDI_2_OUT_N	C3	SerDes Q0	-	LMH1218 IN0-

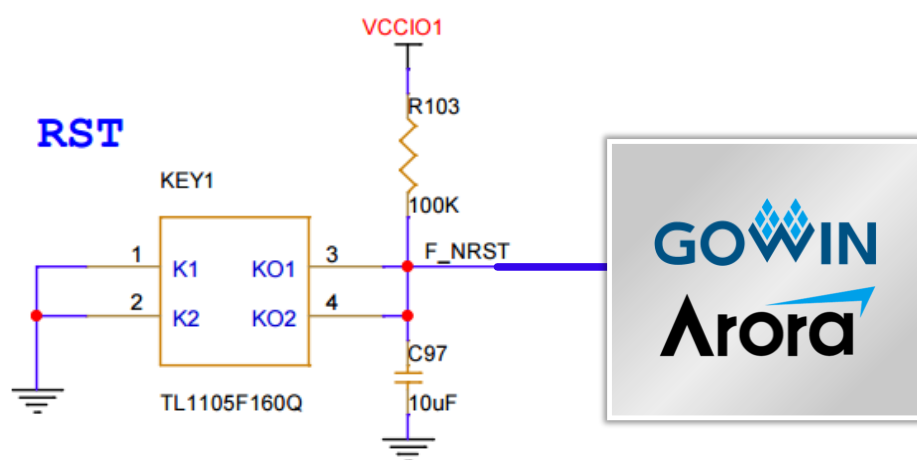
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
SDI_1_OUT_P	B6	SerDes Q0	-	LMH1218 IN0+
SDI_1_OUT_N	C6	SerDes Q0	-	LMH1218 IN0-
SDI_2_IN_P	A2	SerDes Q0	-	LMH1219 OUT0+
SDI_2_IN_N	A1	SerDes Q0	-	LMH1219 OUT0-
SDI_1_IN_P	A4	SerDes Q0	-	LMH1219 OUT0+
SDI_1_IN_N	A5	SerDes Q0	-	LMH1219 OUT0-

3.11 Key

3.11.1 Introduction

The development board includes one reset key, which is connected to the Done pin of FPGA BANK1. The corresponding IO input voltage of the FPGA is low when the key is pressed while high when the key is not pressed. The connection diagram is shown in Figure 3-11.

Figure 3-11 Connection Diagram of Key



3.11.2 Pin Distribution

Table 3-10 Pin Distribution of Key

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_NRST	L3	2	2.5V	The reset key is reused as the DONE pin.

3.12 SMA Interface

3.12.1 Introduction

The development board leads out two pairs of SMA differential signals, including transmitting signal and receiving signal, which are connected to FPGA SerDes pins. The connection diagram is shown in Figure 3-12.

Figure 3-12 Connection Diagram of SMA Interface



3.12.2 Pin Distribution

Table 3-11 Pin Distribution of SMA Interface

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
SMA_TXP	C12	SerDes Q0	--	FPGA transmit data
SMA_TXN	B12	SerDes Q0	--	FPGA transmit data
SMA_RXP	A13	SerDes Q0	--	FPGA receive data
SMA_RXN	A14	SerDes Q0	--	FPGA receive data

