

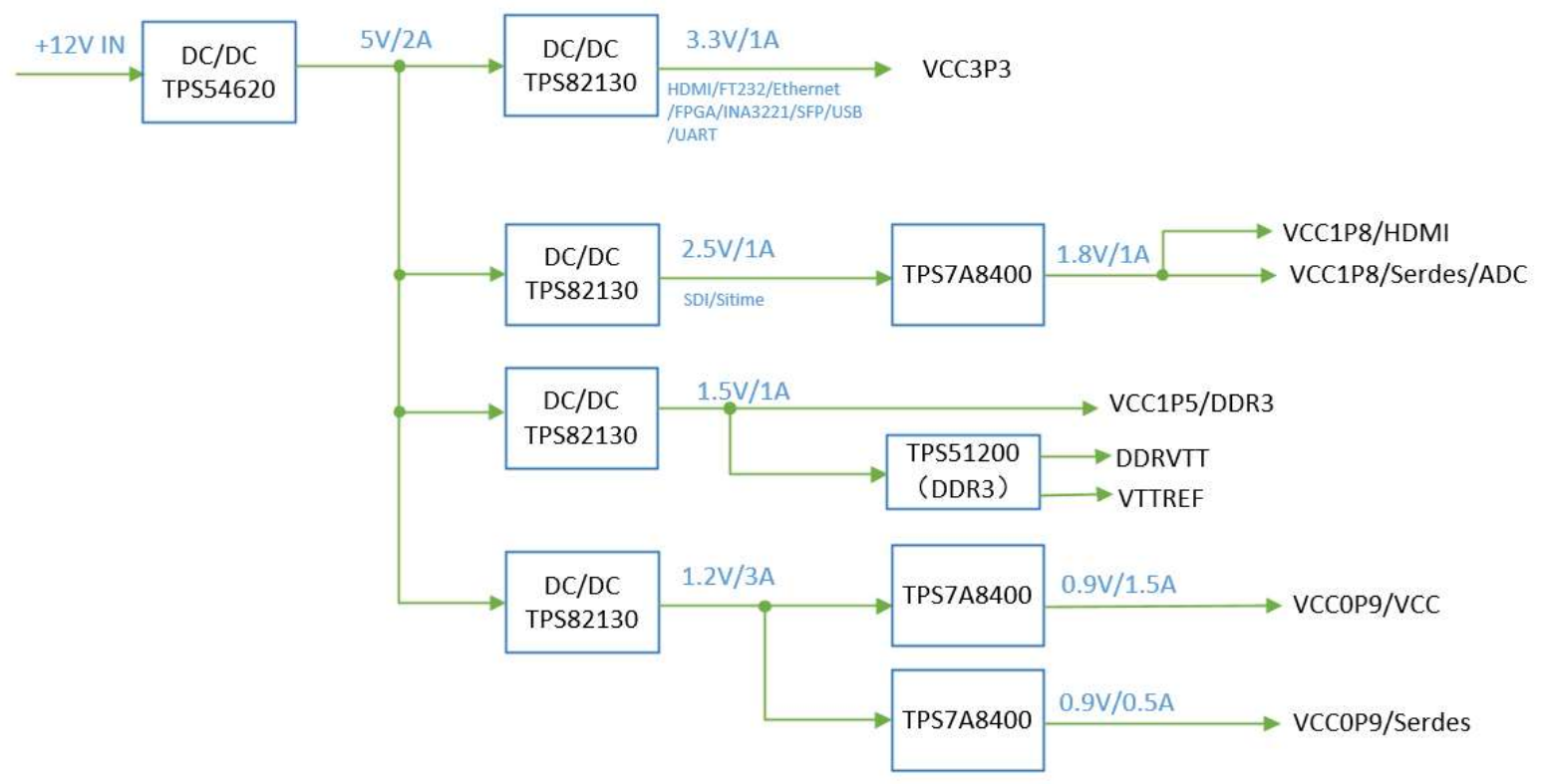
SCHEMATIC	CONTENT	PAGE
COVER PAGE	COVER PAGE	01
DIAGRAM	PCB DIAGRAM	02
POWER	VCC5P0,VCC3P3,VCC2P5,VCC1P8,VCC1P2,VCC1P5,VCC0P9	03~05
FPGA	FPGA	06~08
SFP	2*SFP	09
HDMI	HDMI-RX, HDMI-TX	10
SDI	SDI-IN,SDI-OUT	11
ETHERNET	2*ETHERNET PHY	12
DDR3	DDR3	13
OTHERS	MIPI, LVDS,USB-JTAG, UART	14

The diagram illustrates the functional blocks of the GW5AT-LV60PG484A FPGA board. At the center is the **FPGA GW5AT-LV60PG484A**. The board features a variety of interfaces and components:

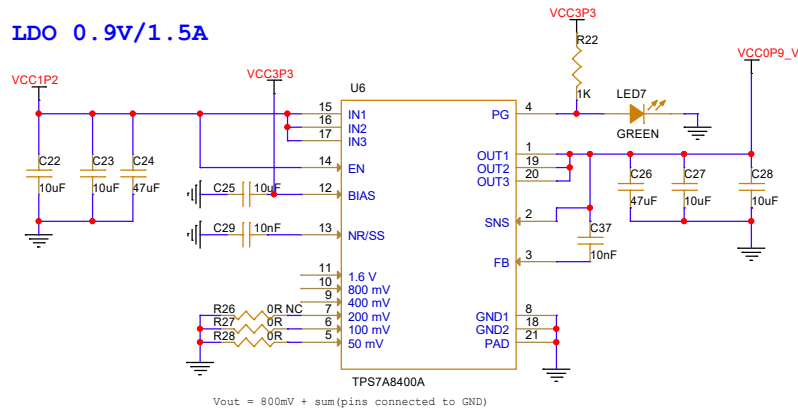
- Top Row:** GPIO, SPI FLASH, USB-JTAG, KEY&LED, and POWER 12V-IN.
- Second Row:** LVDS, 148.5MHz OSC (serdes), 125MHz OSC (serdes), 200MHz OSC, 50MHz OSC, and INA3221.
- Left Column:** Ethernet, HDMI-IN, HDMI-OUT, and UART.
- Right Column:** SFP, SFP, SDI-IN, SDI-OUT, and ADC.
- Bottom Row:** 2*DDR3 SDRAM and MIPI.

Title DK_START_GW5AT-LV60PG484A_V1.2				
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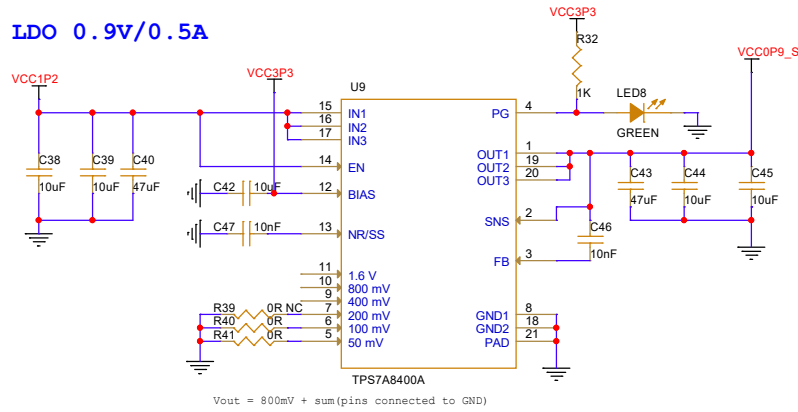
POWER TREE



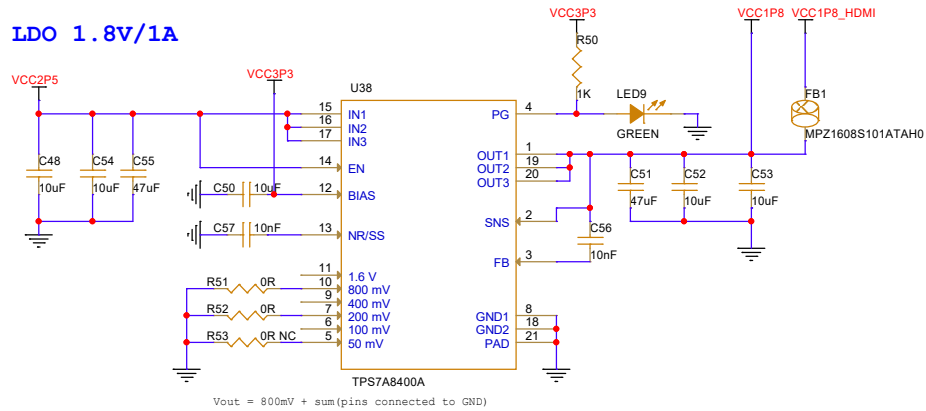
LDO 0.9V/1.5A



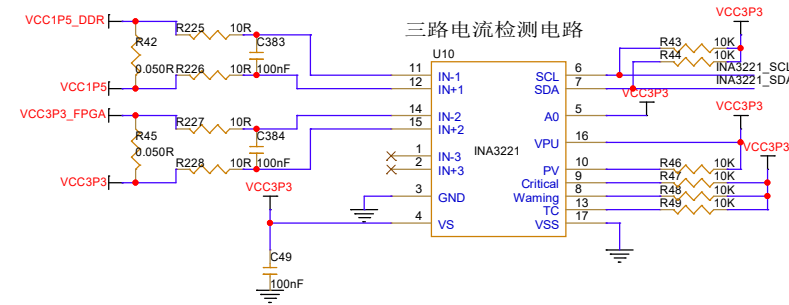
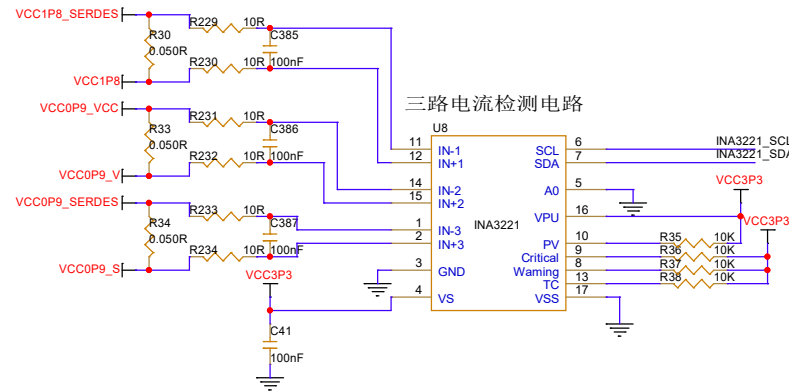
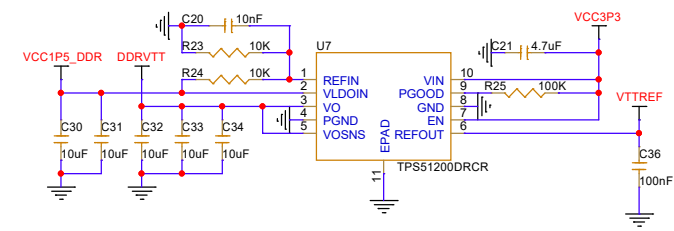
LDO 0.9V/0.5A



LDO 1.8V/1A



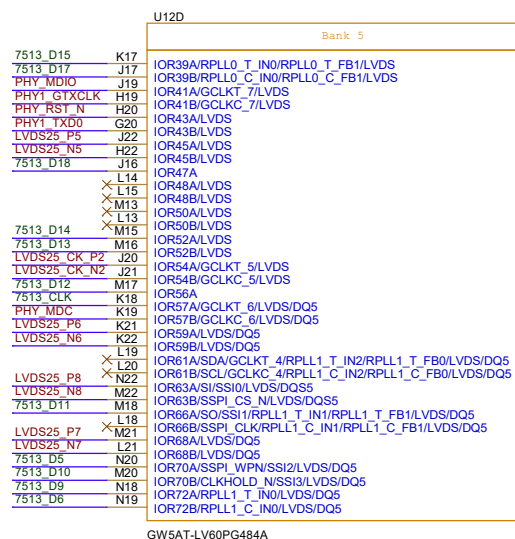
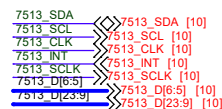
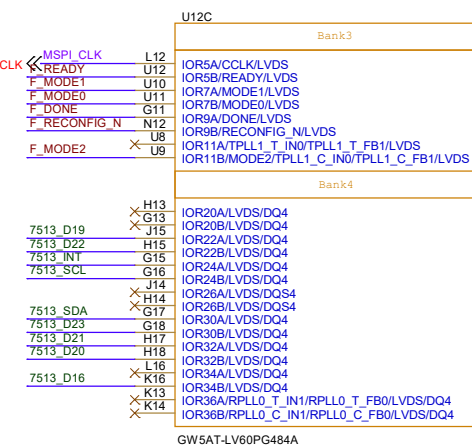
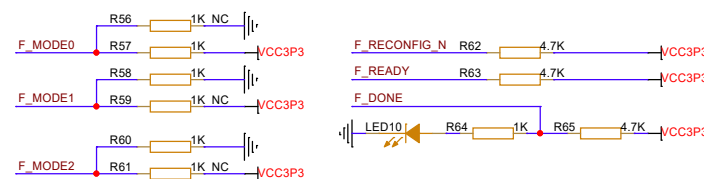
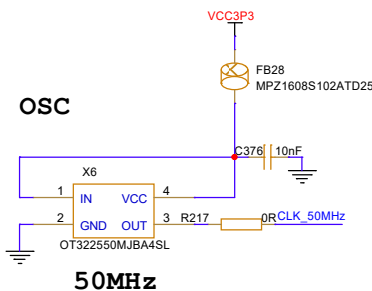
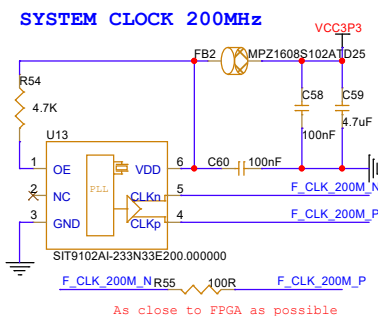
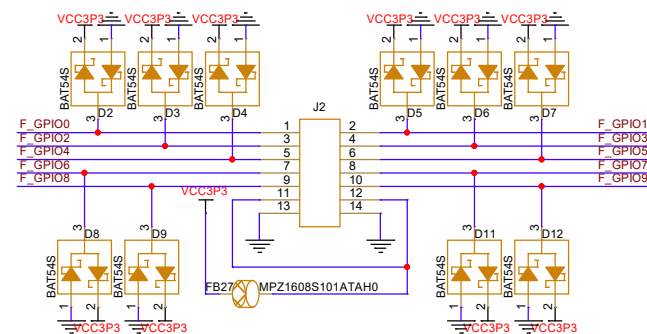
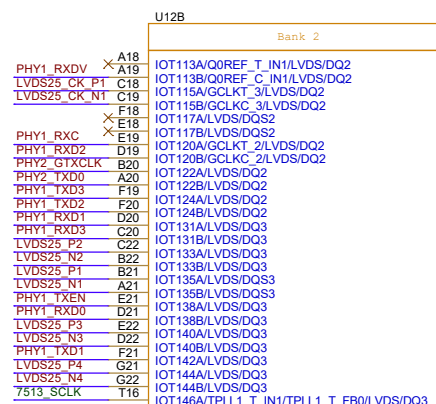
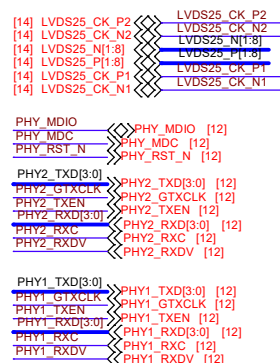
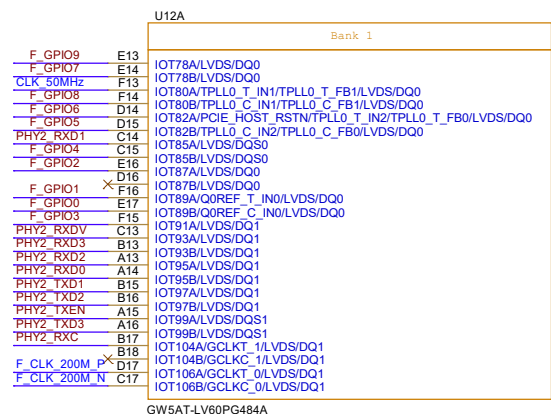
DDR Power For VTT/VREF

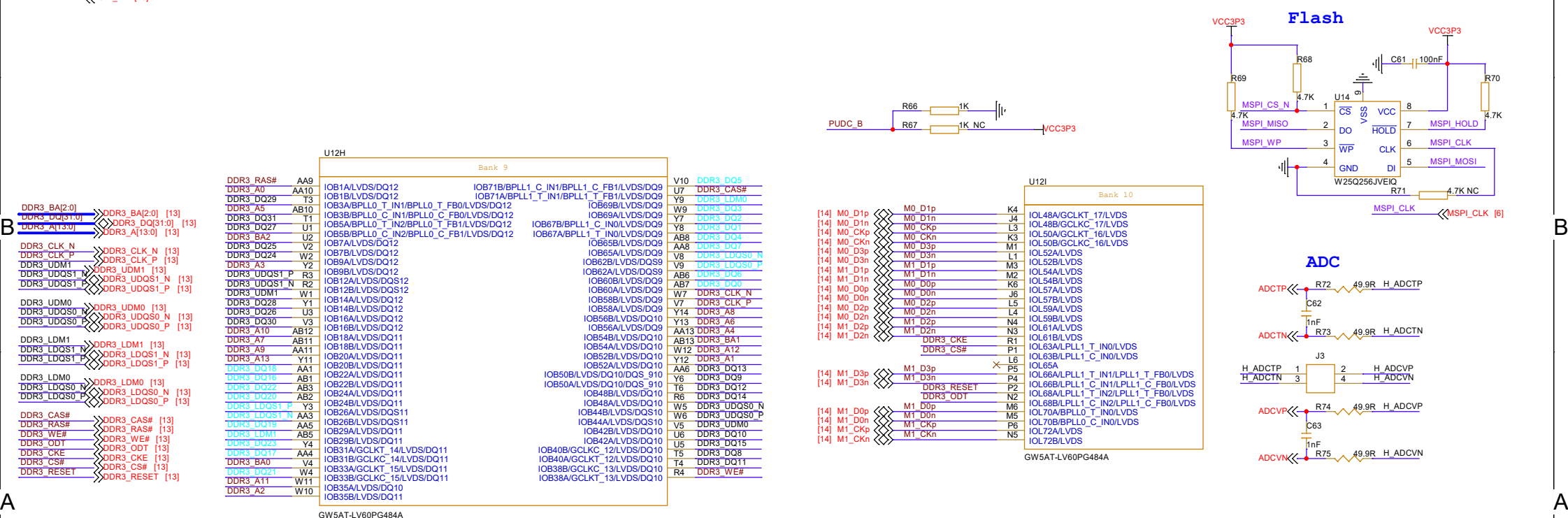
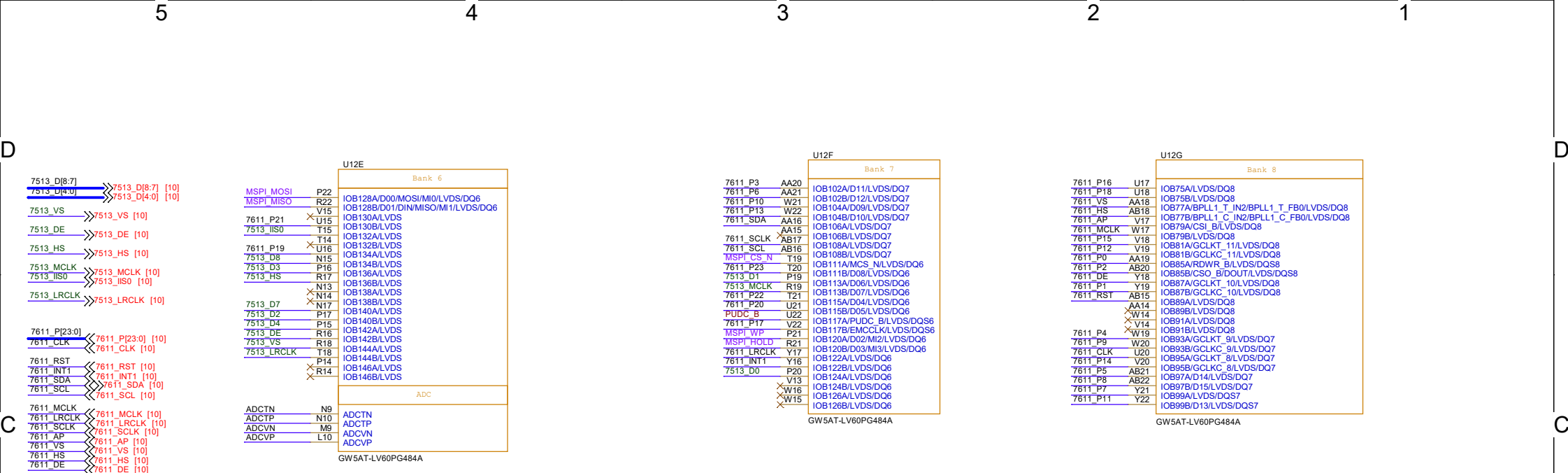


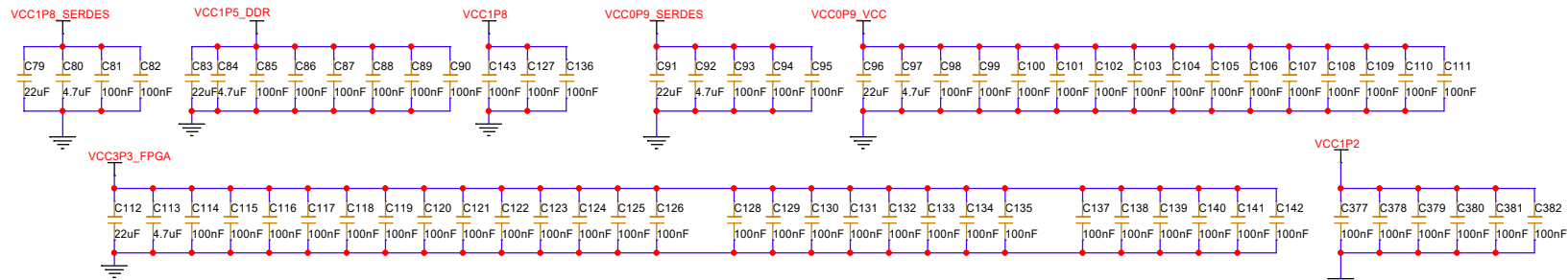
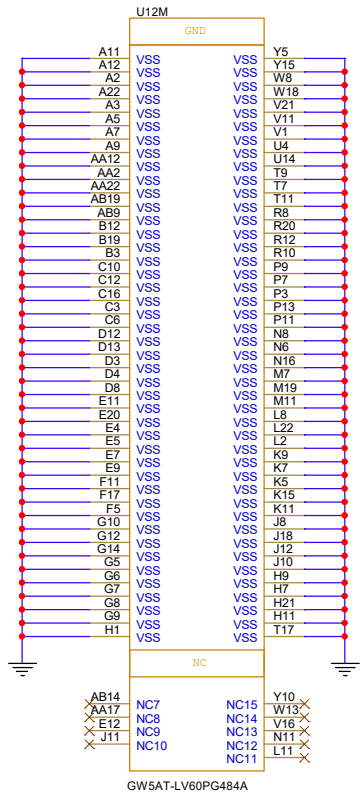
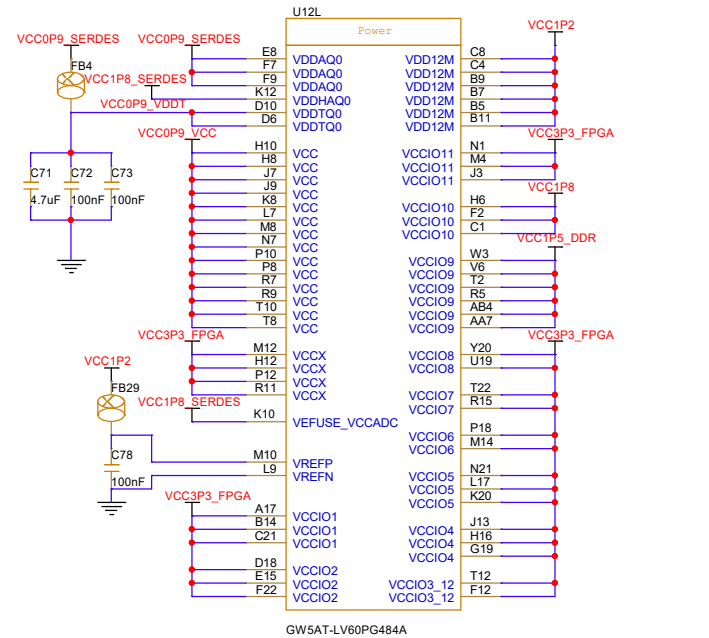
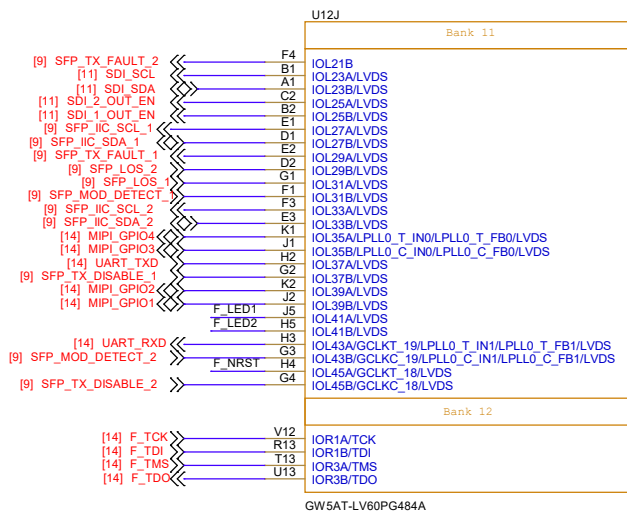
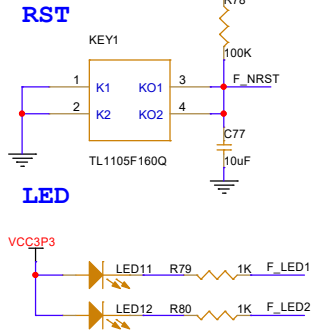
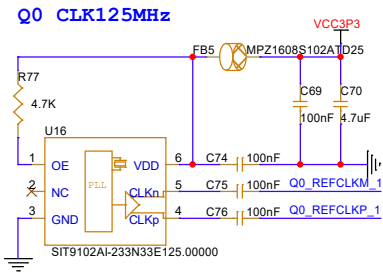
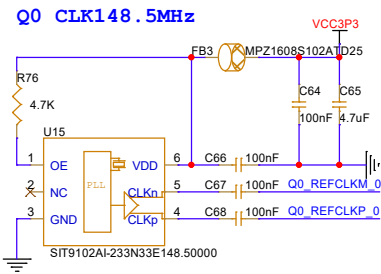
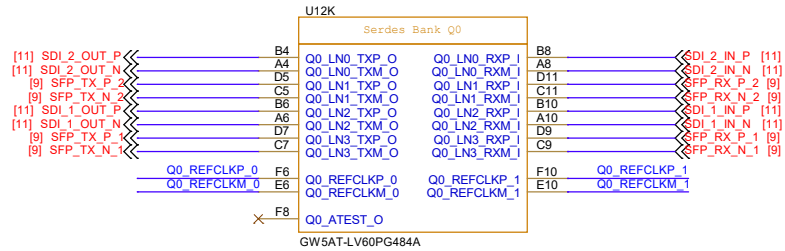
Power Test Hole



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D

C

B

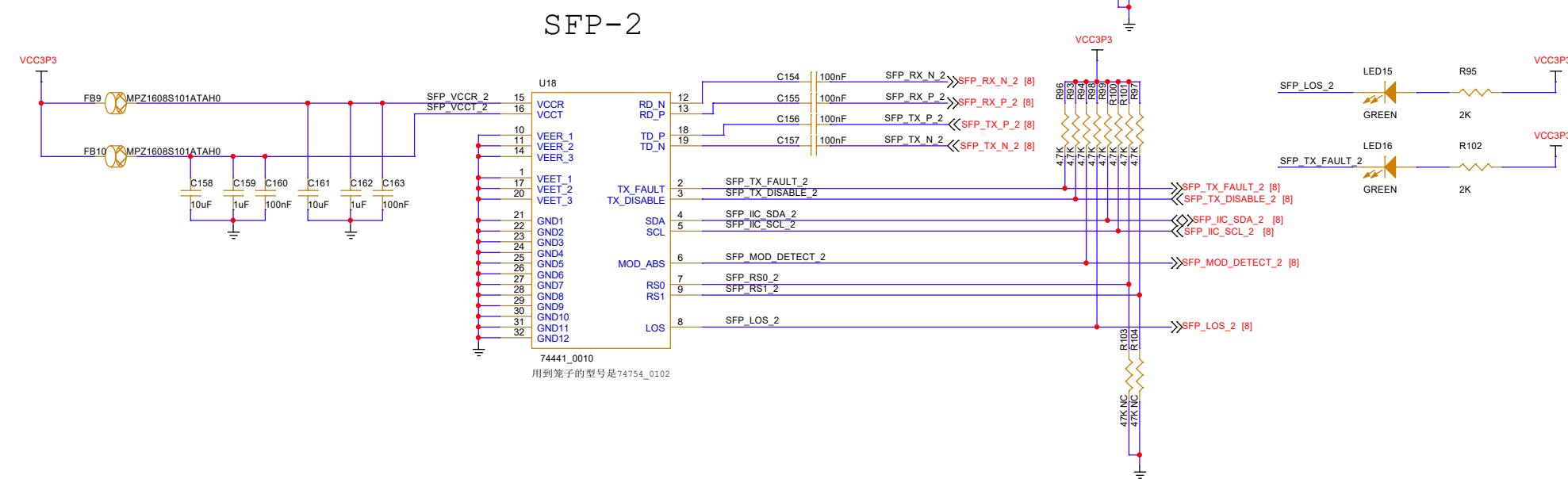
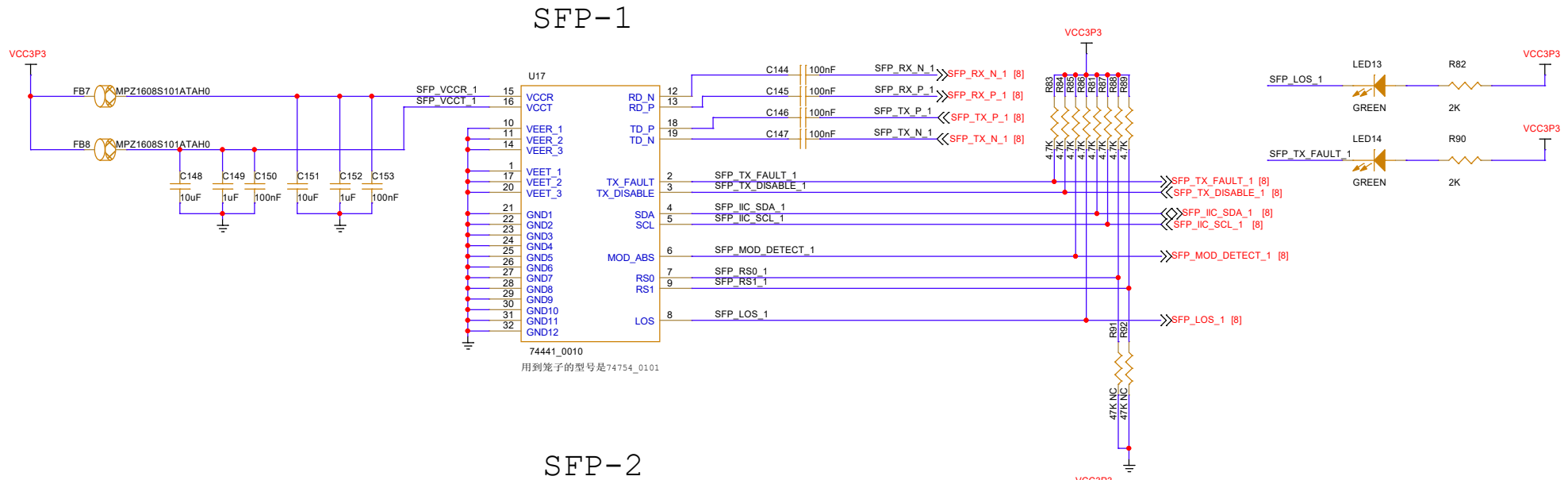
A

D

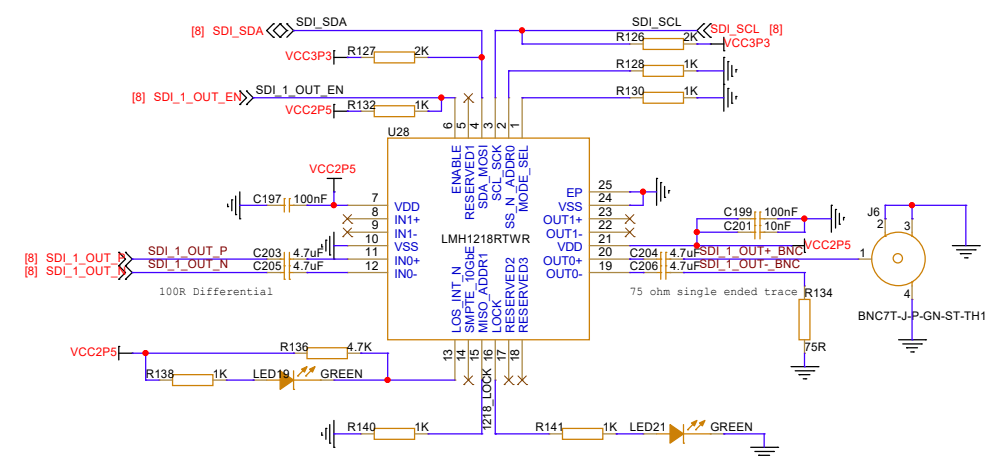
C

B

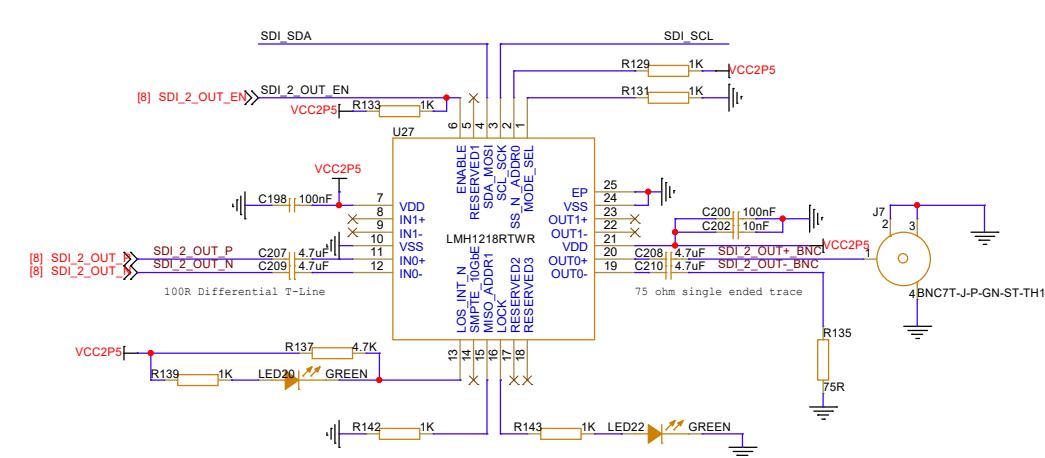
A



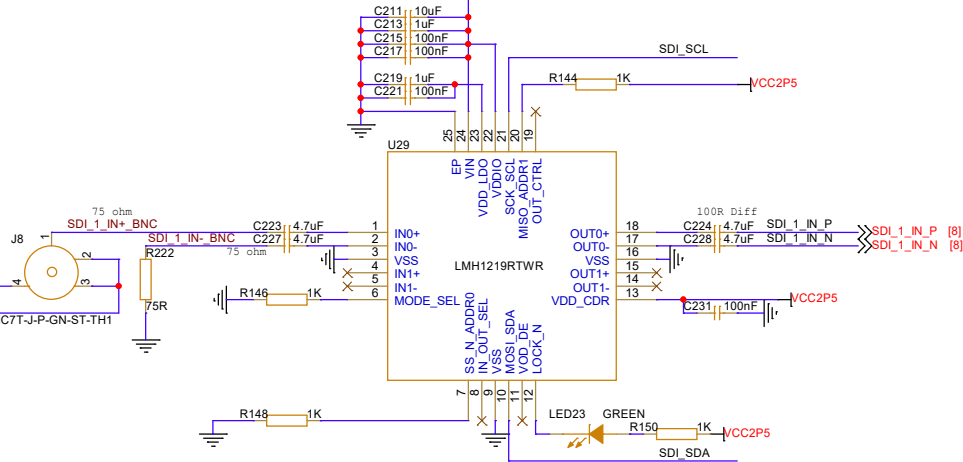
SDI-OUT-1



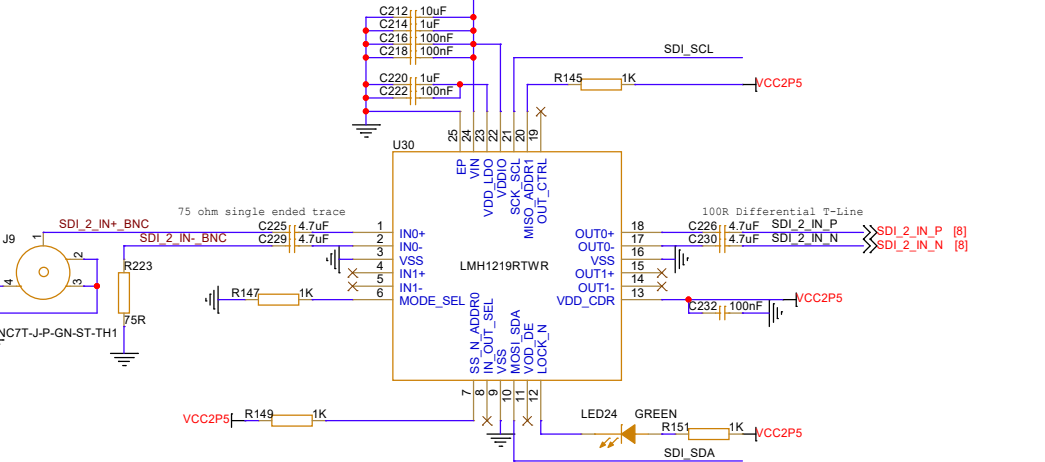
SDI-OUT-2



SDI-IN-1

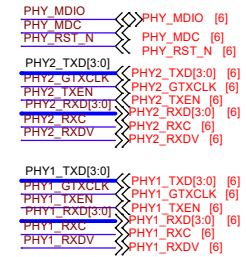
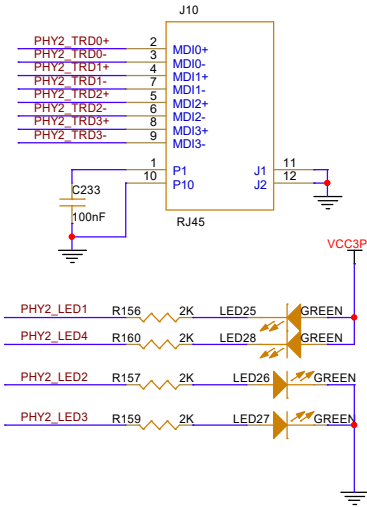
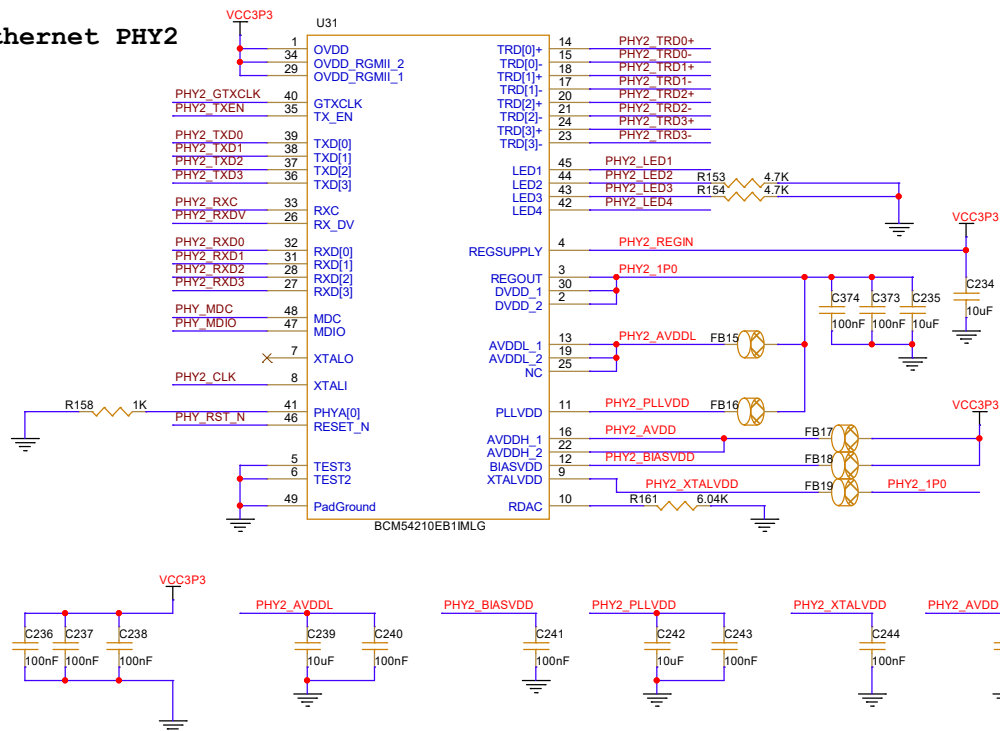


SDI-IN-2

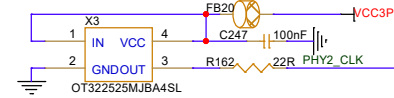


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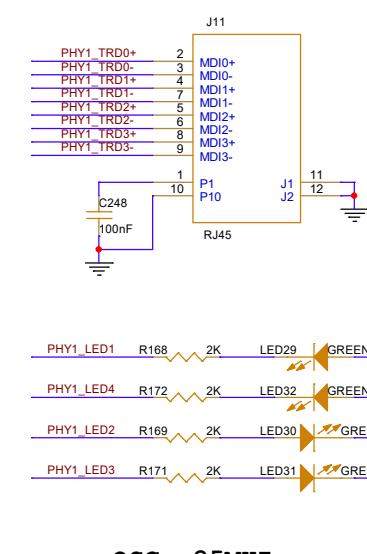
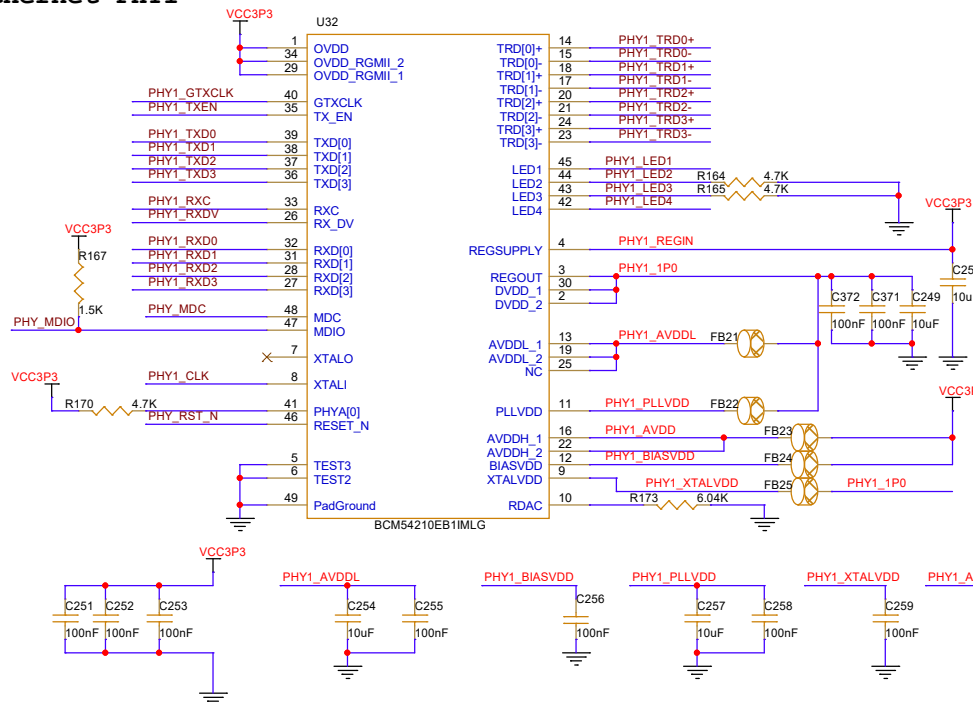
Ethernet PHY2



OSC 25MHZ



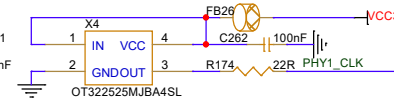
Ethernet PHY1



Default-LED Mode	(Non-LOM-LED mode):	
Status	LED[2]	LED[1]
1000BASE-T	ON	ON
100BASE-T	ON	OFF
10BASE-T	OFF	ON
No link	OFF	OFF

```
Set PHY Address as required.
TEST3/TES2 = 00, PHY[A] = 0: PHY address = 00000.
TEST3/TES2 = 00, PHY[A] = 1: PHY address = 00001.
```

OSC 25MHZ



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DDR3

