



DK_START_GW5AST-LV138FPG676A_V2.1

User Guide

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Revision History

Date	Version	Description
12/13/2024	1.0E	Initial version published.
04/30/2025	1.0.1E	The IO level in “Table 3-1 JTAG Pin Distribution” in “3.3 Download Module” updated.
03/13/2026	1.0.2E	The description of DDR3 in “2.1 Overview” optimized.

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1 About This Guide

1.1 Purpose

The DK_START_GW5AST-LV138FPG676A_V2.1 development board (hereinafter referred to as “the development board”) user guide consists of following three parts:

- A brief introduction to the features of the development board.
- An introduction to the development board system architecture and hardware resources.
- An introduction to the hardware circuits, functions and pin distribution.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [UG986, GW5AST-138 Pinout](#)
- [UG1102, GW5AST series of FPGA Products Package and Pinout User Guide](#)
- [UG704, Arora V 138K FPGA Products Programming and Configuration User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
ADC	Analog-to-Digital conversion
SFP	Small Form Pluggable
DDR	Double Data Rate
JTAG	Joint Test Action Group
LDO	Low Dropout Regulator
MIPI	Mobile Industry Processor Interface
HDMI	High Definition Multimedia Interface
SDI	Serial Digital Interface
LVDS	Low-Voltage Differential Signaling

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

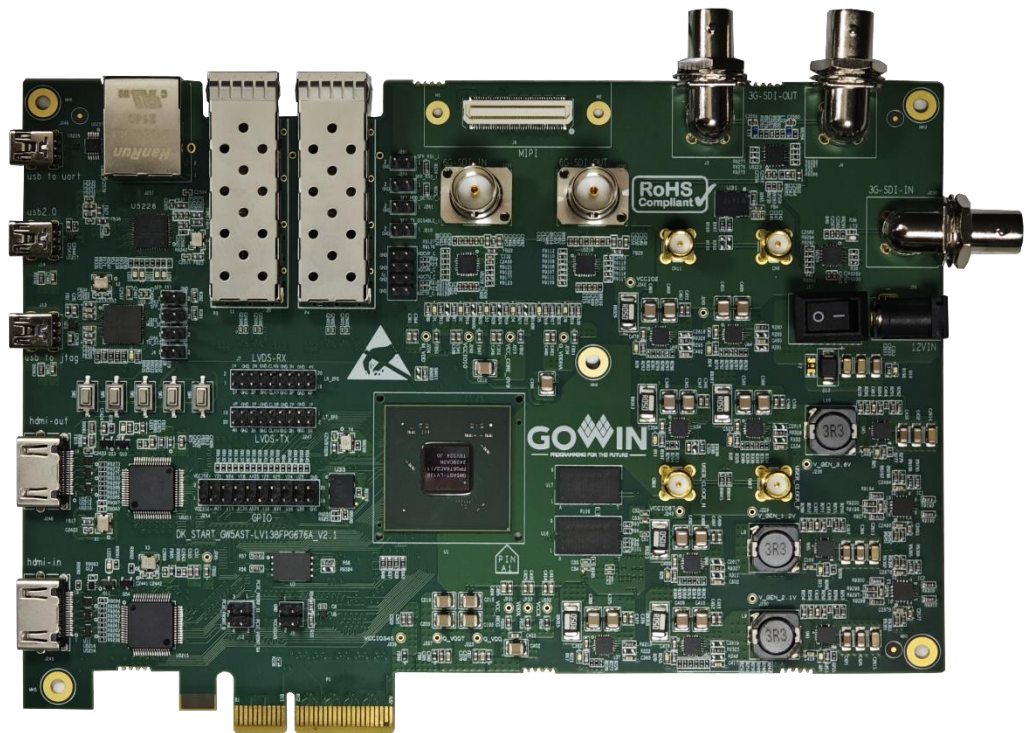
Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Development Board Introduction

2.1 Overview

Figure 2-1 DK_START_GW5AST-LV138FPG676A_V2.1 Development Board



Gowin GW5AST series of FPGA products are the 5 series products of Arora family, with abundant internal resources, high-performance DSP with a new architecture that supports AI operations, high-speed LVDS interface and abundant BSRAM resources. At the same time, it supports self-developed DDR3, 12.5Gbps SerDes supporting multiple protocols, and hard core processor RiscV AE350_SOC, providing a variety of packages. It is suitable for applications such as low power, high performance and compatibility design.

DK_START_GW5AST-LV138FPG676A_V2.1 development board applies to DDR3 high-speed storage, MIPI and SFP high-speed communication, integrates LVDS, SDI, Ethernet, HDMI, and ADC interfaces, supporting FPGA function evaluation, hardware verification, and software learning and debugging, etc.

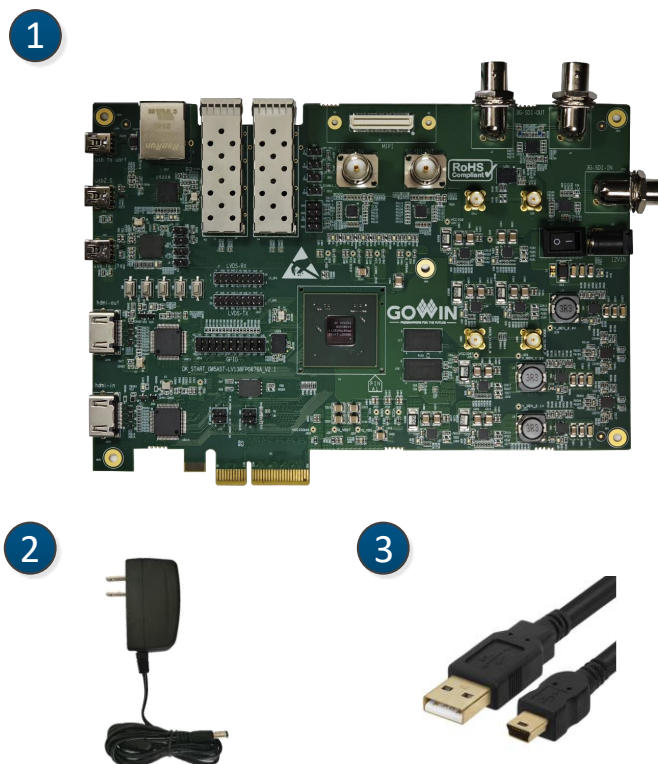
The development board adopts Gowin GW5AST-LV138FPG676A FPGA device. For the internal resources of the chip, see [DS1239](#), [GW5AST series of FPGA Products Data Sheet](#).

2.2 A Development Board Kit

The development board kit includes the following items:

1. DK_START_GW5AST-LV138FPG676A_V2.1 development board
2. 12V power (Input: AC 100-240V~50/60Hz 0.6A, output: DC12V 2A)
3. Mini USB-B download cable

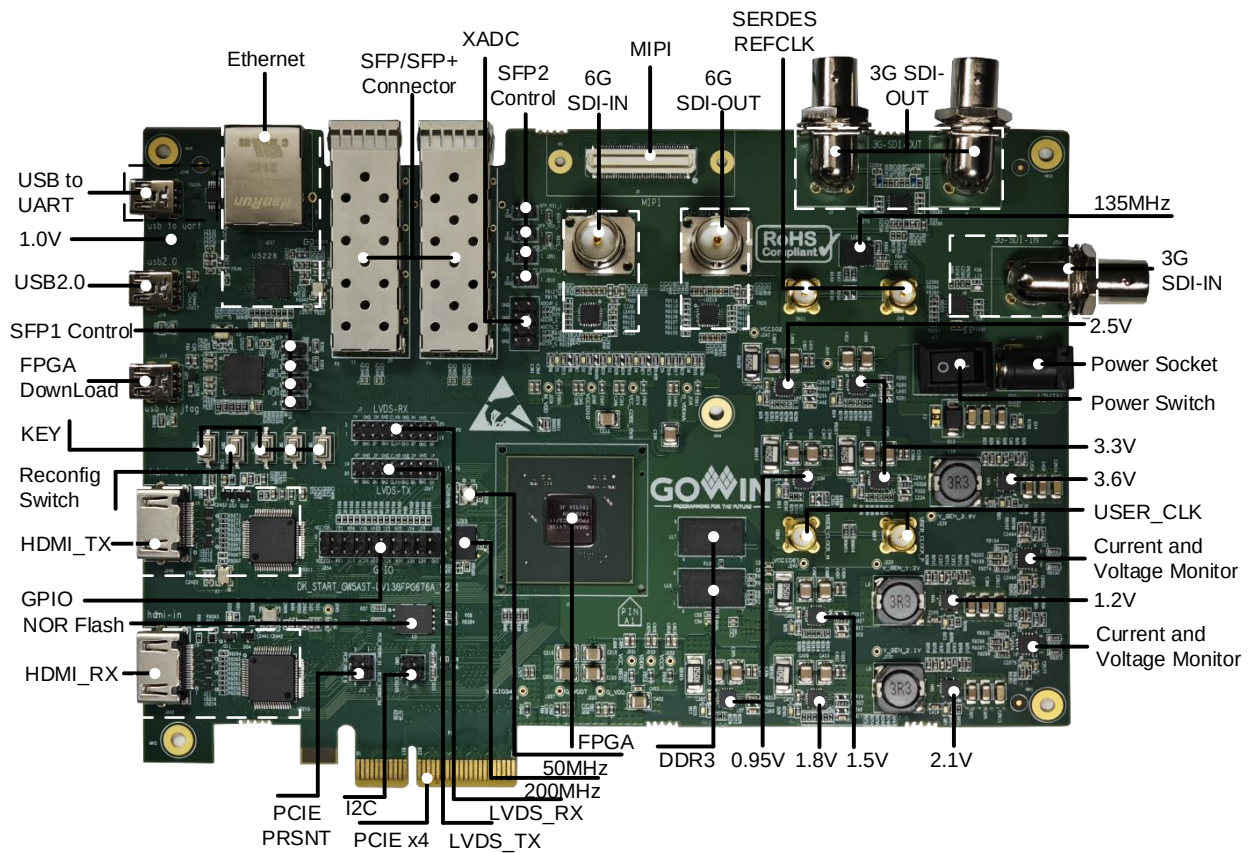
Figure 2-2 A Development Board Kit



- ① DK_START_GW5AST-LV138FPG676A_V2.1 development board
- ② 12V power supply adapter
- ③ Mini USB-B Cable

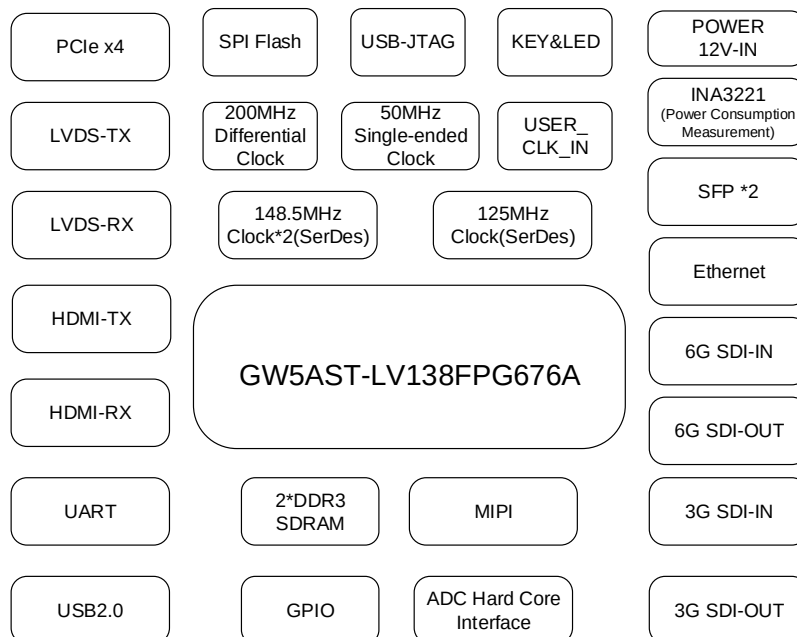
2.3 PCB Components

Figure 2-3 PCB Components



2.4 System Block Diagram

Figure 2-4 System Block Diagram



2.5 Features

The key features are as follows:

- **FPGA Device**
 - Gowin GW5AST-LV138FPG676A FPGA
- **Download and Boot**
 - Integrate USB download circuit on the development board, download through Mini USB-B interface
 - External SPI Flash Boot
- **Power**
 - External DC 12V 2A Power
 - The Power light is on after power on.
 - The development board generates 3.6V, 3.3V, 2.5V, 2.1V, 1.8V, 1.5V, 1.2V, 0.95V, and 0.75V power supplies.
- **Clock system**
 - 50MHz single-ended clock
 - 125MHz differential clock
 - 148.5MHz differential clock
 - 200MHz differential clock
 - Receiving differential clock signal through SMA interface
- **Memory device**
 - 4Gbit DDR3 SDRAM
 - 256Mbit NOR Flash
- **SFP Interface**
 - 2-channel SFP (Small Form Pluggable) connectors for SFP or SFP+ modules
- **HDMI Interface**
 - 1-channel HDMI-TX interface for HDMI-TX communication via the encoding chip
 - 1-channel HDMI-RX interface for HDMI-RX communication via the decoding chip
- **SDI Interface**
 - 3G SDI interfaces, including 1-channel 3G SDI-IN interface and 2-channel 3G SDI-OUT interfaces
 - 6G SDI interfaces, including 1-channel 6G SDI-IN interface and 1-channel 6G SDI-OUT interface
 - The 3G SDI interface supporting 2.97Gbps SDI data transfer
 - The 6G SDI interface supporting 5.94Gbps SDI data transfer
- **Ethernet Interface**
 - 1-channel Ethernet interface

- Support RGMII interfaces (10Base-T/100Base-TX/1000BASE-T)
 - RJ45 connector integrated with network transformer internally
- MIPI Interface
 - MIPI interface with dual channels, each channel includes 4 Data + 1 Clk
 - MIPI D-PHY RX hard core
 - 4-channel single-ended signals
- PCIe interface
 - 1-channel PClex4 interface
- LVDS Interface
 - 1-channel LVDS-TX interface, including 4 Data + 1 Clk
 - 1-channel LVDS-RX hard core, including 4 Data + 1 Clk
- USB 2.0 Interface
 - 1-channel USB2.0 interface
 - Mini USB-B Interface
- UART Interface
 - 1-channel UART interface
 - Mini USB-B Interface
- ADC Interface
 - 1-channel ADC interface
- LED & Key
 - 4 keys
 - 4 LED indicators
- GPIO
 - 16 GPIOs with 2.5V power

3 Development Board Circuit

3.1 FPGA

Overview

For the resources of GW5AST series of FPGA Products, refer to [*DS1239, GW5AST series of FPGA Products Data Sheet*](#).

I/O BANK Description

For the I/O BANK, package, and pinout information, see [*UG1102, GW5AST series of FPGA Products Package and Pinout User Guide*](#).

3.2 Power Supply for more details.

3.2.1 Introduction

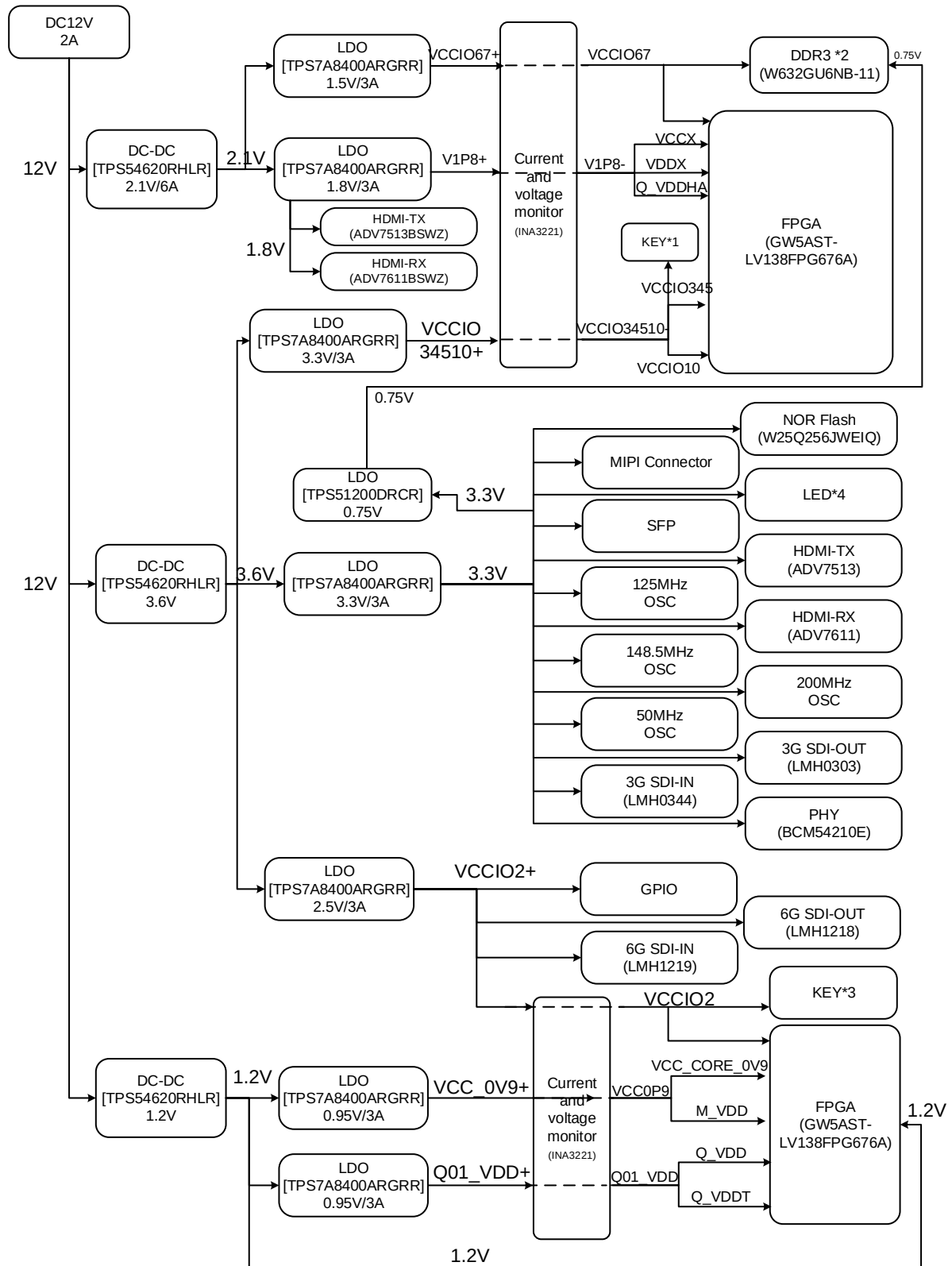
The development board needs to be powered by a 12V power adapter.

The input parameter of the adapter is AC 100-240V~50/60MHz 0.6A, and the output parameter is DC 12V 2A.

The input 12V power is regulated by the PMIC on the development board to generate 3.6V, 3.3V, 2.5V, 2.1V, 1.8V, 1.5V, 1.2V, 0.95V, and 0.75V power supplies.

3.2.2 Power Distribution

Figure 3-1 Power Distribution Diagram



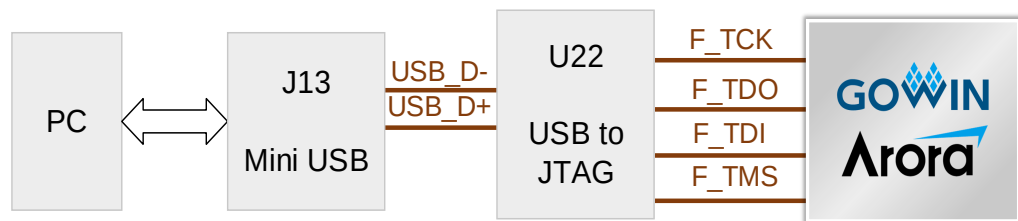
3.3 Download Module

3.3.1 Introduction

The development board includes a Mini USB-B download port (J13) designed to program the programs to external SPI FLASH or SRAM.

The download connection diagram is show in Figure 3-2.

Figure 3-2 Connection Diagram of Download



3.3.2 Pin Distribution

Table 3-1 JTAG Pin Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
TCK	H12	10	3.3V	JTAG signal
TDO	J10	10	3.3V	
TDI	H10	10	3.3V	
TMS	H11	10	3.3V	

3.4 Clock

3.4.1 Introduction

The development board includes multiple FPGA clock sources, including 1-channel 50 MHz single-ended clock, 1-channel 200 MHz differential clock, and 1-channel 125 MHz differential clock, 2-channel 148.5 MHz differential clocks, and 1-channel SMA input differential clock. The 125 MHz differential clock signal and 148.5 MHz differential clock signal are connected to the FPGA's SerDes high-speed clock pin, where the 125 MHz differential clock that provides the clock for the SerDes Q1 can be changed to an external SMA input clock. The clock pin distribution is as shown in Figure 3-3.

Figure 3-3 Clock Connection Diagram

50MHz	⌚	<u>F_CLK_50M</u>
200MHz	⌚	<u>SYS_CLK_P</u> <u>SYS_CLK_N</u>
148.5MHz	⌚	<u>Q0_REFCLKP_1</u> <u>Q0_REFCLKM_1</u>
125MHz/SMA	⌚	<u>Q1_REFCLKP_0</u> <u>Q1_REFCLKM_0</u>
148.5MHz	⌚	<u>Q1_REFCLKP_1</u> <u>Q1_REFCLKM_1</u>
SMA	⌚	<u>USER_CLOCK_P</u> <u>USER_CLOCK_N</u>



3.4.2 Pin Distribution

Table 3-2 Clock Pin Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_CLK_50M	N21	3	3.3V	50MHz single-ended clock
SYS_CLK_P	M21	3	3.3V	200MHz differential clock
SYS_CLK_N	M22	3	3.3V	200MHz differential clock
Q1_REFCLKP_0	AA11	Q1	-	125MHz differential clock/SMA input differential clock
Q1_REFCLKM_0	AB11	Q1	-	125MHz differential clock/SMA input differential clock
Q1_REFCLKP_1	AA13	Q1	-	148.5MHz differential clock
Q1_REFCLKM_1	AB13	Q1	-	148.5MHz differential clock
Q0_REFCLKP_1	F13	Q0	-	148.5MHz differential clock
Q0_REFCLKM_1	E13	Q0	-	148.5MHz differential clock
USER_CLOCK_P	R3	7	1.5V	SMA input differential clock
USER_CLOCK_N	P3	7	1.5V	SMA input differential clock

3.5 DDR3

3.5.1 Introduction

The development board includes two 2-Gbit DDR3 chips. The signal of DDR3 chip is connected to the BANK6 and BANK7 of FPGA. The specific configurations of DDR3 are as shown in Table 3-3.

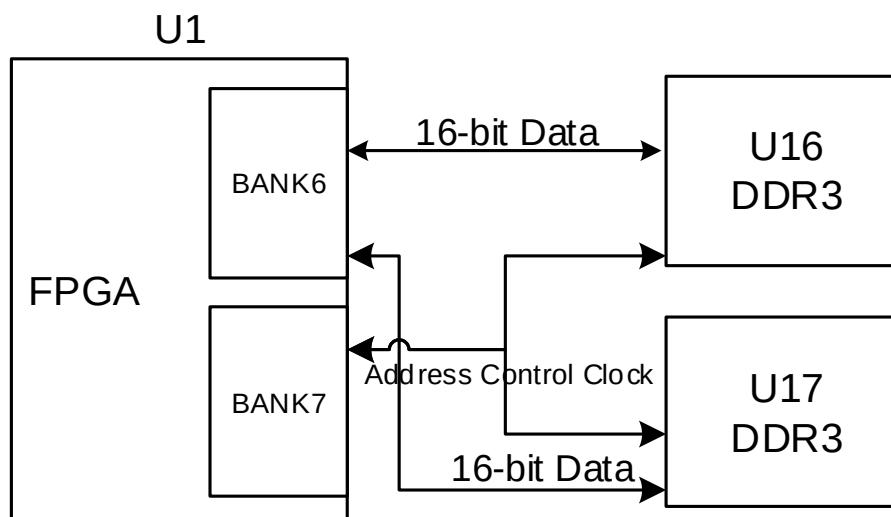
Table 3-3 DDR3 Configuration

Designator	Capacity
U16	16M x 8 Banks x 16bit
U17	16M x 8 Banks x 16bit

DDR3 hardware design requires strict consideration of signal integrity. In the design of circuit and PCB, matching resistor/termination resistor, impedance control and equal length control of traces have been fully considered to ensure DDR3 works stably at high speed.

The hardware connection diagram of DDR3 is as show in Figure 3-4.

Figure 3-4 Hardware Connection Diagram of DDR3



3.5.2 Pin Distribution

Table 3-4 DDR3 Pin Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
DDR3_A0	N1	7	1.5V	Address
DDR3_A1	R1	7	1.5V	Address
DDR3_A2	R2	7	1.5V	Address
DDR3_A3	N2	7	1.5V	Address
DDR3_A4	P1	7	1.5V	Address
DDR3_A5	T2	7	1.5V	Address
DDR3_A6	N4	7	1.5V	Address
DDR3_A7	U1	7	1.5V	Address
DDR3_A8	T4	7	1.5V	Address
DDR3_A9	T3	7	1.5V	Address
DDR3_A10	M1	7	1.5V	Address
DDR3_A11	P4	7	1.5V	Address
DDR3_A12	N3	7	1.5V	Address
DDR3_A13	U2	7	1.5V	Address
DDR3_BA0	M4	7	1.5V	Bank address
DDR3_BA1	L5	7	1.5V	Bank address
DDR3_BA2	K3	7	1.5V	Bank address
DDR3_CS#	L4	7	1.5V	Chip select
DDR3_CAS#	H1	7	1.5V	Column address strobe
DDR3_CKE	L3	7	1.5V	Clock Enable
DDR3_ODT	J1	7	1.5V	On-Die Termination Enable
DDR3_RAS#	H2	7	1.5V	Row address strobe
DDR3_RESET	N8	7	1.5V	Reset
DDR3_WE#	J3	7	1.5V	Write enable
DDR3_CLK0_P	M2	7	1.5V	Differential clock
DDR3_CLK0_N	L2	7	1.5V	Differential clock

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
DDR3_DQ0	G4	6	1.5V	Data
DDR3_DQ1	J6	6	1.5V	Data
DDR3_DQ2	L8	6	1.5V	Data
DDR3_DQ3	G5	6	1.5V	Data
DDR3_DQ4	K7	6	1.5V	Data
DDR3_DQ5	J5	6	1.5V	Data
DDR3_DQ6	K8	6	1.5V	Data
DDR3_DQ7	K6	6	1.5V	Data
DDR3_DQ8	E6	6	1.5V	Data
DDR3_DQ9	H8	6	1.5V	Data
DDR3_DQ10	H6	6	1.5V	Data
DDR3_DQ11	G8	6	1.5V	Data
DDR3_DQ12	D6	6	1.5V	Data
DDR3_DQ13	F8	6	1.5V	Data
DDR3_DQ14	G6	6	1.5V	Data
DDR3_DQ15	F7	6	1.5V	Data
DDR3_DM0	F4	6	1.5V	Data input mask
DDR3_DM1	H9	6	1.5V	Data input mask
DDR3_DQS0_P	J4	6	1.5V	Data Clock
DDR3_DQS0_N	H4	6	1.5V	Data Clock
DDR3_DQS1_P	H7	6	1.5V	Data Clock
DDR3_DQS1_N	G7	6	1.5V	Data Clock
DDR3_DQ0_1	C4	6	1.5V	Data
DDR3_DQ1_1	F3	6	1.5V	Data
DDR3_DQ2_1	B4	6	1.5V	Data
DDR3_DQ3_1	E5	6	1.5V	Data
DDR3_DQ4_1	D3	6	1.5V	Data
DDR3_DQ5_1	D5	6	1.5V	Data
DDR3_DQ6_1	A4	6	1.5V	Data
DDR3_DQ7_1	D4	6	1.5V	Data

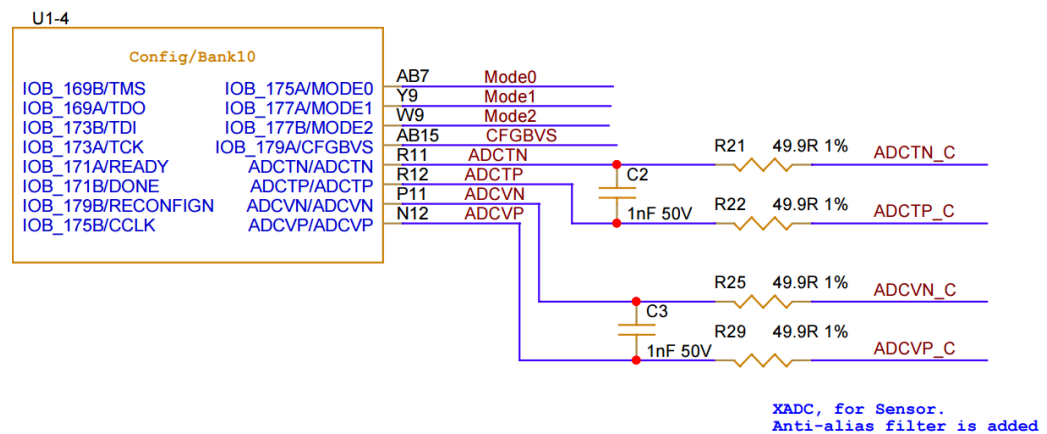
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
DDR3_DQ8_1	E1	6	1.5V	Data
DDR3_DQ9_1	A2	6	1.5V	Data
DDR3_DQ10_1	G2	6	1.5V	Data
DDR3_DQ11_1	C2	6	1.5V	Data
DDR3_DQ12_1	F2	6	1.5V	Data
DDR3_DQ13_1	E2	6	1.5V	Data
DDR3_DQ14_1	G1	6	1.5V	Data
DDR3_DQ15_1	D1	6	1.5V	Data
DDR3_DM0_1	E3	6	1.5V	Data input mask
DDR3_DM1_1	A3	6	1.5V	Data input mask
DDR3_DQS0_P_1	B5	6	1.5V	Data Clock
DDR3_DQS0_N_1	A5	6	1.5V	Data Clock
DDR3_DQS1_P_1	C1	6	1.5V	Data Clock
DDR3_DQS1_N_1	B1	6	1.5V	Data Clock

3.6 ADC Interface

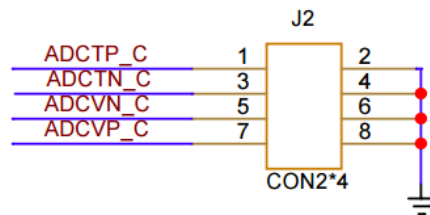
3.6.1 Introduction

The development board includes input interfaces for ADC signals. The connector uses a 2x4P pin header with 2.54 mm pitch. Figure 3-5 is the ADC schematic connection diagram and the anti-aliasing filter circuit.

Figure 3-5 ADC Schematic



XADC Header



3.6.2 Pin Distribution

Table 3-5 Pin Distribution of ADC Interface

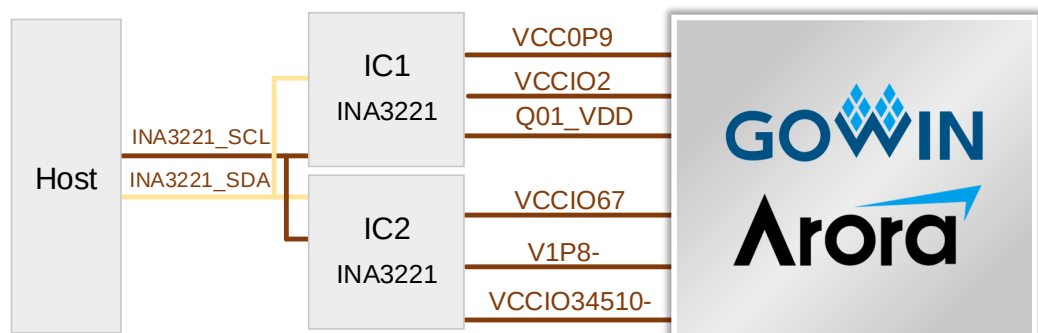
J2 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	ADCTP_C	R12	10	3.3V	Analog signal input
3	ADCTN_C	R11	10	3.3V	Analog signal input
5	ADCVN_C	P11	10	3.3V	Analog signal input
7	ADCVP_C	N12	10	3.3V	Analog signal input

3.7 I2C Interface

3.7.1 Introduction

The development board includes 1-channel I2C interface as the host communication interface. The host can monitor the power consumption of FPGA VCC, MIPI, VCCX, SerDes, and each BANK through this interface. The connection diagram of I2C interface is shown in Figure 3-6.

Figure 3-6 Connection Diagram of I2C Interface



3.7.2 Pin Distribution

Table 3-6 Pin Distribution of I2C Interface

J5 Pin No.	Signal Name	I/O Level	Description
1	GND	-	GND
2	VCCIO345	3.3V	Power
3	INA3221_SDA	3.3V	Serial bus data line
4	INA3221_SCL	3.3V	Serial bus clock line

3.8 MIPI Interface

3.8.1 Introduction

The development board leads one dual-channel MIPI interface from the FPGA, each with 4 Data and 1 Clk. The MIPI interface is connected to the FPGA's MIPI-DPHY RX hard core and uses 80P AXK580147YG connector with 0.5mm pitch. In addition, the MIPI interface also exposes 4 single-ended signals, a power supply, and ground. The connection diagram of MIPI interface is shown in Figure 3-7.

Figure 3-7 Connection Diagram of MIPI Interface



3.8.2 Pin Distribution

Table 3-7 Pin Distribution of MIPI Interfaces

J9 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	M0_D0N	W1	MIPI	-	MIPI data signal
2	NC	-	-	-	Floating
3	M0_D0P	V1	MIPI	-	MIPI data signal
4	NC	-	-	-	Floating
5	GND	-	-	-	GND
6	NC	-	-	-	Floating
7	M0_D1N	AA2	MIPI	-	MIPI data signal
8	NC	-	-	-	Floating
9	M0_D1P	Y2	MIPI	-	MIPI data signal
10	GND	-	-	-	GND
11	GND	-	-	-	GND
12	NC	-	-	-	Floating
13	M0_CKN	AA3	MIPI	-	MIPI clock signal
14	NC	-	-	-	Floating
15	M0_CKP	Y3	MIPI	-	MIPI clock signal
16	NC	-	-	-	Floating
17	GND	-	-	-	GND
18	NC	-	-	-	Floating
19	M0_D2N	W3	MIPI	-	MIPI data signal
20	GND	-	-	-	GND
21	M0_D2P	V3	MIPI	-	MIPI data signal
22	NC	-	-	-	Floating
23	GND	-	-	-	GND
24	NC	-	-	-	Floating
25	M0_D3N	W4	MIPI	-	MIPI data signal
26	NC	-	-	-	Floating

J9 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
27	M0_D3P	V4	MIPI	-	MIPI data signal
28	NC	-	-	-	Floating
29	GND	-	-	-	GND
30	GND	-	-	-	GND
31	M1_D0N	AC1	MIPI	-	MIPI data signal
32	NC	-	-	-	Floating
33	M1_D0P	AB1	MIPI	-	MIPI data signal
34	NC	-	-	-	Floating
35	GND	-	-	-	GND
36	NC	-	-	-	Floating
37	M1_D1N	AE1	MIPI	-	MIPI data signal
38	NC	-	-	-	Floating
39	M1_D1P	AD1	MIPI	-	MIPI data signal
40	GND	-	-	-	GND
41	GND	-	-	-	GND
42	NC	-	-	-	Floating
43	M1_CKN	AF2	MIPI	-	MIPI clock signal
44	NC	-	-	-	Floating
45	M1_CKP	AE2	MIPI	-	MIPI clock signal
46	NC	-	-	-	Floating
47	GND	-	-	-	GND
48	NC	-	-	-	Floating
49	M1_D2N	AF3	MIPI	-	MIPI data signal
50	GND	-	-	-	GND
51	M1_D2P	AE3	MIPI	-	MIPI data signal
52	CSI_RST	G17	5	3.3V	Reset signal
53	GND	-	-	-	GND
54	CSI_CLK	J23	4	3.3V	Clock signal
55	M1_D3N	AF5	MIPI	-	MIPI data signal

J9 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
56	CSI_SCL	H23	4	3.3V	I2C clock signal
57	M1_D3P	AE5	MIPI	-	MIPI data signal
58	CSI_SDA	H24	4	3.3V	I2C data signal
59	GND	-	-	-	GND
60	GND	-	-	-	GND
61	GND	-	-	-	GND
62	NC	-	-	-	Floating
63	NC	-	-	-	Floating
64	NC	-	-	-	Floating
65	NC	-	-	-	Floating
66	GND	-	-	-	GND
67	NC	-	-	-	Floating
68	NC	-	-	-	Floating
69	NC	-	-	-	Floating
70	NC	-	-	-	Floating
71	GND	-	-	-	GND
72	NC	-	-	-	Floating
73	NC	-	-	-	Floating
74	GND	-	-	-	GND
75	NC	-	-	-	Floating
76	AlwaysOn_3.3V	-	-	3.3V	Power
77	NC	-	-	-	Floating
78	AlwaysOn_3.3V	-	-	3.3V	Power
79	NC	-	-	-	Floating
80	AlwaysOn_3.3V	-	-	3.3V	Power

3.9 PCIe Interface

3.9.1 Introduction

The development board provides one PCIe x4 interface. The transceiver signals of the PCIe interface are directly connected to the SerDes high-speed signals of the FPGA, and the TX and RX signals of the four channels are connected to the FPGA as differential signals. The design diagram is shown in Figure 3-8.

Figure 3-8 Connection Diagram of PCIe Interface



3.9.2 Pin Distribution

Table 3-8 Pin Distribution of PCIe Interface

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
PCIE_WAKE_B	N26	3	3.3V	The PCIe device wakes up
PCIE_PERST	M26	3	3.3V	The PCIe device wakes up
PCIE_CLK_QO_C_P	F11	Q0	-	Reference clock of PCIe
PCIE_CLK_QO_C_N	E11	Q0	-	Reference clock of PCIe
PCIE_RX0_P	D12	Q0	-	PCIe receive data
PCIE_RX0_N	C12	Q0	-	PCIe receive data
PCIE_RX1_P	D14	Q0	-	PCIe receive data
PCIE_RX1_N	C14	Q0	-	PCIe receive data
PCIE_RX2_P	B13	Q0	-	PCIe receive data
PCIE_RX2_N	A13	Q0	-	PCIe receive data

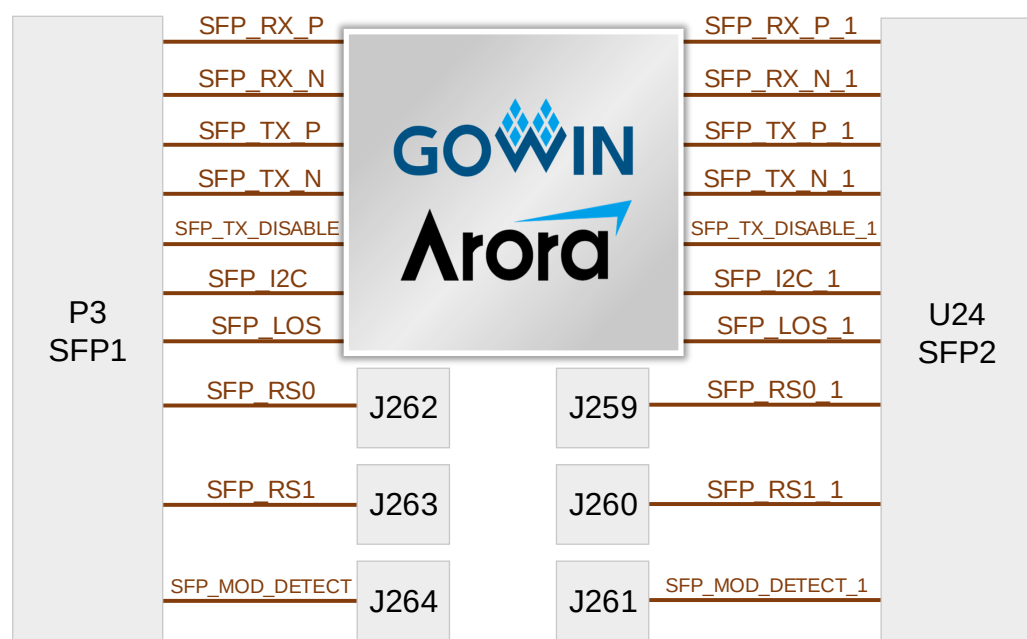
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
PCIE_RX3_P	B11	Q0	-	PCIE receive data
PCIE_RX3_N	A11	Q0	-	PCIE receive data
PCIE_TX0_P	D10	Q0	-	PCIE transmit data
PCIE_TX0_N	C10	Q0	-	PCIE transmit data
PCIE_TX1_P	D8	Q0	-	PCIE transmit data
PCIE_TX1_N	C8	Q0	-	PCIE transmit data
PCIE_TX2_P	B9	Q0	-	PCIE transmit data
PCIE_TX2_N	A9	Q0	-	PCIE transmit data
PCIE_TX3_P	B7	Q0	-	PCIE transmit data
PCIE_TX3_N	A7	Q0	-	PCIE transmit data

3.10 SFP Interface

3.10.1 Introduction

The development board includes two SFP connectors for SFP or SFP+ modules. The external jumper cap can be used to control the level to select whether to turn off the transmission, the SFP module rate, and whether the module is in place. The design diagram is shown in Figure 3-9.

Figure 3-9 Connection Diagram of SFP Interface



3.10.2 Pin Distribution

Table 3-9 Pin Distribution of SFP1 Interface

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
SFP_RX_P	AC12	Q1	-	Receive partial differential signal outputs
SFP_RX_N	AD12	Q1	-	Receive partial differential signal outputs
SFP_TX_P	AC10	Q1	-	Transmit partial differential signal inputs
SFP_TX_N	AD10	Q1	-	Transmit partial differential signal inputs
SFP_TX_FAULT	-	-	-	Transmitting error
SFP_TX_DISABLE	R23	3	3.3V	Turn off enable input, connect pin J6 when transmitting. High: Transmit disabled; Low: Transmit enabled. The default is high currently.
SFP_IIC_SDA	N19	3	3.3V	I2C data bus
SFP_IIC_SCL	P19	3	3.3V	I2C clock bus
SFP_MODULE_DETECT	-	-	-	Module presence detection: When the module is inserted, it should be connected to pin J264. High: No SFP+ module in P3 slot; Low: SFP+ module in the slot. The default is high currently.
SFP_RS0	-	-	-	Speed selection: Control the speed of the receivers, connecting to pin J262. High: High speed; Low: Low speed. The default is high currently.
SFP_RS1	-	-	-	Speed selection: Control the

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
				speed of the receivers, connecting to pin J263. High: High speed; Low: Low speed. The default is high currently.
SFP_LOS	R20	3	3.3V	Indicator signal for receiver loss

Table 3-10 Pin Distribution of SFP2 Interface

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
SFP_RX_P_1	AE11	Q1	-	Receive partial differential signal outputs
SFP_RX_N_1	AF11	Q1	-	Receive partial differential signal outputs
SFP_TX_P_1	AE7	Q1	-	Transmit partial differential signal input
SFP_TX_N_1	AF7	Q1	-	Transmit partial differential signal input
SFP_TX_FAULT_1	-	-	-	Transmitting error
SFP_TX_DISABLE_1	R25	3	3.3V	Turn off enable input, connect pin J210 when transmitting; High: Transmit disabled; Low: Transmit enabled The default is high currently.
SFP_IIC_SDA_1	P26	3	3.3V	I2C data bus
SFP_IIC_SCL_1	R26	3	3.3V	I2C clock bus
SFP_MODULE_DETECT_1	-	-	-	Module presence detection: When the module is inserted, it should be connected to pin J261. High: No SFP+ module in P3

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
				slot; Low: SFP+ module in the slot. The default is high currently.
SFP_RS0_1	-	-	-	Speed selection: Control the speed of the receivers, connecting to pin J259. High: High speed; Low: Low speed. The default is high currently.
SFP_RS1_1	-	-	-	Speed selection: Control the speed of the receivers, connecting to pin J260. High: High speed; Low: Low speed. The default is high currently.
SFP_LOS_1	T23	3	3.3V	Indicator signal for receiver loss

3.11 LVDS Interface

3.11.1 Introduction

The development board includes both LVDS transmitter and receiver interfaces, with each connector being a 2x9P pin headers with 2.0 mm pitch. LVDS_TX contains 4 Data and 1 Clk; LVDS_RX contains 4 Data and 1 Clk. The connection diagram is shown in Figure 3-10.

Figure 3-10 Connection Diagram of LVDS Interface



3.11.2 Pin Distribution

Table 3-11 Pin Distribution of LVDS_TX Interface

J247 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	LT_2P5_1p	Y22	2	2.5V	LVDS data
2	LT_2P5_1n	Y23	2	2.5V	LVDS data
3	GND	-	-	-	GND
4	GND	-	-	-	GND
5	LT_2P5_2p	T20	2	2.5V	LVDS data
6	LT_2P5_2n	U20	2	2.5V	LVDS data
7	GND	-	-	-	GND
8	GND	-	-	-	GND
9	LT_2P5_CLKp	U21	2	2.5V	LVDS Clock
10	LT_2P5_CLKn	V21	2	2.5V	LVDS Clock
11	GND	-	-	-	GND
12	GND	-	-	-	GND
13	LT_2P5_3p	W20	2	2.5V	LVDS data
14	LT_2P5_3n	Y20	2	2.5V	LVDS data
15	GND	-	-	-	GND
16	GND	-	-	-	GND
17	LT_2P5_4p	T19	2	2.5V	LVDS data
18	LT_2P5_4n	U19	2	2.5V	LVDS data

Table 3-12 LVDS_RX Interface Pin Distribution

J7 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	LR_2P5_1p	AA24	2	2.5V	LVDS data
2	LR_2P5_1n	AB25	2	2.5V	LVDS data
3	GND	-	-	-	GND
4	GND	-	-	-	GND
5	LR_2P5_2p	V23	2	2.5V	LVDS data

J7 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
6	LR_2P5_2n	W23	2	2.5V	LVDS data
7	GND	-	-	-	GND
8	GND	-	-	-	GND
9	LR_2P5_CLK _p	U22	2	2.5V	LVDS Clock
10	LR_2P5_CLK _n	V22	2	2.5V	LVDS Clock
11	GND	-	-	-	GND
12	GND	-	-	-	GND
13	LR_2P5_3p	AB24	2	2.5V	LVDS data
14	LR_2P5_3n	AC24	2	2.5V	LVDS data
15	GND	-	-	-	GND
16	GND	-	-	-	GND
17	LR_2P5_4p	AA22	2	2.5V	LVDS data
18	LR_2P5_4n	AA23	2	2.5V	LVDS data

3.12 GPIO Interface

3.12.1 Introduction

The development board leads sixteen 2.5V GPIOs through one 2*10P pin header with 2.54 mm pitch, facilitating user testing.

Figure 3-11 Connection Diagram of GPIO Interface



3.12.2 Pin Distribution

Table 3-13 Pin Distribution of GPIO Interface

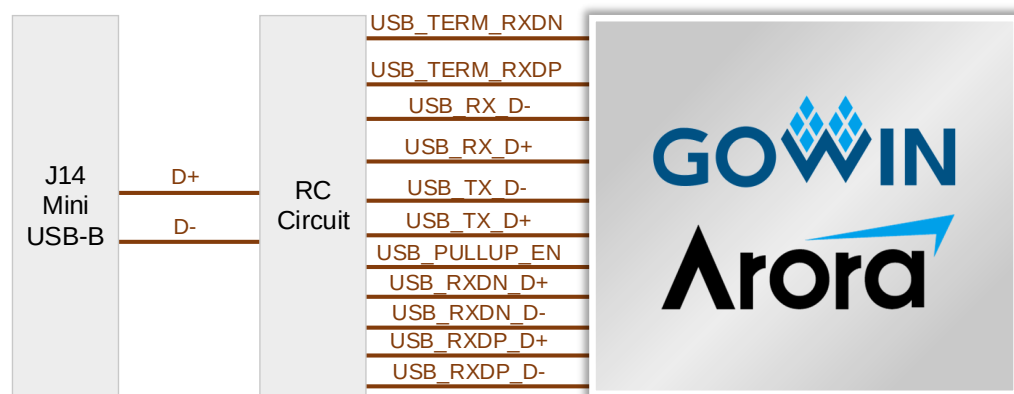
J254 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	VCCIO2+	-	-	2.5V	Power
2	VCCIO2+	-	-	2.5V	Power
3	HGPIO1	W21	2	2.5V	GPIO
4	HGPIO2	Y21	2	2.5V	GPIO
5	HGPIO3	V19	2	2.5V	GPIO
6	HGPIO4	W24	2	2.5V	GPIO
7	HGPIO5	AC26	2	2.5V	GPIO
8	HGPIO6	V18	2	2.5V	GPIO
9	HGPIO7	AB26	2	2.5V	GPIO
10	HGPIO8	AA25	2	2.5V	GPIO
11	HGPIO9	Y26	2	2.5V	GPIO
12	HGPIO10	Y25	2	2.5V	GPIO
13	HGPIO11	W26	2	2.5V	GPIO
14	HGPIO12	W25	2	2.5V	GPIO
15	HGPIO13	V26	2	2.5V	GPIO
16	HGPIO14	V24	2	2.5V	GPIO
17	HGPIO15	U26	2	2.5V	GPIO
18	HGPIO16	U25	2	2.5V	GPIO
19	GND	-	-	-	GND
20	GND	-	-	-	GND

3.13 USB 2.0 Interface

3.13.1 Introduction

The development board leads the USB 2.0 interface through the Mini USB-B connector and includes the ESD protection circuit for communication between the FPGA and external devices. The connection diagram of USB2.0 interface is shown in Figure 3-12.

Figure 3-12 Connection Diagram of USB2.0 Interface.



3.13.2 Pin Distribution

Table 3-14 Pin Distribution of USB2.0 Interface

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
USB_TERM_RXDP	G22	4	3.3V	Terminal resistance control at high speed, used as USB data pin at full speed and low speed
USB_TERM_RXDN	F22	4	3.3V	Terminal resistance control at high speed, used as USB data pin at full speed and low speed
USB_RX_D+	M16	4	3.3V	USB data pin at high speed
USB_RX_D-	M17	4	3.3V	USB data pin at high speed
USB_TX_D+	K16	4	3.3V	USB data pin at high speed
USB_TX_D-	K17	4	3.3V	USB data pin at high speed
USB_PULLUP_EN	M14	4	3.3V	Pull-up
USB_RXDN_D+	K22	4	3.3V	USB- signal

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
USB_RXDN_D-	K23	4	3.3V	USB- reference signal
USB_RXDP_D+	F23	4	3.3V	USB+ signal
USB_RXDP_D-	E23	4	3.3V	USB+ reference signal

3.14 HDMI Interface

3.14.1 Introduction

The development board leads one HDMI input interface and one HDMI output interface. The input and output communication is implemented via the decoding and encoding chips, respectively. The connection diagram of HDMI interface is as follows.

Figure 3-13 Connection Diagram of HDMI_TX Interface

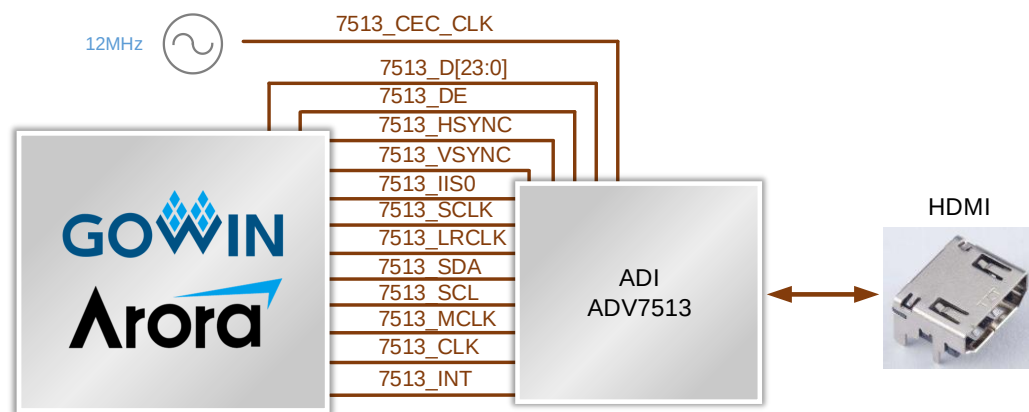
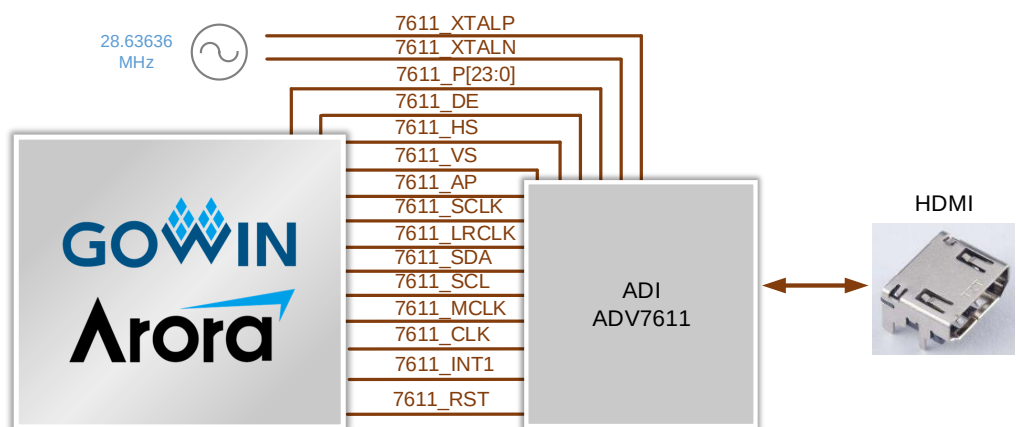


Figure 3-14 Connection Diagram of HDMI_RX Interface



3.14.2 Pin Distribution

Table 3-15 Pin Distribution of HDMI_TX Interface

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
7513_CLK	K21	4	3.3V	The output clock for RGB row locking
7513_D0	K20	4	3.3V	RGB data signal
7513_D1	L19	4	3.3V	RGB data signal
7513_D2	L18	4	3.3V	RGB data signal
7513_D3	J24	4	3.3V	RGB data signal
7513_D4	J26	4	3.3V	RGB data signal
7513_D5	J25	4	3.3V	RGB data signal
7513_D6	H26	4	3.3V	RGB data signal
7513_D7	G26	4	3.3V	RGB data signal
7513_D8	E26	4	3.3V	RGB data signal
7513_D9	E25	4	3.3V	RGB data signal
7513_D10	D26	4	3.3V	RGB data signal
7513_D11	D25	4	3.3V	RGB data signal
7513_D12	G24	4	3.3V	RGB data signal
7513_D13	F24	4	3.3V	RGB data signal
7513_D14	J20	4	3.3V	RGB data signal
7513_D15	J19	4	3.3V	RGB data signal
7513_D16	G20	4	3.3V	RGB data signal
7513_D17	H19	4	3.3V	RGB data signal
7513_D18	K18	4	3.3V	RGB data signal
7513_D19	H18	4	3.3V	RGB data signal
7513_D20	J18	4	3.3V	RGB data signal
7513_D21	J16	4	3.3V	RGB data signal
7513_D22	K15	4	3.3V	RGB data signal
7513_D23	J15	4	3.3V	RGB data signal
7513_VSYNC	M15	4	3.3V	Vertical synchronization signal

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
7513_HSYNC	L15	4	3.3V	Horizontal synchronization signal
7513_DE	L14	4	3.3V	RGB data enable
7513_SCLK	G21	4	3.3V	IIS interface SCLK
7513_LRCLK	J21	4	3.3V	IIS interface LRCLK
7513_MCLK	H21	4	3.3V	IIS interface MCLK
7513_IIS0	H22	4	3.3V	IIS interface data signal
7513_SCL	G25	4	3.3V	I2C serial interface clock
7513_SDA	F25	4	3.3V	I2C serial interface data
7513_INT	J14	4	3.3V	Interrupt signal

Table 3-16 Pin Distribution of HDMI_RX Interface

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
7611_CLK	D18	5	3.3V	The output clock for RGB row locking
7611_P0	D16	5	3.3V	RGB data signal
7611_P1	C26	5	3.3V	RGB data signal
7611_P2	B26	5	3.3V	RGB data signal
7611_P3	B25	5	3.3V	RGB data signal
7611_P4	A25	5	3.3V	RGB data signal
7611_P5	B24	5	3.3V	RGB data signal
7611_P6	A23	5	3.3V	RGB data signal
7611_P7	B22	5	3.3V	RGB data signal
7611_P8	A22	5	3.3V	RGB data signal
7611_P9	B20	5	3.3V	RGB data signal
7611_P10	A20	5	3.3V	RGB data signal
7611_P11	B19	5	3.3V	RGB data signal
7611_P12	A19	5	3.3V	RGB data signal
7611_P13	A18	5	3.3V	RGB data signal
7611_P14	B17	5	3.3V	RGB data signal
7611_P15	A17	5	3.3V	RGB data signal

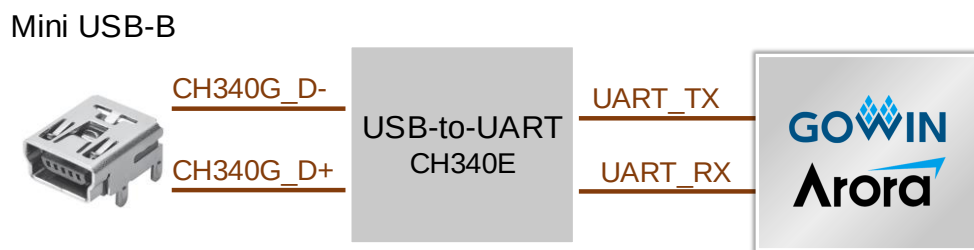
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
7611_P16	D21	5	3.3V	RGB data signal
7611_P17	C22	5	3.3V	RGB data signal
7611_P18	E21	5	3.3V	RGB data signal
7611_P19	C23	5	3.3V	RGB data signal
7611_P20	C24	5	3.3V	RGB data signal
7611_P21	D23	5	3.3V	RGB data signal
7611_P22	D24	5	3.3V	RGB data signal
7611_P23	E22	5	3.3V	RGB data signal
7611_VS	E18	5	3.3V	Vertical synchronization signal
7611_HS	C17	5	3.3V	Horizontal synchronization signal
7611_DE	E16	5	3.3V	RGB data enable
7611_SCLK	E20	5	3.3V	IIS interface SCLK
7611_LRCLK	C19	5	3.3V	IIS interface LRCLK
7611_MCLK	D19	5	3.3V	IIS interface MCLK
7611_AP	B21	5	3.3V	Audio input pin
7611_SCL	H16	5	3.3V	I2C serial interface clock
7611_SDA	G16	5	3.3V	I2C serial interface data
7611_INT1	C21	5	3.3V	Interrupt signal
7611_RST	D20	5	3.3V	System Reset

3.15 UART Interface

3.15.1 Introduction

The UART interface led from the development board uses Mini USB-B connector, which is implemented via USB conversion chips. The connection diagram of UART interface is shown in Figure 3-15.

Figure 3-15 Connection Diagram of UART Interface.



3.15.2 Pin Distribution

Table 3-17 Pin Distribution of UART Interface

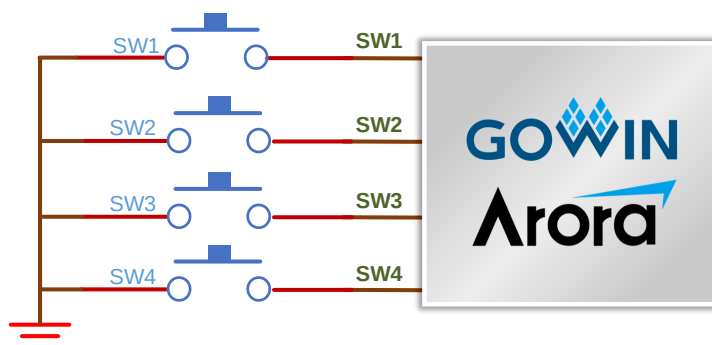
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
UART_TX	R17	3	3.3V	Transmit data
UART_RX	R16	3	3.3V	Receive data

3.16 Key & Indicator

3.16.1 Introduction

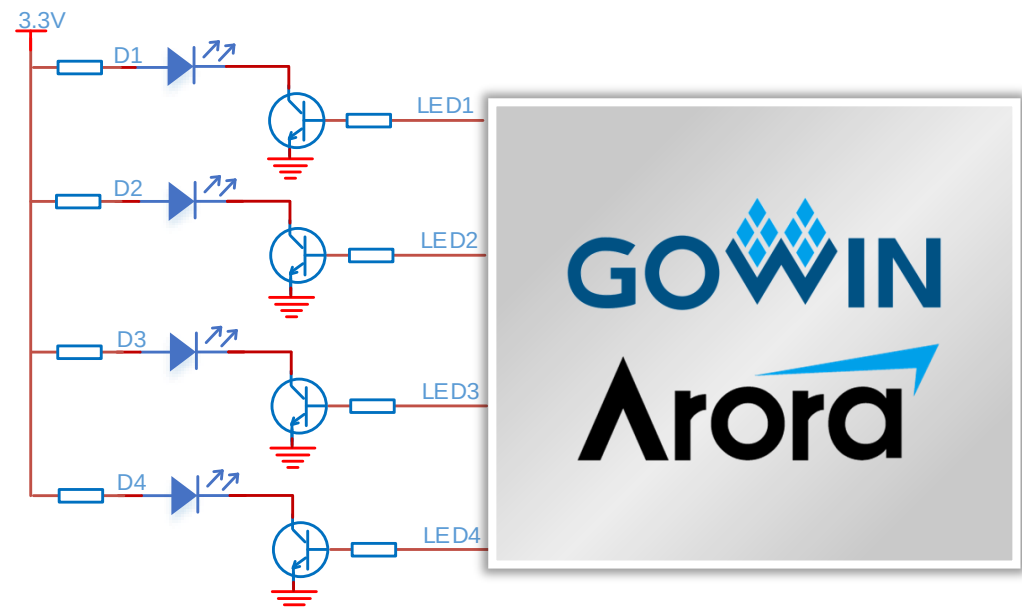
The development board includes four user keys which are connected to the general IO of FPGA BANK2 and BANK3. The corresponding IO input voltage of the FPGA is low when the key is pressed while high when the key is not pressed. The connection diagram is as follows.

Figure 3-16 Connection Diagram of Key



The development board includes four user LEDs. The user LEDs are connected to the IO of FPGA BANK3 and can be switched on and off via the program. The user LEDs will be on when the IO voltage is high. The user LEDs will be off when the IO voltage is low. The connection diagram is shown in Figure 3-17.

Figure 3-17 Connection Diagram of LED



3.16.2 Pin Distribution

Table 3-18 Pin Distribution of Key

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
SW1	N16	3	3.3V	Key
SW2	U17	2	2.5V	Key
SW3	U24	2	2.5V	Key
SW4	V14	2	2.5V	Key

Table 3-19 Pin Distribution of LED Indicator

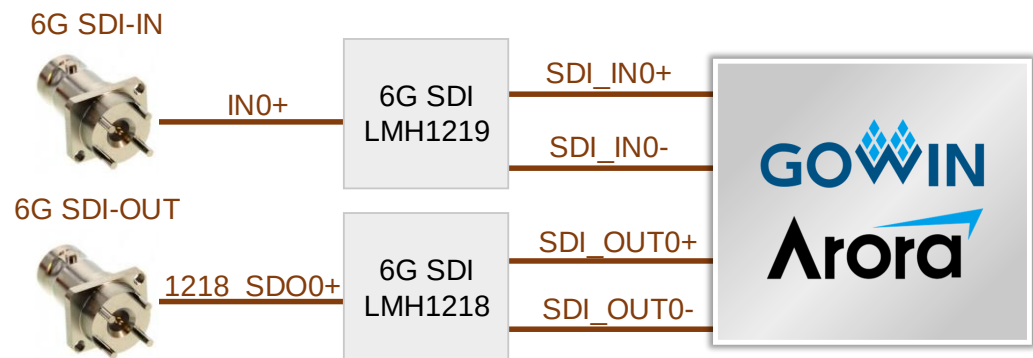
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
LED1	R21	3	3.3V	LED
LED2	M19	3	3.3V	LED
LED3	P23	3	3.3V	LED
LED4	P24	3	3.3V	LED

3.17 6G SDI Interface

3.17.1 Introduction

The development board includes 6G SDI interfaces with transmitters and receivers. The SDI-IN interface receives serial data via one BNC female; the SDI-OUT interface sends the processed serial data via one BNC female. The design diagram of 6G SDI interface is shown in Figure 3-18.

Figure 3-18 Connection Diagram of 6G SDI Interface



3.17.2 Pin Distribution

Table 3-20 Pin Distribution of 6G SDI Interface

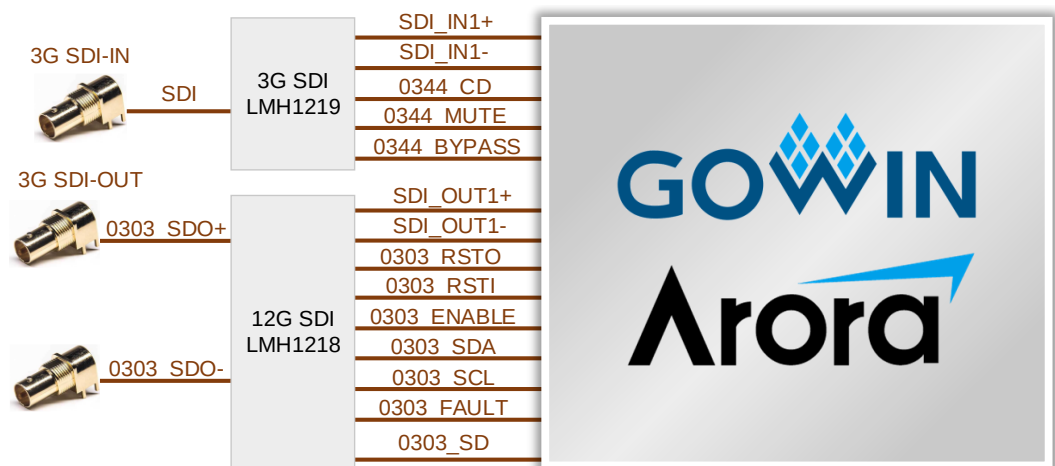
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
SDI_IN0+	AC14	Q1	--	SDI+ input
SDI_IN0-	AD14	Q1	--	SDI- input
SDI_OUT0+	AC8	Q1	--	SDI+ output
SDI_OUT0-	AD8	Q1	--	SDI- output

3.18 3G SDI Interface

3.18.1 Introduction

The development board includes 3G SDI interfaces with transmitters and receivers. The SDI-IN interface receives serial data via one BNC female; the SDI-OUT interface sends the processed serial data via two BNC females. The design diagram of 3G SDI interface are shown in Figure 3-19.

Figure 3-19 Connection Diagram of 3G SDI Interface



3.18.2 Pin Distribution

Table 3-21 Pin Distribution of 3G SDI-IN Interface

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
SDI_IN1+	AE13	Q1	--	SDI+ input
SDI_IN1-	AF13	Q1	--	SDI- input
0344_CD	N24	3	3.3V	Carrier detection
0344_BYPASS	N22	3	3.3V	Bypass signal
0344_MUTE	M20	3	3.3V	Output mute

Table 3-22 Pin Distribution of 3G SDI-OUT Interface

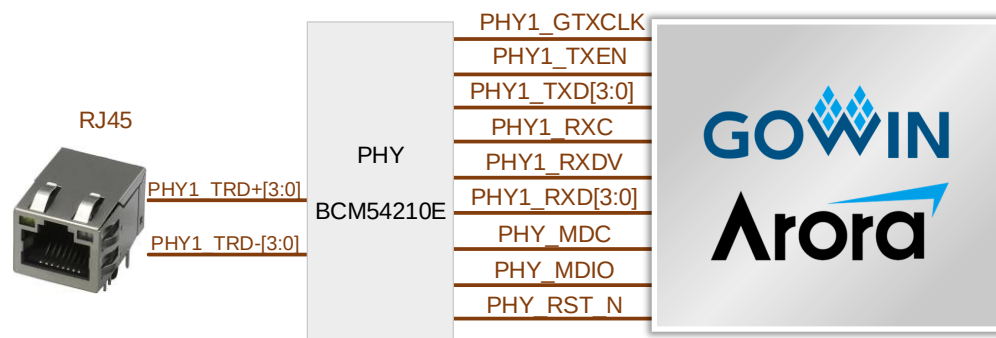
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
SDI_OUT1+	AE9	Q1	--	SDI+ output
SDI_OUT-	AF9	Q1	--	SDI- output
0303_SCL	L22	3	3.3V	SMBus clock signal
0303_SDA	L23	3	3.3V	SMBus Bidirectional data signal
0303_ENABLE	M24	3	3.3V	Output driver enable
0303_RSTI	L20	3	3.3V	Reset input
0303_SD	M25	3	3.3V	Standard definition
0303_RSTO	L25	3	3.3V	Reset output
0303_FAULT	L24	3	3.3V	Error signal

3.19 Ethernet Interface

3.19.1 Introduction

The development board provides 1-channel Ethernet interface, supporting RGMII (10BASE-T/100BASE-TX/1000BASE-T) interfaces. Use the RJ45 connector integrated with network transformer internally. The connection diagram is shown in Figure 3-20.

Figure 3-20 Ethernet Interface Connection Diagram



3.19.2 Pin Distribution

Table 3-23 Ethernet Interface Pin Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
PHY1_RXC	C18	5	3.3V	RGMII receive clock
PHY1_GTXCLK	A24	5	3.3V	RGMII transmit clock
PHY1_RXDV	G19	5	3.3V	RGMII receive data valid
PHY1_RXD3	F20	5	3.3V	RGMII receive data
PHY1_RXD2	F18	5	3.3V	RGMII receive data
PHY1_RXD1	F19	5	3.3V	RGMII receive data
PHY1_RXD0	F17	5	3.3V	RGMII receive data
PHY1_TXEN	H15	5	3.3V	RGMII transmit enable
PHY1_TXD3	G15	5	3.3V	RGMII transmit data
PHY1_TXD2	H14	5	3.3V	RGMII transmit data
PHY1_TXD1	E17	5	3.3V	RGMII transmit data
PHY1_TXD0	F15	5	3.3V	RGMII transmit data
PHY_MDC	N18	3	3.3V	Management data clock

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
PHY_MDIO	R18	3	3.3V	Management data I/O
PHY_RST_N	N23	3	3.3V	Reset

