



Gowin UHS2 PSRAM Memory Interface IP

User Guide

IPUG1194-1.1E, 2025-03-07

Copyright © 2025 Guangdong Gowin Semiconductor Corporation. All Rights Reserved.

GOWIN高云, **GOWIN**, , GOWINSEMI, GOWIN, Gowin, 高云, 晨熙, 小蜜蜂, LittleBee, , GowinPnR, GoBridge are trademarks of Guangdong Gowin Semiconductor Corporation and are registered in China and/or other countries or regions. All other words and logos identified as trademarks or service marks are the property of their respective holders. No part of this document may be reproduced or transmitted in any form or by any means, electronic, mechanical, photocopying, recording or otherwise, without the prior written consent of GOWINSEMI.

Disclaimer

GOWINSEMI assumes no liability and provides no warranty (either expressed or implied) and is not responsible for any damage incurred to your hardware, software, data, or property resulting from usage of the materials or intellectual property except as outlined in the GOWINSEMI Terms and Conditions of Sale. GOWINSEMI may make changes to this document at any time without prior notice. Anyone relying on this documentation should contact GOWINSEMI for the current documentation and errata.

Revision History

Date	Version	Description
11/22/2024	1.0E	Initial version published.
03/07/2025	1.1E	• Descriptions of 4 Functional Description updated. • Descriptions of 6 Parameter Configuration updated. • Descriptions of 7 Interface Configuration updated.

Contents

List of Figures.....	iii
List of Tables.....	iv
1 About This Guide.....	1
1.1 Purpose.....	1
1.2 Related Documents.....	1
1.3 Terminology and Abbreviations.....	2
1.4 Support and Feedback.....	2
2 Overview.....	3
3 Features and Performance.....	4
3.1 Features.....	4
3.2 Operating Frequency and Bandwidth Efficiency.....	4
3.3 Resource Utilization.....	4
4 Functional Description.....	5
4.1 Structure.....	5
4.2 MC.....	6
4.3 PHY.....	7
4.3.1 Init Module.....	7
4.3.2 Data_Channel.....	7
4.3.3 CMD/ADDR_Ctr_Ch.....	8
4.3.4 I/O_Logic.....	8
4.4 Functions and User Interface.....	8
4.4.1 Initialization.....	8
4.4.2 Send Addresses, Commands, and burst_num.....	8
4.4.3 Write Data.....	10
4.4.4 Read Data.....	11
4.4.5 Self-refresh Mode.....	11
4.4.6 Half-sleep Mode.....	12
5 Port List.....	13
6 Parameter Configuration.....	16
6.1 Parameter Description.....	16

6.1.1 Wrap Enable, Wrap Length , Auto-precharge, and PRA Enable.....	17
6.1.2 Configuration 1 and Configuration 2.....	17
6.1.3 Configuration 3 and Configuraiton 4.....	18
6.1.4 Configuration 5/6/7/8.....	19
6.2 Clock Phase Setting Parameter1 Value.....	20
7 Interface Configuration.....	22
7.1 IP Configuration.....	22
7.2 VCCX Voltage Configuration.....	26
8 Reference Design.....	28
9 File Delivery.....	30
9.1 Document.....	30
9.2 Reference Design.....	30

List of Figures

Figure 4-1 Gowin UHS2 PSRAM Memory Interface IP Structure Diagram.....	5
Figure 4-2 MC Structure Diagram.....	6
Figure 4-3 PHY Structure Diagram.....	7
Figure 4-4 Initialization Completion Signal Timing Diagram.....	8
Figure 4-5 Timing Diagram for Commands and Addresses.....	9
Figure 4-6 Write Data Port Timing Diagram.....	10
Figure 4-7 Timing Diagram Between Data Mask and Read/Write Data.....	11
Figure 4-8 Read Data Port Timing Diagram.....	11
Figure 4-9 Timing Diagram for Self-refresh Mode Request and Response.....	12
Figure 4-10 Timing Diagram for Half-sleep Mode Request and Response.....	12
Figure 6-1 Initial Phase Relationship Diagram of O_apsram_ck and IO_apsram_dqs.....	21
Figure 6-2 Add dll_step Signal to GAO.....	21
Figure 6-3 View the Value of dll_step.....	21
Figure 7-1 Open IP Core Generator.....	22
Figure 7-2 Open UHS2 PSRAM Memory Interface IP Core.....	23
Figure 7-3 IP Options.....	26
Figure 7-4 VCCX Configuration Interface.....	27
Figure 8-1 Reference Design Block Diagram.....	28

List of Tables

Table 1-1 Terminology and Abbreviations.....	2
Table 2-1 Gowin UHS2 PSRAM Memory Interface.....	3
Table 3-1 Resource Utilization.....	4
Table 4-1 User Interface Address and PSRAM Address Mapping.....	9
Table 4-2 cmd.....	9
Table 5-1 I/O Port List of Gowin UHS2 PSRAM Memory Interface IP.....	13
Table 6-1 Static Parameter Options of Gowin UHS2 PSRAM Memory Interface.....	16
Table 6-2 Burst Types for Array linear write/read and Array write/read Commands.....	18
Table 6-3 Burst Types for Array Read and Array Linear Read Commands.....	19
Table 6-4 Burst Types for Array Read Commands.....	20
Table 8-1 Input Port List.....	29
Table 9-1 Document List.....	30
Table 9-2 Ref.design Folder Content List.....	30

1 About This Guide

1.1 Purpose

The purpose of Gowin UHS2 PSRAM Memory Interface IP User Guide is to help you quickly learn the features and usage of Gowin UHS2 PSRAM Memory Interface IP by providing the descriptions of the functions, ports, timing, GUI, and reference design. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.11.01. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at www.gowinsemi.com:

- [SUG100, Gowin Software User Guide](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1118, GW5ART series of FPGA Products Data Sheet](#)
- [UG1120, GW5ART-15 Pinout](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in [Table 1-1](#).

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
ALU	Arithmetic Logical Unit
IP	Intellectual Property
LUT	Look-up Table
MR	Mode Register
PSRAM	Pseudo Static Random Access Memory
RAM	Random Access Memory

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

The PSRAM memory part number that can be accessed by Gowin UHS2 PSRAM Memory Interface IP is AP26408A-OKX. This IP consists of two parts: Memory Controller Logic (MC) and Physical Interface (PHY), providing users with command interfaces. It interconnects with AP26408A-OKX to fulfill users' memory access requirements.

Table 2-1 Gowin UHS2 PSRAM Memory Interface

Gowin UHS2 PSRAM Memory Interface IP	
Logic Resource	Please refer to Table 3-1 .
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (1.9.10.03 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

3 Features and Performance

3.1 Features

- The supported PSRAM memory part number is AP26408A-OKX with data width of 8 bits.
- Supports Array write/read and Array linear write/read modes
- Supports fixed and variable bursts; the fixed burst lengths are 16B, 32B, 64B, and 128B; the variable burst lengths range from 8B to 2048B.
- The ratio of IP system master clock to PSRAM interface clock is 1:4.
- Supports initial READ_WRITE latency: 24_12/20_10/16_6/13_5/9_5.
- Supports Self-refresh mode
- Supports Half-sleep mode
- Configurable driving strength
- Configurable Trim value for decision level
- The maximum operating rate is 1066 Mbps.

3.2 Operating Frequency and Bandwidth Efficiency

- The maximum data rate for the current version is 1066 Mbps.
- The larger the burst length, the higher the bandwidth efficiency; at a burst length of 2048B, the efficiency can reach up to 92%.

3.3 Resource Utilization

Gowin UHS2 PSRAM Memory Interface IP is implemented by Verilog. When GW5AR-LV25UG256P is selected, its resource utilization is as shown in [Table 3-1](#).

Table 3-1 Resource Utilization

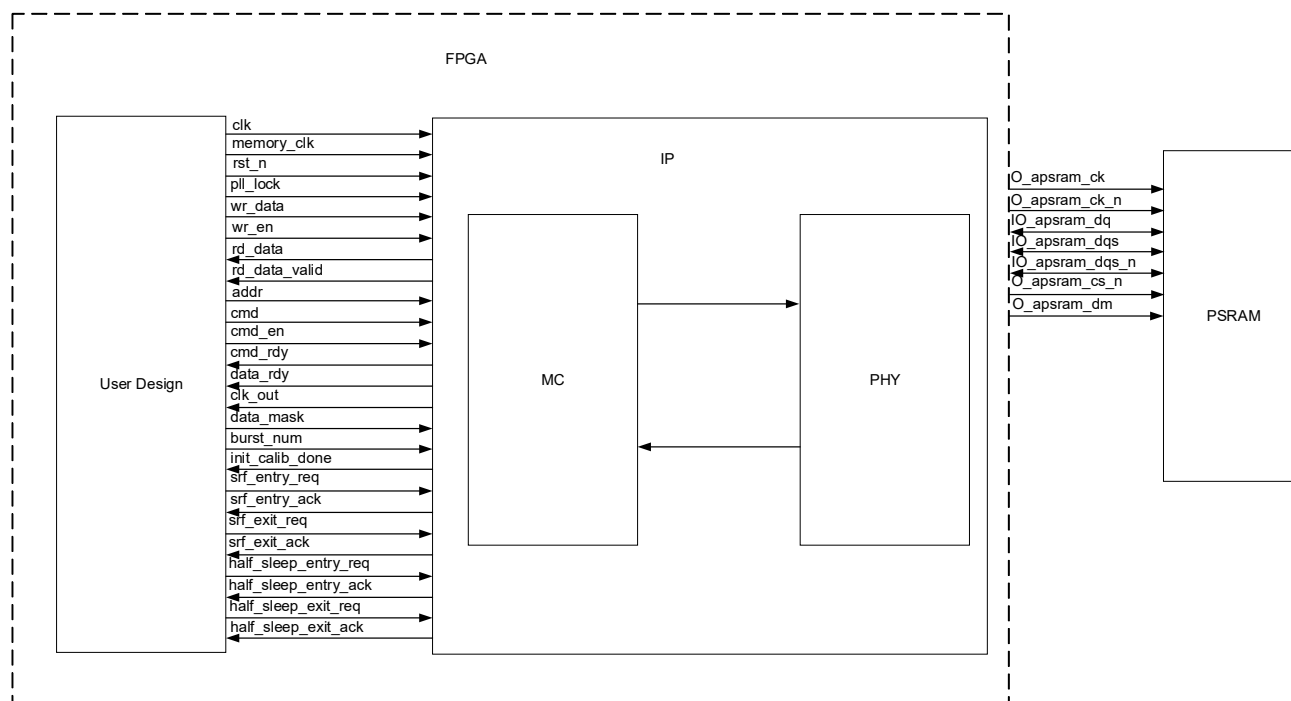
FPGA	REGs	LUT	ALU	BSRAM
GW5AR-LV25UG256P	1266	1277	43	4

4 Functional Description

4.1 Structure

The structure of Gowin UHS2 PSRAM Memory Interface IP is as shown in [Figure 4-1](#), consisting of modules such as Memory Controller Logic (MC) and Physical Interface (PHY). The "User Design" in the diagram refers to the user design that complies with the IP user-side interface protocol.

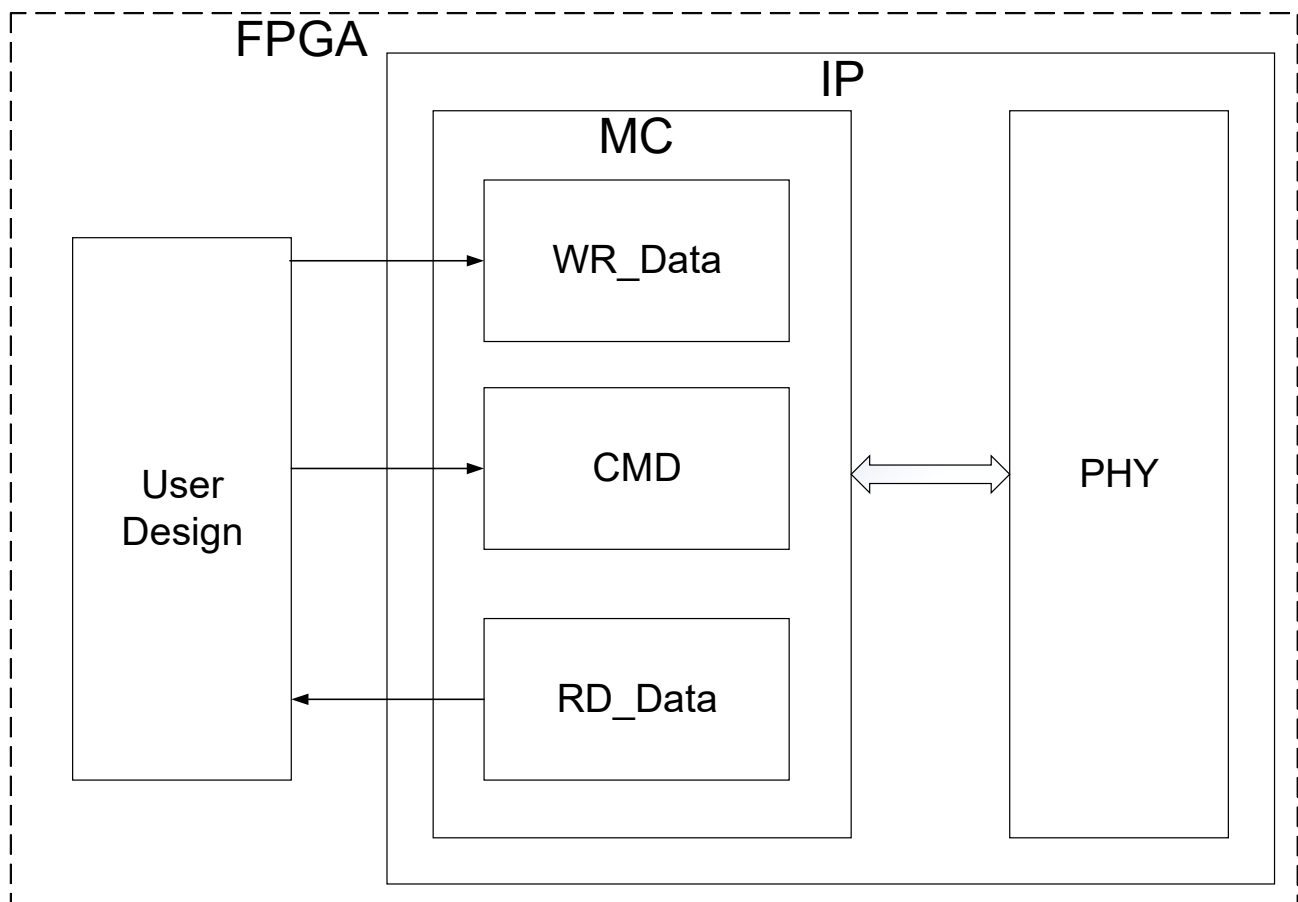
Figure 4-1 Gowin UHS2 PSRAM Memory Interface IP Structure Diagram



4.2 MC

MC is the Controller of the IP, composed of modules such as CMD (command), WR_Data (write data), and RD_Data (read data). CMD and WR_Data receive and buffer commands and data from the user, and send the processed commands and data to the PHY. RD_Data receives the data returned from the PHY and outputs it to the user. The structure of MC is as shown in [Figure 4-2](#).

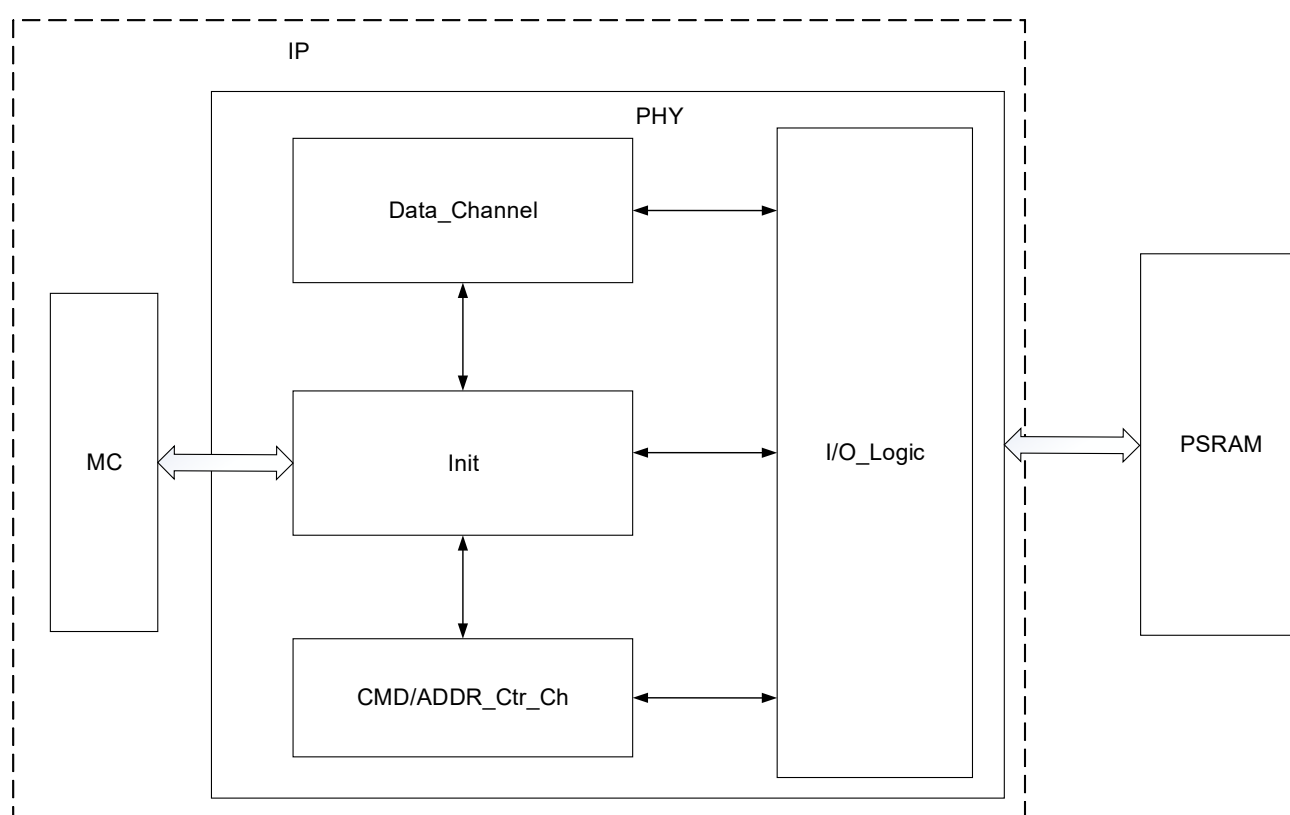
Figure 4-2 MC Structure Diagram



4.3 PHY

The PHY layer is used to connect the MC layer with the PSRAM chip. Its basic structure is shown in [Figure 4-3](#), including four modules: Init (initialization), Data_Channel (data channel), CMD/ADDR_Ctr_Ch (command/address control channel), and I/O_Logic (input/output logic). During write operations, the PHY receives command and data from the MC, processes the data logically, and then transmits it to the PSRAM chip. During read operations, the PHY receives the data returned from the PSRAM, processes it logically, and then transmits it to the MC layer.

Figure 4-3 PHY Structure Diagram



4.3.1 Init Module

The Init module is used to handle the initialization of PSRAM after power on, including PSRAM reset, MR configuration, and read calibration. The signal "init_calib_done" transitions from low to high to indicate the completion of initialization. Users should wait until the init_calib_done signal is asserted (high) before accessing the IP.

4.3.2 Data_Channel

The Data_Channel module handles the write and read data channels and performs data reordering for both write and read operations.

4.3.3 CMD/ADDR_Ctr_Ch

The CMD/ADDR_Ctr_Ch module receives commands and addresses from the MC, reorders them, and transmits them to the I/O_Logic module.

4.3.4 I/O_Logic

During write operations, the I/O_Logic module transmits data signals from the Data_Channel and command/address signals from the CMD/ADDR_Ctr_Ch module to the PSRAM using the OSER8 serializer. During read operations, the I/O_Logic module receives data returned from the PSRAM, converts the high-speed serial signals into low-speed parallel signals using the IDES8 deserializer, and transmits them to the Data_Channel module.

4.4 Functions and User Interface

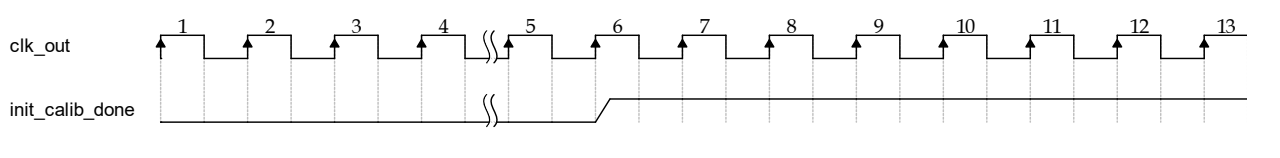
Users can operate the IP through the user interface signals to perform the following functions::

- Initialization
- Sends addresses, commands and burst_num
- Writes data
- Reads data
- Supports self-refresh mode
- Supports half-sleep mode

4.4.1 Initialization

After power on, the PHY first performs initialization on the PSRAM. As shown in [Figure 4-4](#), the "init_calib_done" signal is pulled high to indicate that initialization is complete, after which the user can access the IP normally.

Figure 4-4 Initialization Completion Signal Timing Diagram



4.4.2 Send Addresses, Commands, and burst_num

Users can send addresses, read/write commands, and specify the burst length for write data (wr_data) through the addr, cmd, cmd_en, and burst_num interfaces.

- addr: The addr port specifies the starting address for each burst access. It becomes valid when cmd_en is asserted (high).

addr is a byte address and maps to the PSRAM's row and column addresses. For a 64Mb (8Mx8bits) PSRAM, the mapping is as shown in [Table 4-1](#).

Table 4-1 User Interface Address and PSRAM Address Mapping

User Interface Address	PSRAM Address
addr[22:11]	Row address
addr[10:0]	Column address

The data ratio between the user interface and the PSRAM interface is 1:8. For example, if the PSRAM data width is 8 bits, then the user interface data width is 8 bits $\times 8 = 64$ bits. When writing a single user interface data unit, 8 bytes are written to the PSRAM, occupying 8 address locations. As a result, bits [2:0] of the address remain 0 at all times.

When performing burst access, the user must calculate the address for each burst access. For sequential address burst access, the address increments by $(\text{burst_num} + 1) \times 8$. It is important to note that the address must not cross a 2KB boundary.

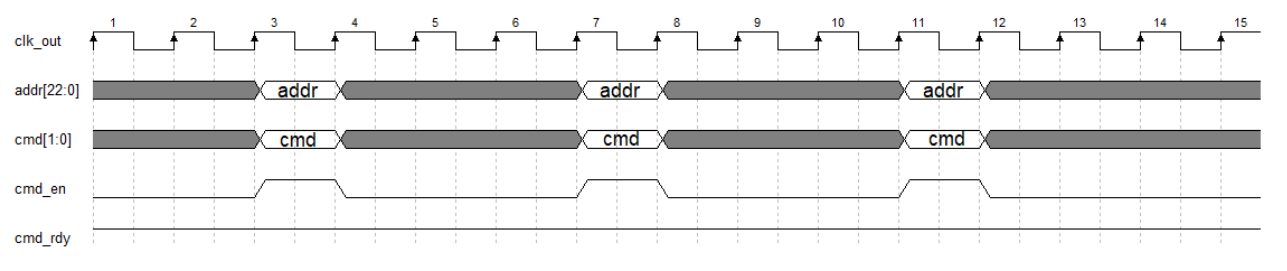
- cmd: cmd is the command port for read or write operations. When cmd_en is 1, cmd is valid. cmd can be configured as array linear read, array linear write, array read, or array write modes, as shown in [Table 4-2](#).

Table 4-2 cmd

Write/Read Mode	cmd[1:0]
array linear read	2'b00
array read	2'b10
array linear write	2'b01
array write	2'b11

- cmd_en: cmd_en is the enable signal for the address, command, and burst_num. It is active high. When cmd_en = 1'b1, cmd, addr, and burst_num are valid, as shown in [Figure 4-5](#). When cmd_rdy = 1'b1, the user can write cmd_en, addr, cmd, and burst_num.

Figure 4-5 Timing Diagram for Commands and Addresses



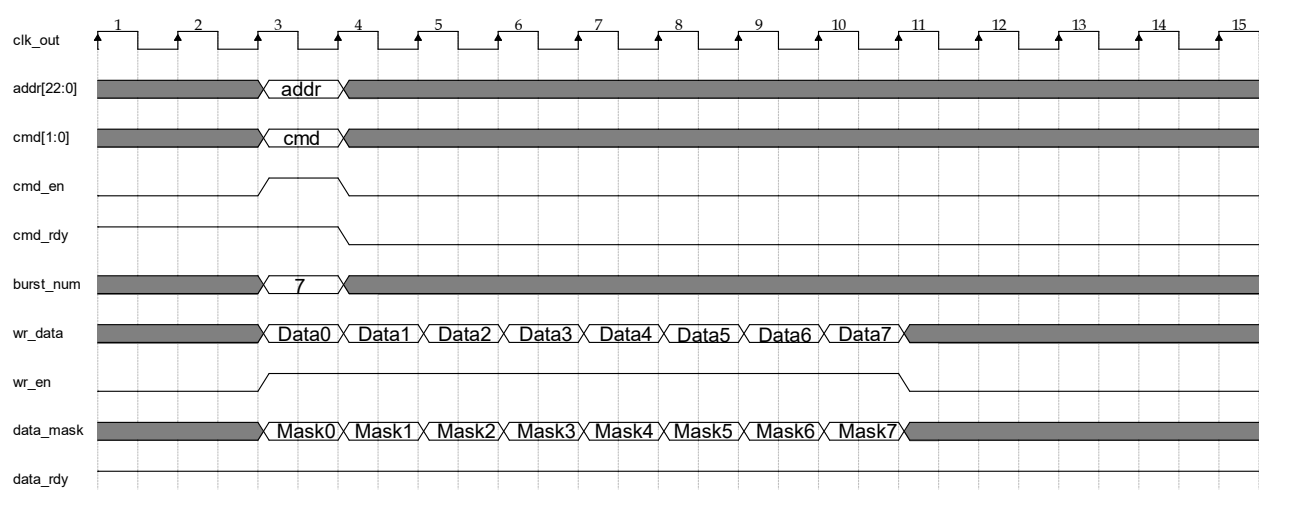
- **burst_num**: burst_num represents the number of wr_data or rd_data for the current burst access. When cmd_en = 1, burst_num is valid. The actual number of wr_data written or rd_data read is burst_num + 1.

4.4.3 Write Data

Users can write data to the IP through the wr_data, wr_en, and data_mask ports. The timing is shown in [Figure 4-6](#).

- wr_data is the write data port. When wr_en is 1, wr_data is valid.
- wr_en is the write enable port, active high.
- data_mask is the mask signal for wr_data, active high.

Figure 4-6 Write Data Port Timing Diagram



When data_rdy is 1, wr_en should be set to 1 to sequentially write wr_data and wr_mask. As shown in [Figure 4-6](#), when burst_num = 7, a total of 8 wr_data must be written continuously.

Data Mask (data_mask)

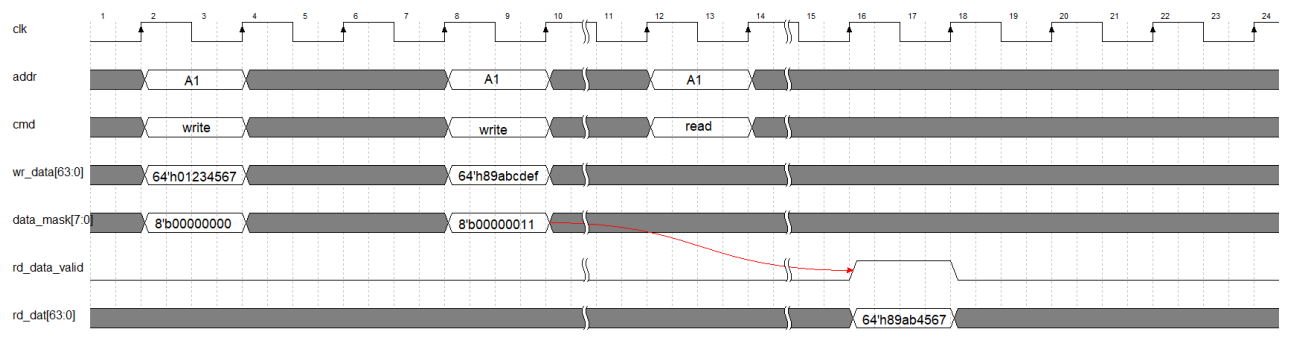
For data that the user does not need, the data mask signal (data_mask) can be used for masking. Each bit in data_mask controls one byte of wr_data. When data_mask[n] = 1'b1, the nth byte of wr_data is masked. The mapping relationship is as follows:

- data_mask[0] controls wr_data[7:0]
- data_mask[1] controls wr_data[15:8]
- data_mask[2] controls wr_data[23:16]
- ... and so on.

As shown in [Figure 4-7](#), the user writes two consecutive frames of data to address A1. In the first frame, no masking is applied, and 64'h01234567 is written. In the second frame, 64'h89abcdef is written with two bytes masked. As a result, when reading from this address,

the returned data is 64'h89ab4567, because `wr_data[15:0] = 16'hcdef` is masked during the write operation, and the 16'hcdef of the current frame will not overwrite the original data when written.

Figure 4-7 Timing Diagram Between Data Mask and Read/Write Data

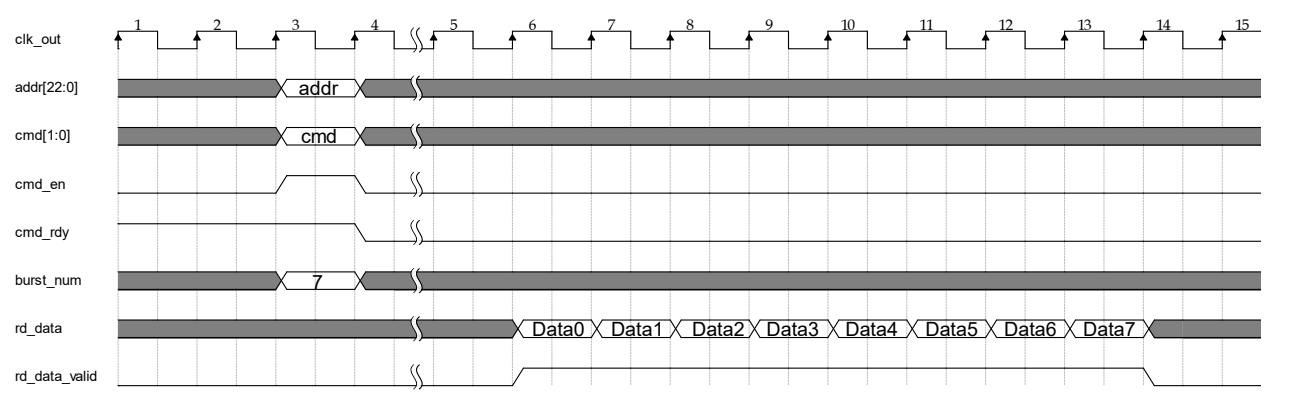


4.4.4 Read Data

The user can read data from PSRAM through the `rd_data` and `rd_data_valid` interface, as shown in [Figure 4-8](#).

- `rd_data`: Read data port.
- `rd_data_valid`: Read data valid port. When `rd_data_valid` is high, `rd_data` is valid.

Figure 4-8 Read Data Port Timing Diagram



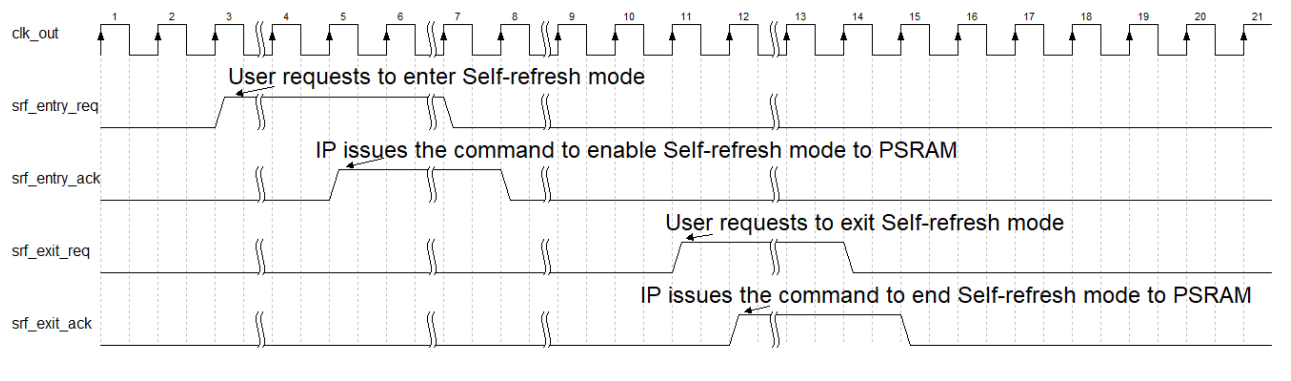
Each time data is read, `rd_data_valid` is always returned continuously without interruption.

4.4.5 Self-refresh Mode

Self-refresh is a power-saving mode of PSRAM. When the user inputs "`srf_entry_req=1'b1`", the IP sends a command to PSRAM to enter Self-refresh mode while simultaneously providing feedback to the user with "`srf_entry_ack=1'b1`". After that, PSRAM enters Self-refresh mode. In this mode, internal data is retained but no read or write commands are received. If the user needs to perform read or write operations on

PSRAM, they must exit Self-refresh mode. To exit, the user can input "srf_exit_req=1'b1", and once the IP responds with "srf_exit_ack=1'b1", the mode exits, as shown in [Figure 4-9](#).

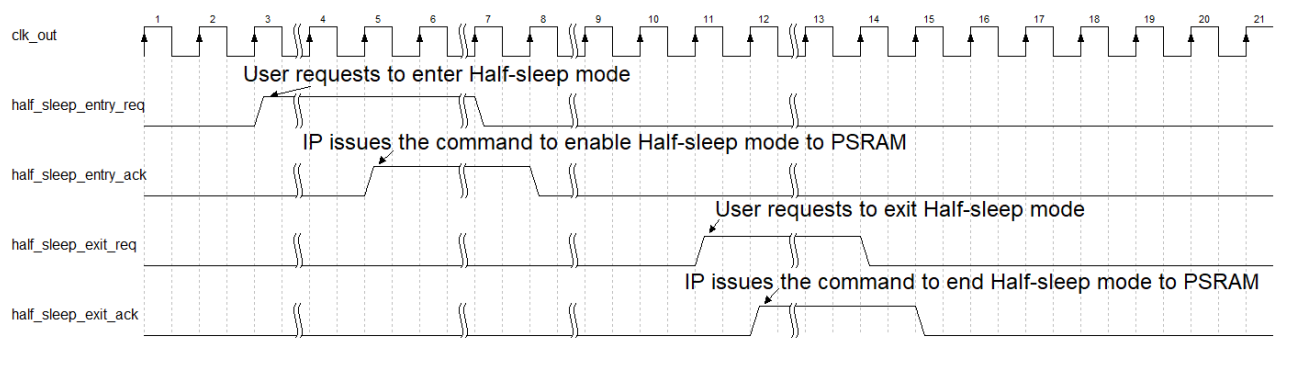
Figure 4-9 Timing Diagram for Self-refresh Mode Request and Response



4.4.6 Half-sleep Mode

When the user inputs "half_sleep_entry_req = 1'b1", the IP sends a command to PSRAM to enter Half-sleep mode while simultaneously providing feedback to the user with "half_sleep_entry_ack = 1'b1". In this mode, PSRAM groups refresh operations together and shuts down most circuits when not refreshing, consuming less power (with lower power consumption than Self-refresh mode). To exit this mode, the user can input "half_sleep_exit_req = 1'b1", and once the IP responds with "half_sleep_exit_ack = 1'b1", the mode will exit, as shown in [Figure 4-10](#).

Figure 4-10 Timing Diagram for Half-sleep Mode Request and Response



5 Port List

The I/O ports of Gowin UHS2 PSRAM Memory Interface IP are shown in [Table 5-1](#).

Table 5-1 I/O Port List of Gowin UHS2 PSRAM Memory Interface IP

Signal	Data Width	I/O	Description
User Interface			
addr	ADDR_WIDTH	Input	Read/write start address
cmd	2	Input	Read/write command
cmd_en	1	Input	The flag bit that allows writing cmd, addr, and burst_num 0: Commands cannot be written 1: Commands can be written
cmd_rdy	1	Output	cmd ready to write 0: Command cannot be written 1: Command can be written
rd_data	8*DQ_WIDTH	Output	Read data channel
rd_data_valid	1	Output	rd_data valid signal 0: Invalid 1: Valid
wr_data	8*DQ_WIDTH	Input	Write data channel
wr_en	1	Input	wr_data enable signal 0: Data invalid 1: Data valid
data_rdy	1	Output	wr_data ready to write 0: Data cannot be written 1: Data can be written
data_mask	MASK_WIDTH	Input	wr_data mask signal

Signal	Data Width	I/O	Description
data_mask	MASK_WIDTH	Input	0: Invalid 1: Valid
clk	1	Input	Reference clock input, which is a continuous clock that can be either an on-board crystal oscillator clock or a PLL output clock.
init_calib_done	1	Output	Initialization completed signal
clk_out	1	Output	IP system clock, with a frequency of 1/4 of memory_clk.
rst_n	1	Input	User input reset signal 0: Reset 1: Release reset
memory_clk	1	Input	The working clock for PSRAM, provided by the user, is typically a high-speed clock generated by PLL multiplication, or it can be done without a PLL.
pll_lock	1	Input	If memory_clk is PLL frequency multiplication input, this port is connected to PLL's pll_lock pin. If the user does not use PLL, this port is connected to 1'b1.
burst_num	8	Input	Number of wr_data or rd_data in a single burst.
srf_entry_req	1	Input	Self-refresh mode entry request signal 0: Invalid 1: Valid
srf_entry_ack	1	Output	Self-refresh mode entry acknowledge signal 0: Invalid 1: Valid
srf_exit_req	1	Input	Self-refresh mode exit request signal 0: Invalid 1: Valid
srf_exit_ack	1	Output	Self-refresh mode exit acknowledge signal 0: Invalid 1: Valid
half_sleep_entry_req	1	Input	Half-sleep mode entry request signal 0: Invalid

Signal	Data Width	I/O	Description
half_sleep_entry_req	1	Input	1: Valid
half_sleep_entry_ack	1	Output	Half-sleep mode entry acknowledge signal 0: Invalid 1: Valid
half_sleep_exit_req	1	Input	Half-sleep mode exit request signal 0: Invalid 1: Valid
half_sleep_exit_ack	1	Output	Half-sleep mode exit acknowledge signal 0: Invalid 1: Valid
PSRAM Interface			
O_apsram_cs_n	CS_WIDTH	Output	PSRAM interface chip select signal 0: Valid 1: Invalid
O_apsram_ck	CS_WIDTH	Output	PSRAM interface clock positive terminal
O_apsram_ck_n	CS_WIDTH	Output	PSRAM interface clock negative terminal
O_apsram_dm	CS_WIDTH	Output	PSRAM interface data mask signal 0: Invalid 1: Valid
IO_apsram_dq	DQ_WIDTH	Bidirection	PSRAM interface data
IO_apsram_dqs	CS_WIDTH	Bidirection	PSRAM interface data strobe signal (p-side)
IO_apsram_dqs_n	CS_WIDTH	Bidirection	PSRAM interface data strobe signal (n-side)

Note!

- In schematic design, O_apsram_cs_n, O_apsram_dm, IO_apsram_dq, IO_apsram_dqs, and IO_apsram_dqs_n should be placed in the same DQ group.
- During PCB routing, O_apsram_cs_n, O_apsram_dm, IO_apsram_dq, IO_apsram_dqs, IO_apsram_dqs_n, O_apsram_ck, and O_apsram_ck_n need to be routed with equal-length traces.
- When using the GW5ART-LV15MG132P, the pins connecting the FPGA to the PSRAM must be left floating on the PCB, and no pads should be present on the PCB. Otherwise, signal quality may be affected, leading to PSRAM initialization failure. For related pin information, see MG132P description in [UG1120](#), [GW5ART-15 Pinout](#).

6 Parameter Configuration

6.1 Parameter Description

You can configure the static and timing parameters of Gowin UHS2 PSRAM Memory Interface IP according to the design requirements, as shown in the [Table 6-1](#).

Table 6-1 Static Parameter Options of Gowin UHS2 PSRAM Memory Interface

Name	Description	Option
Type Tab		
Memory TYPE	PSRAM type	AP26408A-OKX
CLK Ratio	The ratio of the IP logic master clock to the PSRAM interface clock	1:4, and it cannot be selected by the user.
Memory Clock	PSRAM working clock	100-533 MHz
Psram Width	The DQ width of a single PSRAM memory chip	8, and it cannot be selected by the user.
Dq Width	The total DQ width	When selecting an FPGA with integrated PSRAM, the DQ width supports up to the maximum total DQ width of the integrated PSRAM. When selecting an FPGA without integrated PSRAM, the maximum supported DQ width is 32 bits, which corresponds to four PSRAM chips.
Addr Width	PSRAM address width	23
Row Width	PSRAM row address width	12
Data Width	User data width	8*Dq Width
CS Width	Chip selected width	Dq Width/Psram Width
Mask Width	mask width	Data Width/Psram Width
Simulation	Simulation acceleration button	- You can click this button to accelerate simulation. - Not checked for the board test

Name	Description	Option	
Buffer Type	IP data buffer type	BSRAM, SSRAM, REG	
Option Tab			
Wrap Length	Wrap boundary	16B, 32B, 64B, 128B; for the details, you can see 6.1.1 Wrap Enable, Wrap Length , Auto-precharge, and PRA Enable .	
RW Latency	Read/write latency	R Initial Latency W Initial Latency Max Clock Frequency of PSRAM 24 12 533 MHz 20 10 533 MHz 16 6 400 MHz 13 5 300 MHz 9 5 200 MHz	
PRA Enable	Page Read Access enable	OFF, ON	For the details, you can see 6.1.1 Wrap Enable, Wrap Length , Auto-precharge, and PRA Enable .
Wrap Enable	Wrap enable	OFF, ON	
Auto-precharge	Auto-precharge	OFF, ON	
VREF Trim	Decision level for reading DQ data from the PSRAM chip	60.00, 59.00, 57.90, 56.78, 55.56, 54.28, 52.94, 51.50, 50.00, 48.33, 46.67, 44.83, 42.83, 40.72, 38.44	
Drive Strength	Drive strength	18ohm, 40ohm	
tREFI	Refresh rate	7800000 (7.8us)	
Debug Tab			
Debug Parameter1 Value	Phase shift parameter 1	8'h0~8'hFF, 16'h0~16'hFFFF For the details, you can see 6.2 Clock Phase Setting Parameter1 Value .	

6.1.1 Wrap Enable, Wrap Length , Auto-precharge, and PRA Enable

6.1.2 Configuration 1 and Configuration 2

In the default configuration of the IP GUI, Wrap Enable, Auto-precharge, and PRA are all configured as "OFF." This configuration is assumed to be Configuration 1.

In Configuration 1, both array linear write/read and array write/read commands ignore the Wrap Length configuration and perform sequential bursts. The maximum burst size is 2K Bytes. The read or write operation starts from the starting address and proceeds until the end of the page size, then loops back to the beginning of the current page size. The maximum value for burst_num can be set to 255, and the minimum value can be set to 0.

When Wrap Enable is set to "ON," and Auto-precharge and PRA remain "OFF," this configuration is assumed to be Configuration 2.

In Configuration 2, array linear write/read commands still ignore the Wrap Length configuration and perform sequential bursts with a maximum burst size of 2K Bytes. The read or write operation starts from the starting address and proceeds until the end of the page size, then loops back to the beginning of the current page size. The maximum value for burst_num can be set to 255, and the minimum value can be set to 0.

For array write/read commands, the Wrap Length configuration must be considered. The maximum burst length is determined by the Wrap Length configuration. At this point, burst_num is fixed and set to Wrap Length/8-1. For example, when the Wrap Length is configured as "16B," burst_num should be set to 1.

The burst types for array linear write/read and array write/read commands under Configuration 1 and Configuration 2 are shown in the following table.

Table 6-2 Burst Types for Array linear write/read and Array write/read Commands

PRA	Auto-precharge	Wrap Enable	Wrap Length	Burst Type	Example of bytes sequence(starting address from 8)
OFF	OFF	OFF	16B	NO Wrap,2KB sequential	[8,9,10,...,2047,2047,0,1,...,6,7]
OFF	OFF	OFF	32B	NO Wrap,2KB sequential	[8,9,10,...,2047,2047,0,1,...,6,7]
OFF	OFF	OFF	64B	NO Wrap,2KB sequential	[8,9,10,...,2047,2047,0,1,...,6,7]
OFF	OFF	OFF	128B	NO Wrap,2KB sequential	[8,9,10,...,2047,2047,0,1,...,6,7]
OFF	OFF	ON	16B	Wrap 16B	[8,9,10,...,14,15,0,1,...,6,7]
OFF	OFF	ON	32B	Wrap 16B	[8,9,10,...,30,31,0,1,...,6,7]
OFF	OFF	ON	64B	Wrap 16B	[8,9,10,...,62,63,0,1,...,6,7]
OFF	OFF	ON	128B	Wrap 16B	[8,9,10,...,126,127,0,1,...,6,7]

6.1.3 Configuration 3 and Configuration 4

When Auto-precharge is set to "ON," PRA is set to "OFF," and Wrap Enable is set to "OFF," this mode is assumed to be Configuration 3.

In Configuration 3, the operations of array linear write and array write commands are not affected. The array linear write and array write commands are the same as in Configuration 1.

In Configuration 3, the burst length for array read and array linear read commands is determined by the Wrap Length configuration. These commands perform sequential bursts, and once the length specified by the Wrap Length is reached, the read/write operation will automatically terminate.

When Auto-precharge is set to "ON," PRA is set to "OFF," and Wrap Enable is set to "ON," this mode is assumed to be Configuration 4.

In Configuration 4, the operations of array linear write and array write commands are not affected. The array linear write and array write commands are the same as in Configuration 2.

In Configuration 4, the burst length for array read is determined by the Wrap Length configuration, and wrap burst type is performed. The array linear read command is the same as in Configuration 1.

The burst types for array read and array linear read commands in Configurations 3 and 4 are shown in the following table.

Table 6-3 Burst Types for Array Read and Array Linear Read Commands

PRA	Auto-precharge	Wrap Enable	Wrap Length	Burst Type	Example of bytes sequence(starting address from 8)
OFF	ON	OFF	16B	16B sequential	[8,9,10,...,22,23]
OFF	ON	OFF	32B	32B sequential	[8,9,10,...,38,39]
OFF	ON	OFF	64B	64B sequential	[8,9,10,...,70,71]
OFF	ON	OFF	128B	128B sequential	[8,9,10,...,134,135]
OFF	ON	ON	16B	Wrap 16B	[8,9,10,...,14,15,0,1,...,6,7]
OFF	ON	ON	32B	Wrap 16B	[8,9,10,...,30,31,0,1,...,6,7]
OFF	ON	ON	64B	Wrap 16B	[8,9,10,...,62,63,0,1,...,6,7]
OFF	ON	ON	128B	Wrap 16B	[8,9,10,...,126,127,0,1,...,6,7]

6.1.4 Configuration 5/6/7/8

When PRA is set to "ON," it still only affects array read and array linear read commands. Array write and array linear write commands are not affected.

When PRA is set to "ON," Auto-precharge is set to "OFF," and Wrap Enable is set to "OFF," this configuration is assumed to be Configuration 5.

- In Configuration 5, the operations of array linear write and array write commands are the same as in Configuration 1.
- In Configuration 5, the operations of array linear read commands are the same as in Configuration 1.
- In Configuration 5, the array read command supports a 2KB sequential burst read.

When PRA is set to "ON," Auto-precharge is set to "OFF," and Wrap Enable is set to "ON," this configuration is assumed to be Configuration 6.

- In Configuration 6, the operations of array linear write and array write commands are the same as in Configuration 2.

- In Configuration 6, the operations of array linear read commands are the same as in Configuration 1.
- In Configuration 6, the array read command is the same as in Configuration 2.

When PRA is set to "ON," Auto-precharge is set to "ON," and Wrap Enable is set to "OFF," this configuration is assumed to be Configuration 7.

- In Configuration 7, the operations of array linear write and array write commands are the same as in Configuration 1.
- In Configuration 7, the operations of array linear read commands are the same as in Configuration 1.
- In Configuration 7, the array read command supports only a 128B sequential burst read.

When PRA is set to "ON," Auto-precharge is set to "ON," and Wrap Enable is set to "ON," this configuration is assumed to be Configuration 8.

- In Configuration 8, the operations of array linear write and array write commands are the same as in Configuration 2.
- In Configuration 8, the operations of array linear read commands are the same as in Configuration 1.
- In Configuration 8, the array read command supports only a 128B wrap burst read.

When PRA is set to "ON," the burst types for the array read commands are shown in the following table.

Table 6-4 Burst Types for Array Read Commands

Wrap Length	Auto-precharge="OFF"		Auto-precharge="ON"	
	Wrap Enable="OFF"	Wrap Enable="ON"	Wrap Enable="OFF"	Wrap Enable="ON"
-	Wrap Enable="OFF"	Wrap Enable="ON"	Wrap Enable="OFF"	Wrap Enable="ON"
16B	2KB sequential	16B wrap	Not supported	Not supported
32B	2KB sequential	32B wrap	Not supported	Not supported
64B	2KB sequential	64B wrap	Not supported	Not supported
128B	2KB sequential	128B wrap	128B sequential	128B wrap

6.2 Clock Phase Setting Parameter1 Value

During write access, this parameter is used to adjust the phase difference between IO_apsram_dqs and O_apsram_ck. If the number of chips selected is 2, the parameter is 16 bits, with the lower 8 bits and upper 8 bits driving chip 1 and chip 2 respectively. The parameter value ranges from 16'h0000 to 16'hFFFF. When the parameter is set to 0, the rising edge of IO_apsram_dqs aligns with the midpoint of the low level of O_apsram_ck, as shown in [Figure 6-1](#).

If the user sets the value of Debug Parameter1 Value to n, IO_apsram_dqs shifts to the right relative to O_apsram_ck by $n \times \text{step}$ size, based on the user-defined value.

The user can calculate the step size by adding and viewing dll_step via gao (as shown in Figure 6-2, Figure 6-3). The dll_step is the value mapped corresponding to 1/4 of memory_clk cycle. The step size is calculated as $= \frac{1}{f} \div 4 \div dll_step$, with the step size in ps (picoseconds). f represents the frequency of memory_clk. The memory_clk in Figure 6-2 and Figure 6-3 is 533 MHz, then the step size is 15.6 ps.

Figure 6-1 Initial Phase Relationship Diagram of O_apsram_ck and IO_apsram_dqs

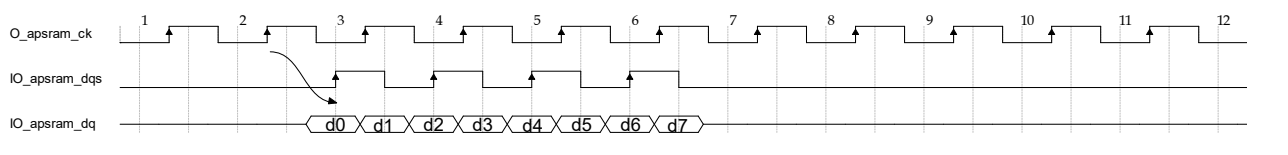


Figure 6-2 Add dll_step Signal to GAO

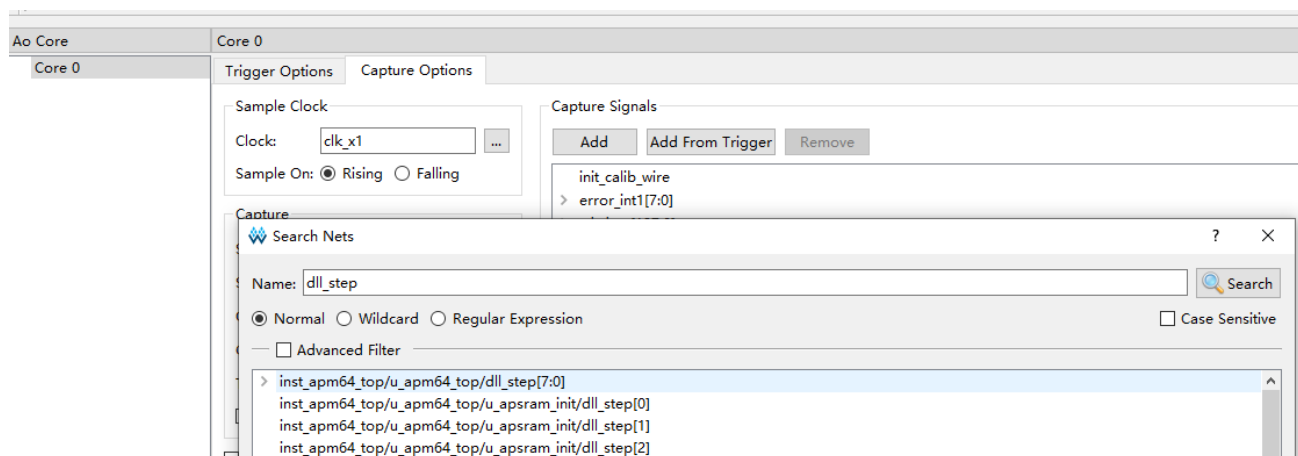
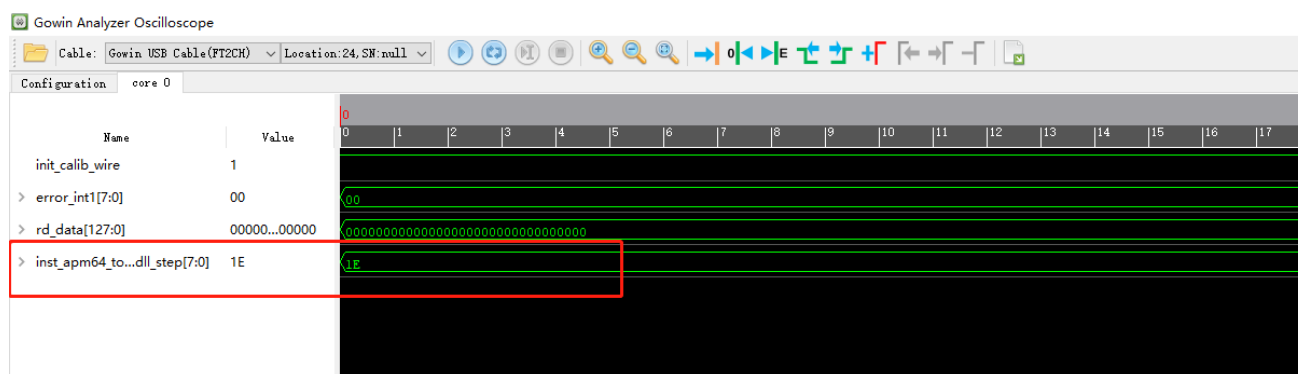


Figure 6-3 View the Value of dll_step



7 Interface Configuration

To correctly use the IP, users need to follow two steps. Step 1 is to correctly configure and generate the IP. Step 2 is to configure the VCCX voltage correctly. Users can select the GW5A series of device to configure the IP and the VCCX voltage in Gowin Software.

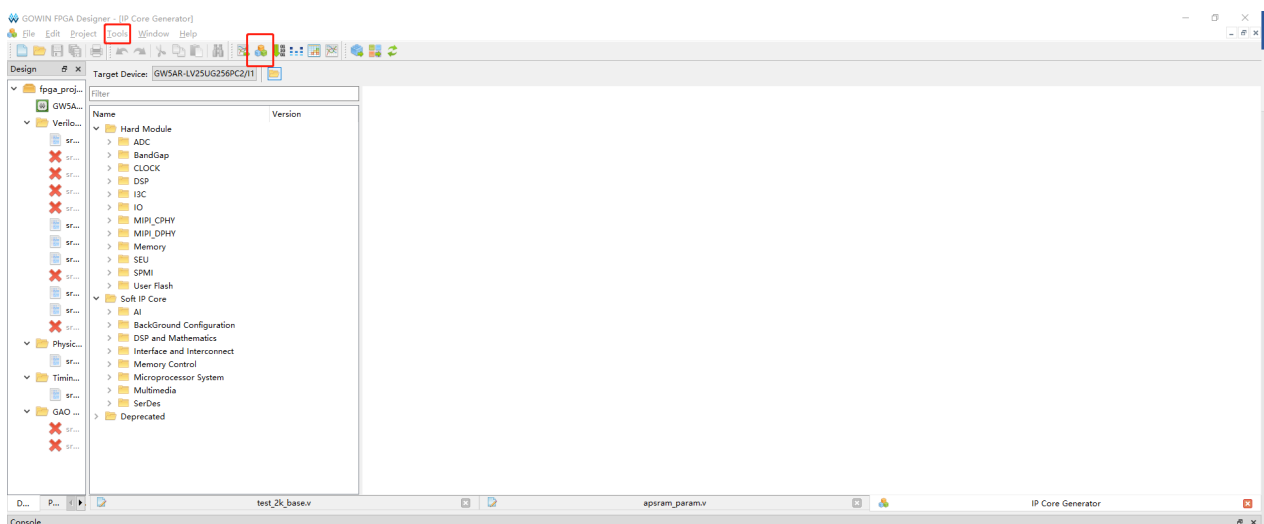
7.1 IP Configuration

Below is a description of the steps to create an IP core, using the GW5AR-LV25UG256P device as an example.

1. Open IP Core Generator.

After creating a new project, click “Tools > IP Core Generator” or directly click the "  " icon on the toolbar to open the IP Core Generator, as shown in [Figure 7-1](#).

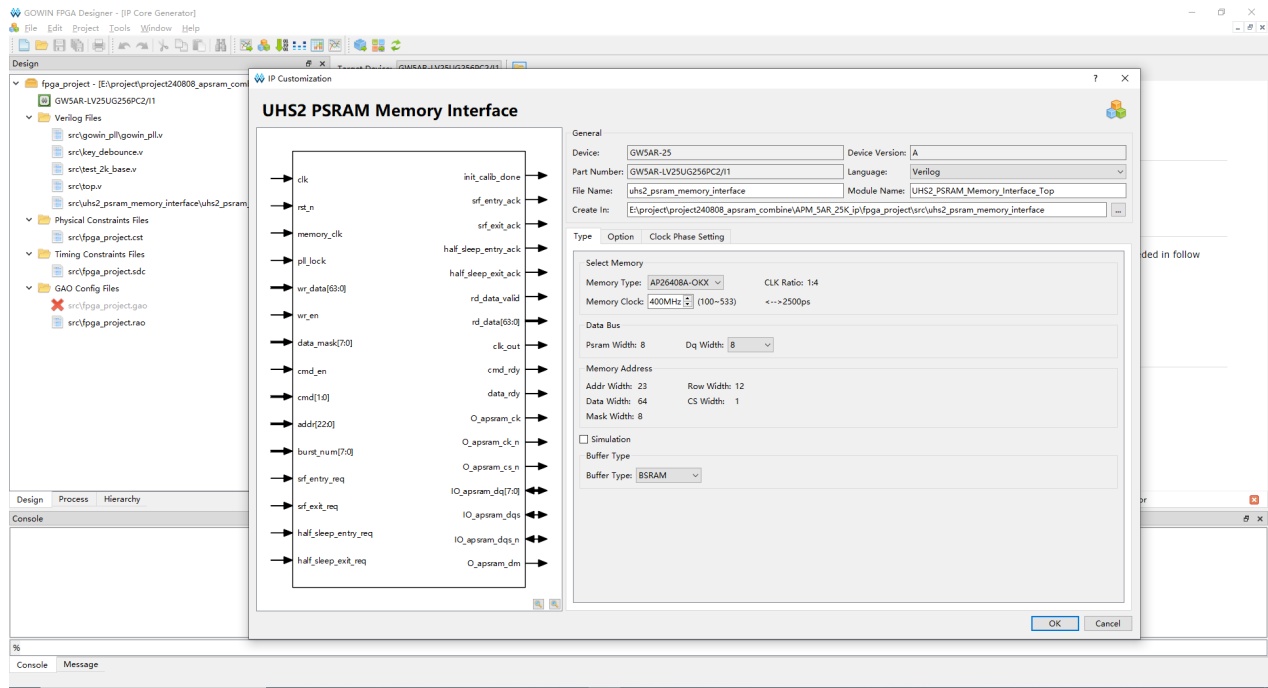
Figure 7-1 Open IP Core Generator



2. Open the UHS2 PSRAM Memory Interface IP core.

Click “Soft IP Core > Memory Control > PSRAM Memory Interface”, then double-click “UHS2 PSRAM Memory Interface” to open UHS2 PSRAM Memory Interface IP core, as shown in [Figure 7-2](#).

Figure 7-2 Open UHS2 PSRAM Memory Interface IP Core



3. IP Configuration Option.

- Select Memory

The "Memory Type" is fixed as "Read-only," indicating the supported PSRAM part number. The current IP only supports the PSRAM AP26408A-OKX.

The "Memory Clock" indicates the memory interface speed required for the current IP. This speed is equal to the differential clock speed of the PSRAM interface. For example, if the IP needs to run at 400MHz, then the "Memory Clock" option should be set to 400 MHz.

- Data Bus

The DQ width of AP26408A-OKX is 8 bits, so the "Psram Width" option is fixed at 8, and users do not need to pay attention to it. DQ Width refers to the total DQ bit width supported by the IP. For example, if the IP supports two PSRAM chips, the total DQ width will be $2 \times 8 = 16$. GW5AR-LV25UG25P device is integrated with two PSRAMs, and if both devices are used, the total DQ width will be 16, so DQ Width should be set to 16.

- Memory Address

The capacity of the AP26408A-OKX is $8\text{M} \times 8\text{bits} = 64\text{Mbits}$, with a column address of 11 bits and a row address of 12 bits. According to the addr-to-PSRAM address mapping in [4.4.2 Send Addresses, Commands, and burst_num](#), the "Addr Width" is calculated as 23 bits. "CS Width" represents the number of PSRAM chips. According to the explanation in Section 4.4.2, the data width between the IP user interface and the PSRAM is 8:1 (Clk Ratio: 4:1), so the "Data Width" is displayed as 64. The "Data Mask" refers to the write data mask width, and each byte corresponds to 1 bit of the Data Mask. Therefore, when the "Data Width" is 64 bits, the "Data Mask" is 8.

- Simulation

When users need to simulate the IP, they can check the "Simulation" option to shorten the PSRAM initialization time. However, when users are performing board-level testing, this option should be turned off, and the IP should be regenerated by clicking the "OK" button at the bottom right.

- Buffer Type

This option is used to configure the type of internal storage resource for the IP. The IP uses a FIFO to buffer the user interface commands and data written to it, as well as the data read from PSRAM. When the "Buffer Type" is set to BSRAM, the FIFO will use BSRAM resources. When the "Buffer Type" is set to REG, the FIFO will use register and LUT resources.

- Options Tab

The Options tab is for configuring the PSRAM chip.

For configuring Wrap Length, PRA Enable, Wrap Enable, and Auto-precharge, users should follow the configuration instructions in [6.1.1 Wrap Enable, Wrap Length, Auto-precharge, and PRA Enable](#). This section will not go into further detail.

The "RW Latency" option must match the Memory Clock. For Memory Clock speeds of 200MHz and below, select 9_5. For speeds greater than 200MHz and less than or equal to 333MHz, select 13_5. For speeds greater than 333MHz and less than or equal to 400MHz, select 16_6. For speeds greater than 400MHz and less than or equal to 533MHz, select 20_10. Users must configure the RW Latency according to the correct range; otherwise, the IP's read and write operations may be incorrect.

The "VREF Trim" option is used to calculate the decision level of the PSRAM chip. When this option is set to 50.00, the decision level is 50% of the PSRAM operating voltage. Since the PSRAM operating voltage is 1.8V, the decision level will be $1.8V \times 50.00\% = 0.9V$. When using a Gowin development board for board-level testing, if VCCX = 3.3V, select 50.00, and the maximum IP speed will be 533MHz. If VCCX = 1.8V, select 44.83, and the maximum IP speed will still be 533MHz.

The "Drive Strength" option adjusts the output current strength of the PSRAM interface. When this option is set to 18 ohms, the power consumption is greater than that when it is set to 40 ohms.

The tREFi option is fixed at 7800000ps.

- Clock Phase Setting

For the details of Clock Phase Setting Parameter1 Value, see Section [6.2 Clock Phase Setting Parameter1 Value](#).

Figure 7-3 IP Options

UHS2 PSRAM Memory Interface

General

Device: GW5AR-25 Device Version: B

Part Number: GW5AR-LV25UG256PC1/I0 Language: Verilog

File Name: 2_psram_memory_interface Module Name: Memory_Interface_Top

Create In: Documents\uhs2_psram_memory_interface

Type **Option** **Clock Phase Setting**

Select Memory

Memory Type: AP26408A CLK Ratio: 1:4

Memory Clock: 400MHz (100~533) <--> 2500ps

Data Bus

Psram Width: 8 Dq Width: 8

Memory Address

Addr Width: 23 Row Width: 12

Data Width: 64 CS Width: 1

Mask Width: 8

☐ Simulation

Buffer Type

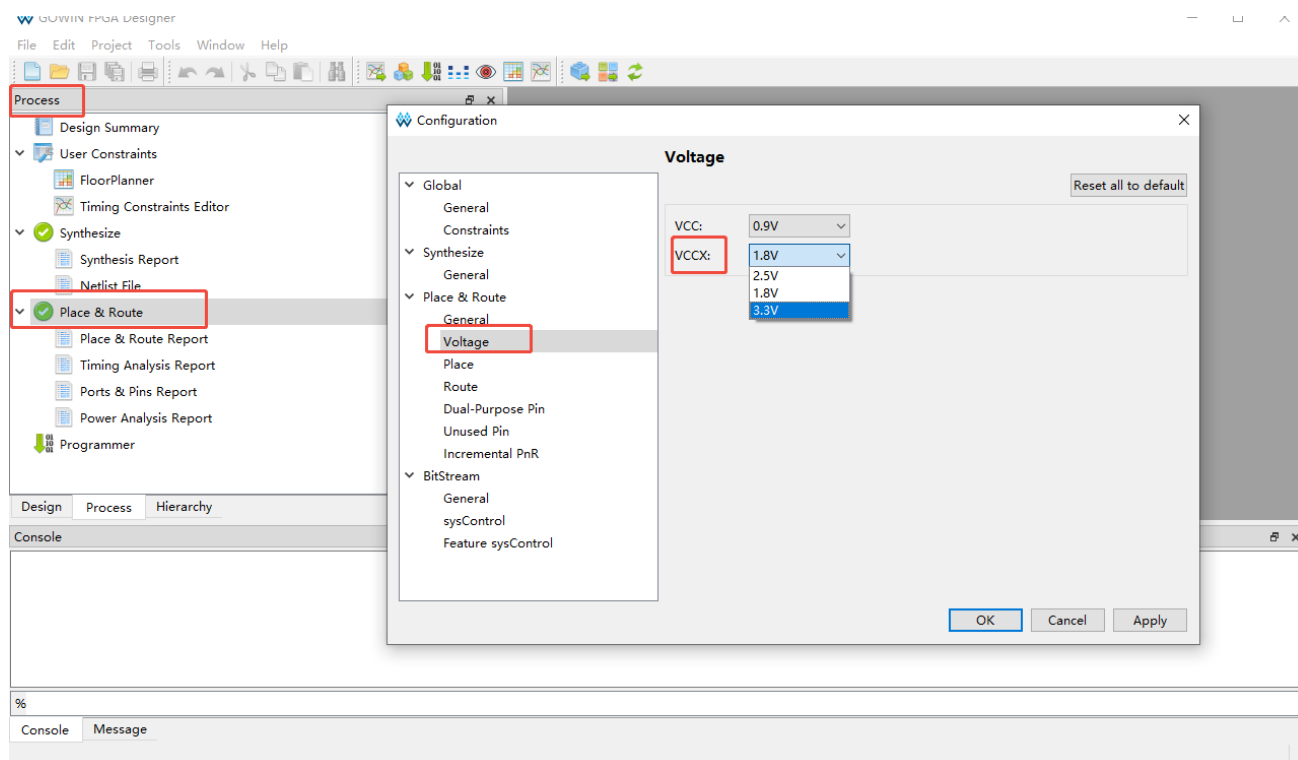
Buffer Type: BSRAM

OK Cancel

7.2 VCCX Voltage Configuration

Users can right-click on "Place & Route" in the process dialog box and select "Configuration." In the pop-up dialog, click on "Voltage" to configure VCCX. As shown in [Figure 7-4](#), the selected VCCX voltage must be consistent with the VCCX supply voltage in the schematic.

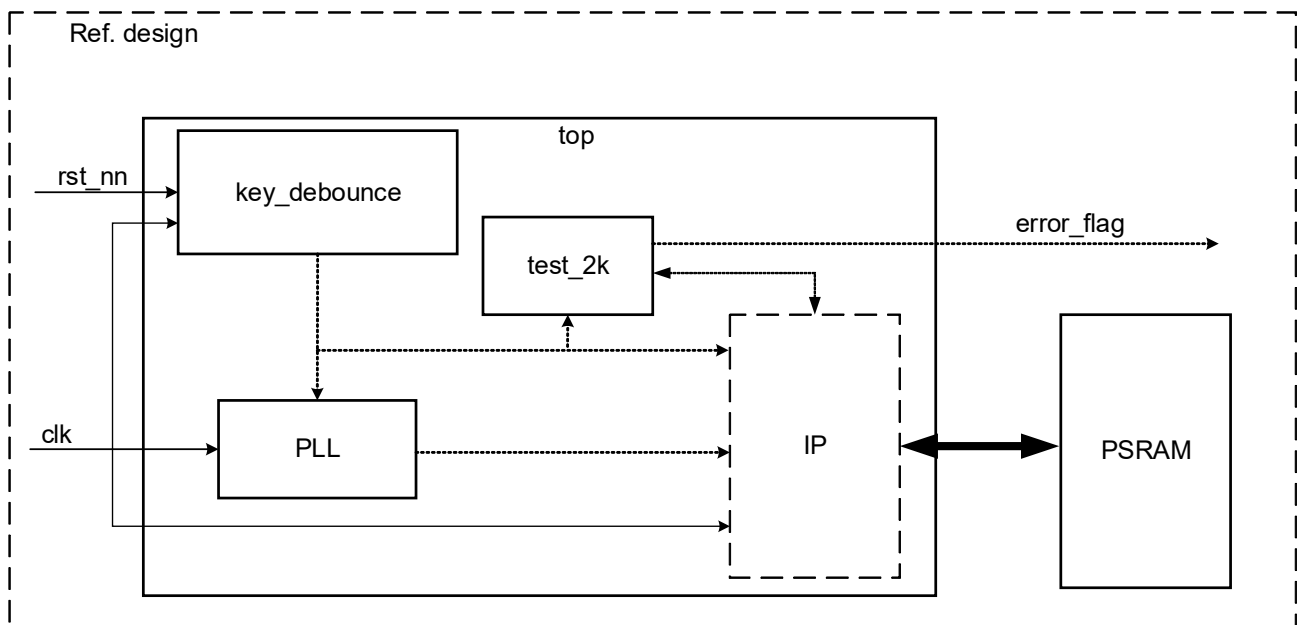
Figure 7-4 VCCX Configuration Interface



8 Reference Design

To help users quickly familiar with Gowin UHS2 PSRAM Memory Interface IP, a [reference design](#) is provided. The basic structure of the reference is as shown in [Figure 8-1](#).

Figure 8-1 Reference Design Block Diagram



The functions of each module are as follows:

- The key_debounce is used to eliminate the signal jitter generated by the key or DIP switch when it controls the external stimulus, and generate a global reset signal.
- test_2k is used to generate read/write timing, write data, and enable signals, and check whether the data returned from the PSRAM to the IP is correct.
- The PLL is used to perform frequency multiplication for the memory clock, etc.

Table 8-1 Input Port List

Name	Description
clk	Input reference clock, 50 MHz by default.
rst_nn	Input reset signal

After IP initialization is completed, test_2k can automatically cycle read and write operations to different addresses, and each burst length is increased by itself, traversing all burst cases. It analyzes and verifies the read data returned by Gowin UHS2 PSRAM Memory Interface IP, and outputs the detection signal. When the error_flag signal is pulled high to indicate that there is an error code; otherwise, there is no error.

9 File Delivery

The delivery file of Gowin UHS2 PSRAM Memory Interface IP includes documentation and reference design.

9.1 Document

The folder contains the user guide in PDF version.

Table 9-1 Document List

Name	Description
IPUG1194, Gowin UHS2 PSRAM Memory Interface IP User Guide	Gowin UHS2 PSRAM Memory Interface IP, i.e., this manual.

9.2 Reference Design

The Ref. Design folder contains the netlist file, the user reference design, the constraint file, the jitter elimination module, the top file, and the project file folder, etc.

Table 9-2 Ref.design Folder Content List

Name	Description
top.v	The top module of reference design
key_debounce.v	Key jitter elimination module
test_2k.v	Test stimulus generation module
UHS2_PSRAM_Memory_Interface.vo	Gowin UHS PSRAM Memory Interface IP netlist file
psram.cst	Project physical constraints file
psram.sdc	Project timing constraints file
psram.gao	Project gao file
UHS2_PSRAM_Memory_Interface	IP core folder

