



Gowin SSCPLL IP

User Guide

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Revision History

Date	Version	Description
11/08/2024	1.0E	Initial version published.
01/17/2025	1.1E	Supported devices updated.
02/28/2025	1.2E	The issue of unstable output clock under certain combinations fixed and the clock frequency range updated.
06/06/2025	1.3E	● The input clock frequency range adjusted. ● PLL initialization optimized.
03/27/2026	1.4E	● Added support for GW3A-20 devices. ● Added mDRP functionality for GW3A-20 devices.
06/26/2026	1.5E	Added the lock port signal.

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1 About This Guide

1.1 Purpose

The purpose of Gowin SSCPLL IP User Guide is to help you to quickly understand the features and usage of Gowin SSCPLL IP by providing the descriptions of the functions, signal definition, parameters, and reference design. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.12.03. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at www.gowinsemi.com:

- [SUG100, Gowin Software User Guide](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1118, GW5ART series of FPGA Products Data Sheet](#)
- [DS1351, GW3A series of FPGA Products Data Sheet](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
ALU	Arithmetic Logic Unit
DRP	Dynamic Reconfiguration Port
EMI	Electromagnetic Interference

Terminology and Abbreviations	Meaning
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
IP	Intellectual Property
LUT	Look-up Table
PLL	Phase-locked Loop
REG	Register
SSC	Spread Spectrum Clocking

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Introduction

Gowin SSCPLL IP generates spread-spectrum output clocks at different frequencies based on the given input clocks and Spread Spectrum Clocking (SSC) parameters, reducing electromagnetic interference (EMI) between devices.

Table 2-1 Gowin SSCPLL IP Overview

Gowin SSCPLL IP	
Logic Resource	See Table 2-2.
Delivered Doc.	
Design Files	Verilog (encryption)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.10.03 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features

- Supports configurable input and output clock frequencies, with the range determined by the selected device
- Supports SSC
- Supports configurable modulation frequency, ranging from 30 to 50 KHz
- Supports configurable modulation depth, ranging from 0 to 30000 ppm
- Supports configurable modulation direction, including both Up and Down
- Supports mDRP (micro Dynamic Reconfiguration Port) functionality, available only for the GW3A-20 devices

2.3 Resource Utilization

Gowin SSCPLL IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW5AST device as an instance, the resource utilization is as shown in Table 2-2. For the resource utilization of other devices, please refer to later release information.

Table 2-2 Resource Utilization

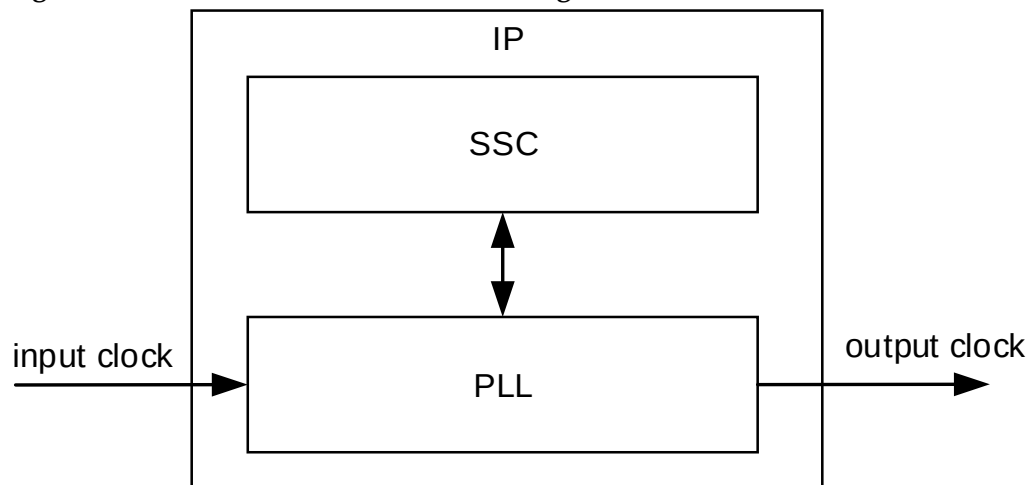
Device	Programming Language	LUTs	REGs	ALUs
GW5AST-138	Verilog	86	156	130

3 Functional Description

3.1 Structure

Gowin SSCPLL IP consists of two parts, the PLL and SSC, as shown in Figure 3-1.

Figure 3-1 Gowin SSCPLL IP Structure Diagram



- PLL: Generates spread-spectrum output clocks at different frequencies based on the given input clocks and SSC parameters.
- SSC: Generates the data needed by the PLL for spread-spectrum operation, based on parameters such as modulation depth, frequency, and direction.

3.2 SSCPLL

Gowin SSCPLL IP essentially functions as a PLL that generates the desired output clock based on the input clock. To reduce EMI between devices when using the output clock, Gowin SSCPLL IP integrates an SSC.

First, set the input and output clock frequencies of Gowin SSCPLL IP according to the design requirements. Note that the supported frequency range of Gowin SSCPLL IP varies depending on devices, and you can see Table 3-1 for details.

Table 3-1 Input and Output Clock Range

Device	Input Clock Range	Output Clock Range
GW5AT-75	19 MHz~400 MHz	6.25 MHz~1000 MHz
GW5A-138		
GW5AS-138		
GW5AT-138		
GW5AST-138		
GW5A-25	19 MHz~400 MHz	6.25 MHz~1200 MHz
GW5AR-25		
GW5AS-25		
GW5ART-15		
GW5AT-15		
GW5A-60		
GW5AT-60		
GW3A-20	19 MHz~400 MHz	5 MHz~640 MHz

For the input clock, select the oscillator on the development board as the clock source. For the output clock, based on the clock requirements in the design, it can be configured as either single-ended or differential within the FPGA, then output to the development board used as a reference clock.

Next, configure the SSC parameters, including modulation speed, depth, and direction.

- The modulation speed reflects the speed of the frequency change of the modulated signal. If the modulation speed is set too high, the subsequent PLL circuit may not be able to track. The modulation speed range for SSC is from 30 to 50 kHz.
- Modulation depth refers to the frequency variation range of the modulated signal during spread-spectrum operation. If the modulation depth is set too low, the improvement in EMI reduction is limited; if set too high, the clock frequency may deviate significantly. The SSC modulation depth range is from 0 to 30,000 ppm.
- Modulation direction supports up and down. Since up-spreading can cause the frequency to exceed the output clock frequency, which may impact the system, down-spreading is generally more widely used.

The SSC parameters should be gradually adjusted during the debugging based on actual conditions to achieve the goal of reducing EMI between devices.

3.3 mDRP

Gowin SSCPLL IP supports the mDRP functionality, which is available only for the GW3A-20 devices.

The mDRP function allows users to configure and control the PLL dynamically. Its usage is consistent with the standard mDRP interface.

It is recommended not to modify the MDIV-related configurations of the PLL when using the mDRP function, as this may conflict with the SSC function.

4 Port Description

Gowin SSCPLL IP port diagram is as shown in Figure 4-1.

Figure 4-1 Gowin SSCPLL IP Port Diagram

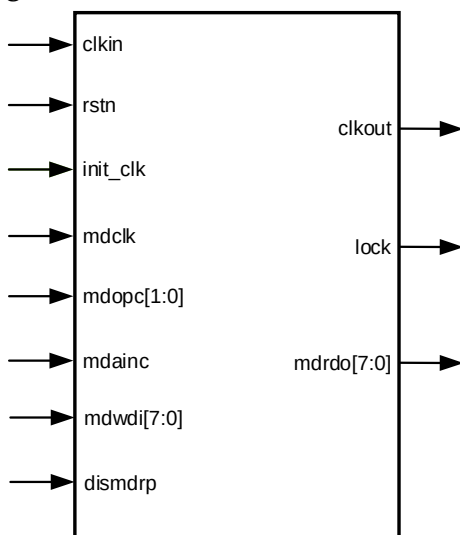


Table 4-1 SSCPLL Port Signal

Name	Type	Data Width	Description
<code>clk</code> in	Input	1	Clock input
<code>rst</code> n	Input	1	Reset signal, active-low.
<code>lock</code>	Output	1	Clock stable signal, active-high
<code>clk</code> out	Output	1	Clock output
<code>init_clk</code>	Input	1	Initialization clock input; This signal is available only for GW5A series devices.
<code>mdclk</code>	Input	1	Clock input for the mDRP interface. All signal transitions are triggered on the rising edge of this clock.
<code>mdopc</code>	Input	2	Operation code: ● 00: No operation (NOOP) ● 10: Read operation (RD) ● 01: Write operation (WR) ● 11: Register address remains unchanged

Name	Type	Data Width	Description
			regardless of the value of mdainc
mdainc	Input	1	Address increment indicator, active high.
mdwdi	Input	8	Write data signal
mdrdo	Output	8	Read data signal
dismdrp	Input	1	mDRP interface disable signal, active high.

5 Call and Configure IP

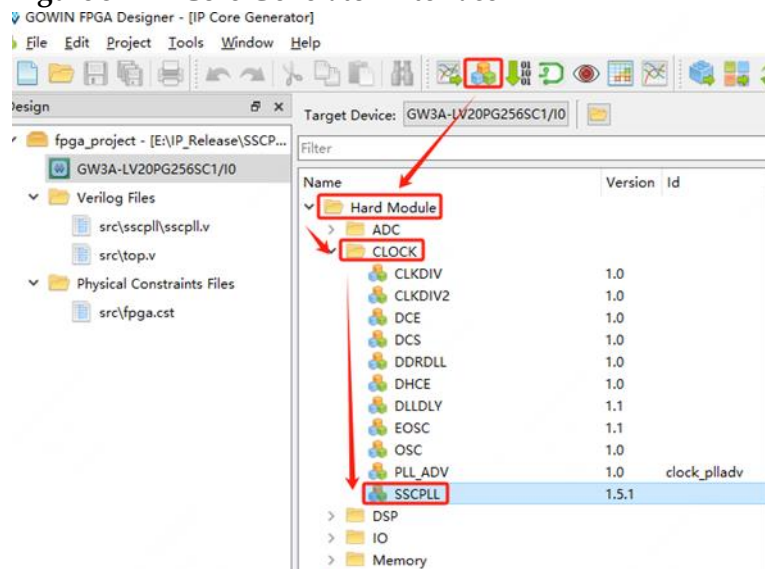
5.1 Call IP

Click on the shortcut " " or "Tools > IP Core Generator" on the menu bar in Gowin Software to call and configure Gowin SSCPLL IP.

1. Open IP Core Generator.

After creating a new project, click "IP Core Generator" to open the IP Core Generator, as shown in Figure 5-1.

Figure 5-1 IP Core Generator Interface



2. Open Gowin SSCPLL IP

Double-click "Hard Module > CLOCK > SSCPLL" to start the SSCPLL IP interface, as shown in Figure 5-2 and Figure 5-3.

Figure 5-2 SSCPLL Configuration Interface for GW5A Series Devices

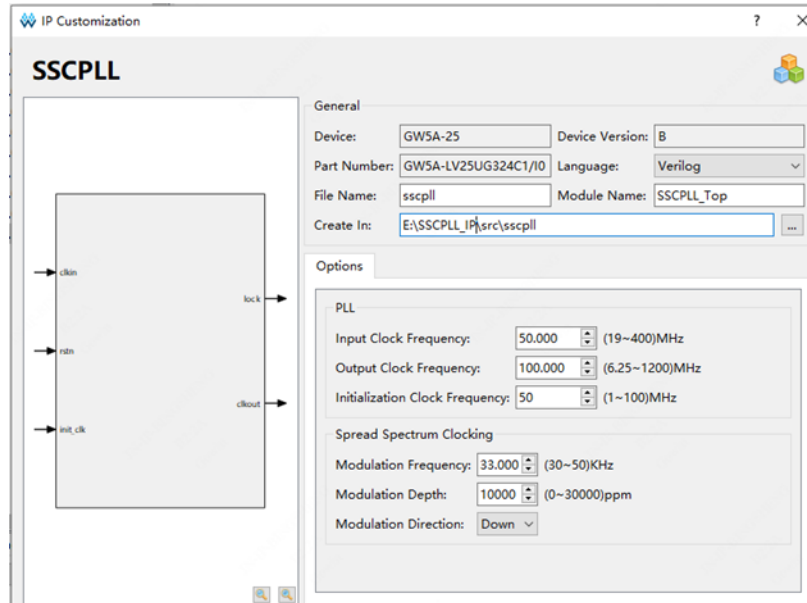
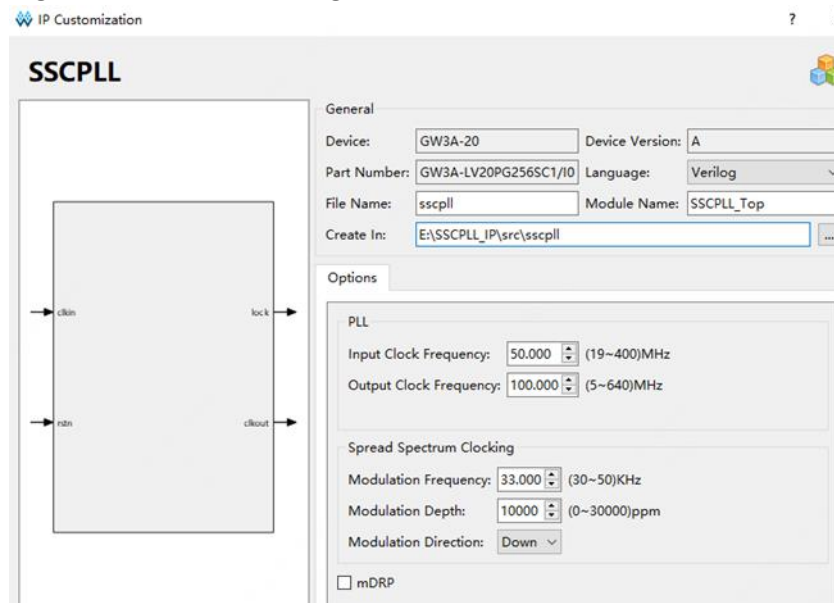


Figure 5-3 SSCPLL Configuration Interface for GW3A Series Devices



- You can configure the generated file name by modifying "File Name".
- You can configure the top module name by modifying "Module Name".
- You can configure other options by modifying "Options" tab.

5.2 Configuration Description

Note!

In the descriptions of GW5A*-[75|138], GW5A*-[15|25|60], and GW3A*-[20], the asterisk * represents zero or more feature codes, and the square brackets [] indicates that one of the options separated by "|" must be chosen. For example, GW5A*-[75|138] can represent devices such as GW5A-138, GW5AS-138, GW5AT-138, GW5AST-138, GW5AT-75, etc.

Table 5-1 Configuration Description

Option	Description
Input Clock Frequency	Input Clock Frequency: ● For GW5A-75/138 devices, the input range is from 19 to 400 MHz, with values specified to three decimal places. ● For GW5A-15/25/60 devices, the input range is from 19 to 400 MHz, with values specified to three decimal places. ● For GW3A-20 devices, the input frequency range is from 19 to 400 MHz, with values specified to three decimal places.
Output Clock Frequency	Output Clock Frequency: ● For GW5A-75/138 devices, the output range is from 6.25 to 1000 MHz, with values specified to three decimal places. ● For GW5A-15/25/60 devices, the output range is from 6.25 to 1200 MHz, with values specified to three decimal places. ● For GW3A-20 devices, the output range is from 5 to 640 MHz, with values specified to three decimal places.
Initialization Clock Frequency	1-100 MHz (integer values only). This option is available only on GW5A-15/25/60/75/138 devices.
Modulation Frequency	The range is from 30 to 50 KHz, with values specified to three decimal places.
Modulation Depth	The range is from 0 to 30000 ppm, integer values.
Modulation Direction	Supports Down and Up.
mDRP	Dynamic reconfiguration port: Checked: mDRP is enabled. Unchecked: mDRP is disabled. This option is available only on GW3A-20 devices.

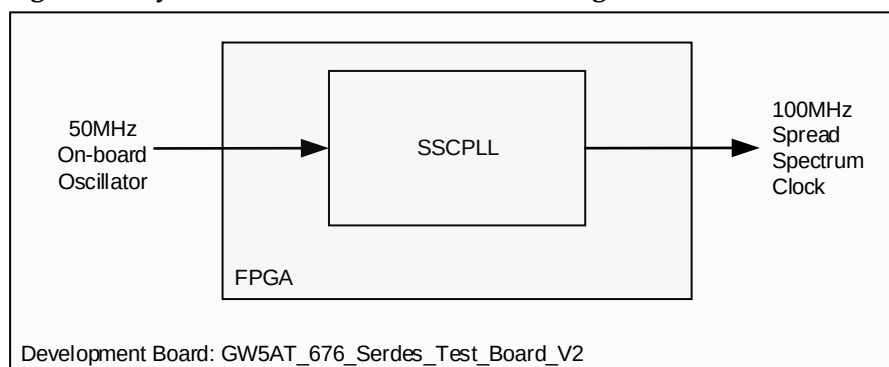
6 Reference Design

For more information, see Gowin SSCPLL IP [reference design](#) at Gowin website.

6.1 Hardware Platform

This section describes the routines for implementing Gowin SSCPLL IP on GW5AT_676_Serdes_Test_Board_V2. The system structure is as shown in Figure 6-1. The system consists of the crystal oscillator and the IP.

Figure 6-1 System Structure of Reference Design



6.2 Operating Principles

The system clock is generated by the on-board crystal oscillator and works as follows:

1. The 50 MHz on-board crystal oscillator generates a clock signal to the FPGA, which serves as the input clock and initialization clock for Gowin SSCPLL IP.
2. The SSCPLL IP generates a 100 MHz spread spectrum clock based on the parameters and outputs this spread spectrum clock to the external FPGA.
3. An oscilloscope or spectrum analyzer is used to analyze the output spread spectrum clock to verify if it meets the requirements.
4. Users can adjust the SSCPLL IP as needed to obtain a clock of the desired frequency for the testing.

6.3 Operating Flow

1. Open Gowin Software (Gowin_V1.9.10.03 and above) > Open routine project and set top level file > Compile routine > Download the generated bitstream file (fpga_project.fs) to the board.
2. Open the oscilloscope and select a channel to test the spread spectrum clock output from the FPGA.
3. Enable Fast Fourier Transform (FFT) function on the oscilloscope to perform an FFT analysis on the measured clock, converting it from the time domain to the frequency domain.
4. A 100 MHz clock signal without spread spectrum will have most of its energy concentrated around 100 MHz in the frequency domain, with a very narrow bandwidth, as shown in Figure 6-2.
5. The 100 MHz spread spectrum clock signal output by the SSCPLL IP will also have most of its energy concentrated around 100 MHz in the frequency domain; however, its bandwidth is broadened in comparison, as shown in Figure 6-3.

Figure 6-2 Frequency Domain of 100MHz

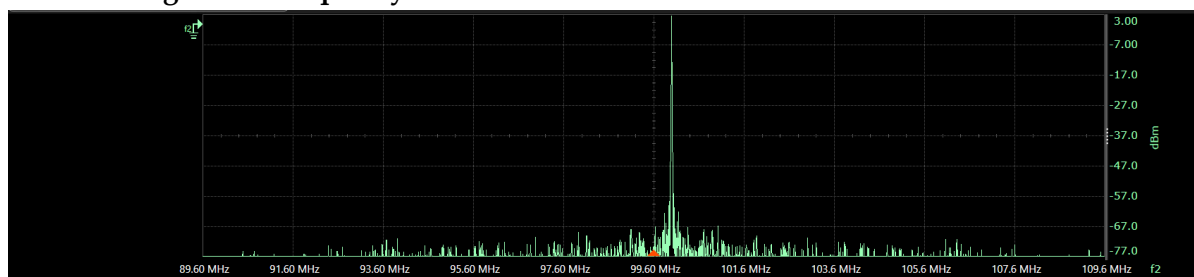
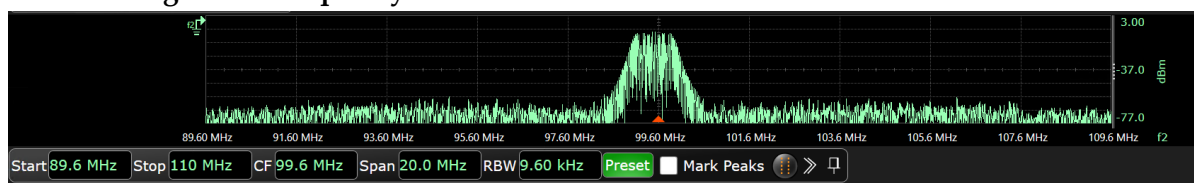


Figure 6-3 Frequency Domain of 100MHz



7 File Delivery

The delivery file of Gowin SSCPLL IP includes documentation and reference design.

7.1 Documentation

The folder contains the user guide in PDF version.

Table 7-1 Document List

Name	Description
IPUG1193, Gowin SSCPLL IP User Guide	Gowin SSCPLL IP User Guide

7.2 Reference Design

Table 7-2 Reference Design File List

File Name	Description
top.v	The top-level file of the IP routine, which provides interface information, unencrypted
sscpll	The SSCPLL IP folder, containing the files related to SSCPLL
fpga.cst	Project physical constraints file

