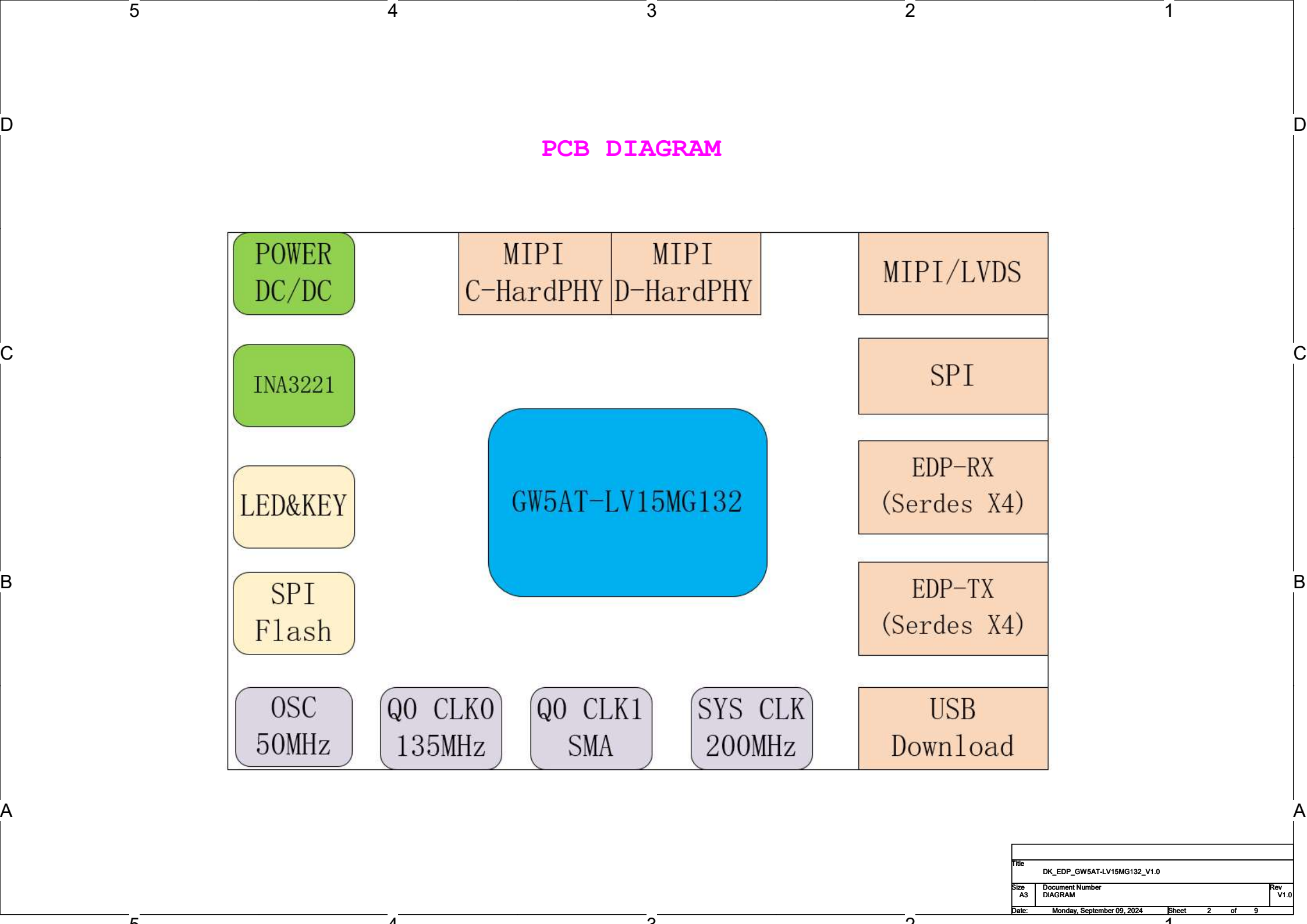
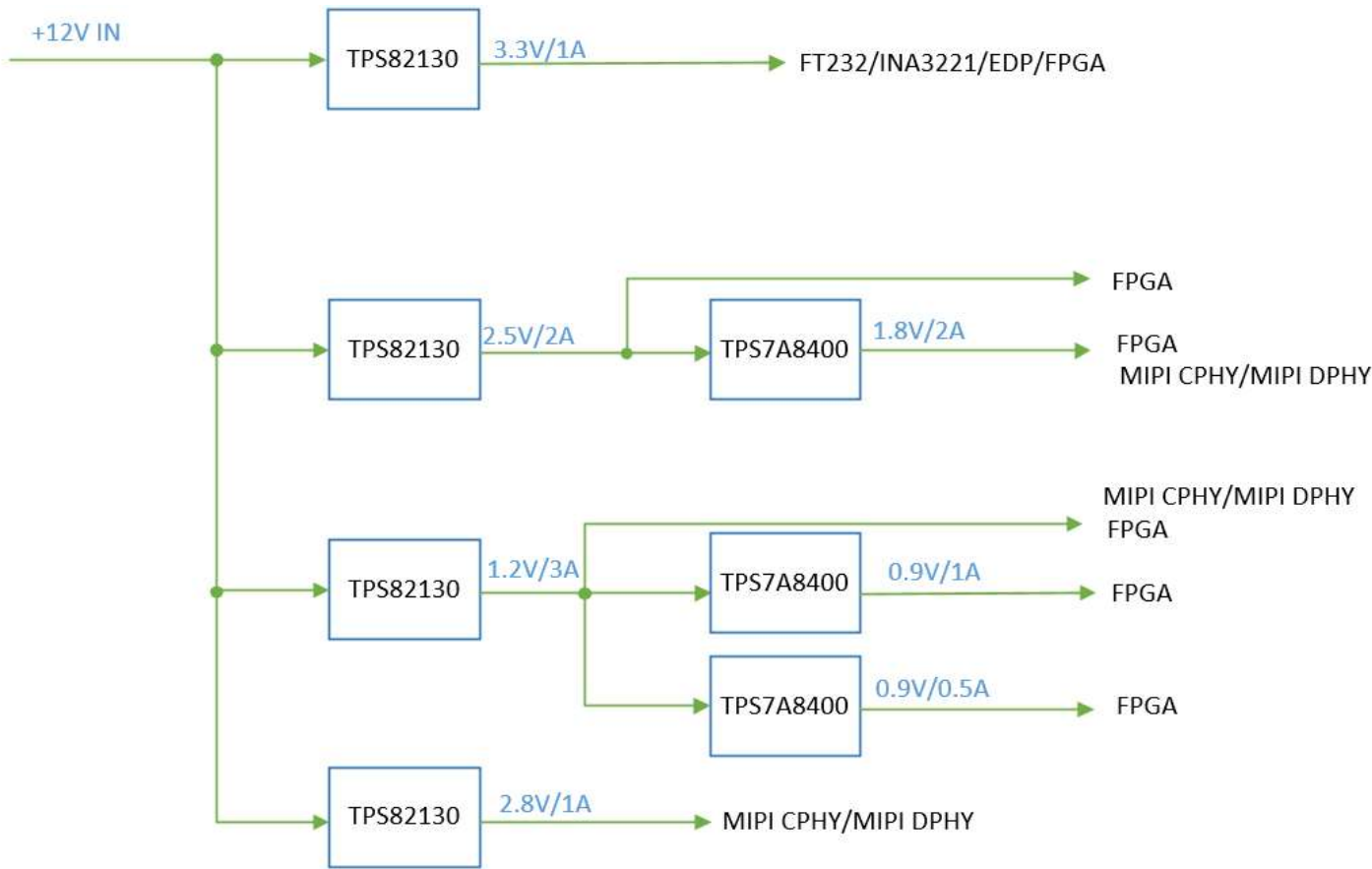


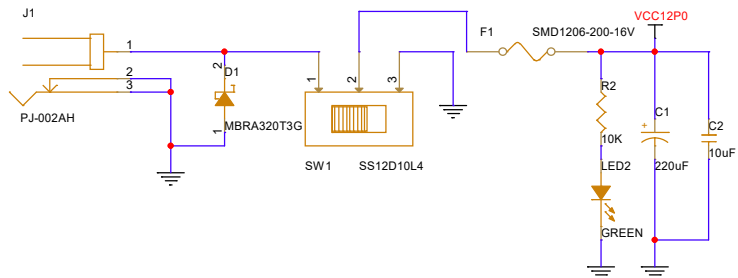
SCHEMATIC	CONTENT	PAGE
COVER PAGE	COVER PAGE	01
DIAGRAM	PCB DIAGRAM	02
POWER	VCC3P3,VCC2P8,VCC2P5,VCC1P8,VCC1P2,VCC0P9	03~05
FPGA-1	MIPI,SPI-FLASH,SPI,CLOCK,CONFIG	06
FPGA-2	EDP-TX,EDP-RX	07
FPGA-3	LVDS/MIPI,USB-JTAG,OSC,RST,LED	08
FPGA-4	FPGA POWER&GND	09



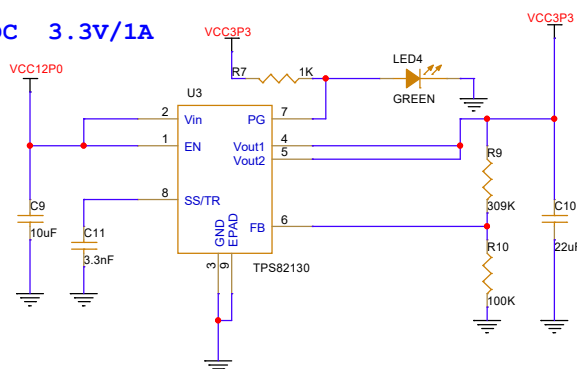
POWER TREE



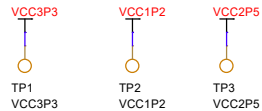
12V INPUT



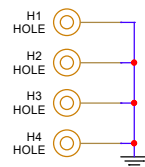
DC/DC 3.3V/1A



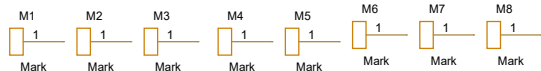
Power Test Hole



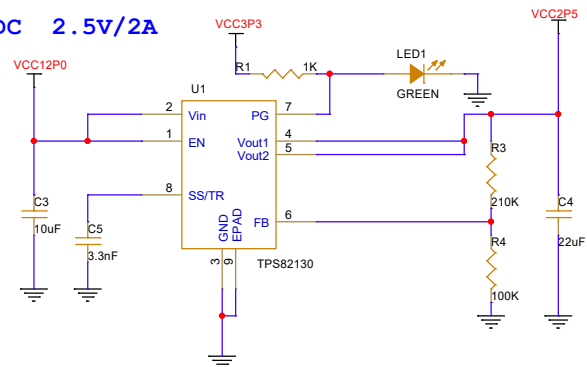
Mounting Hole



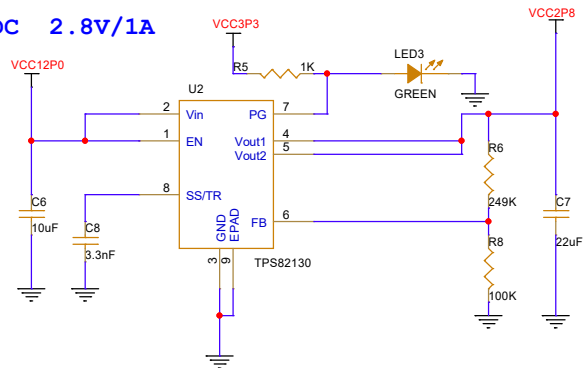
Mark



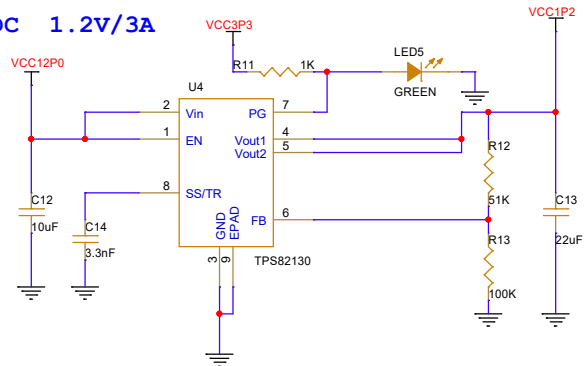
DC/DC 2.5V/2A



DC/DC 2.8V/1A

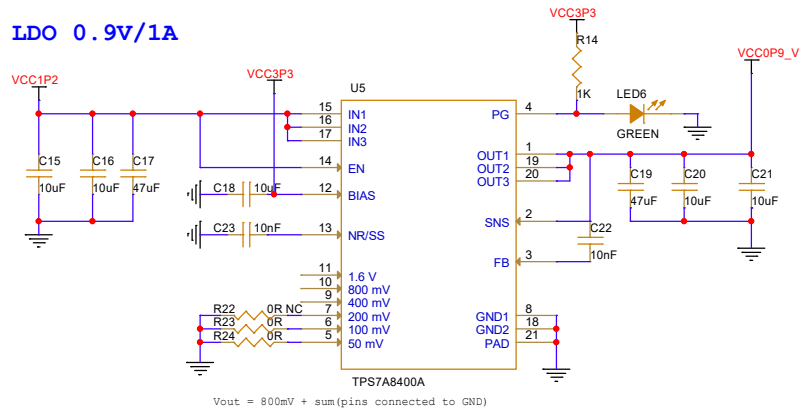


DC/DC 1.2V/3A

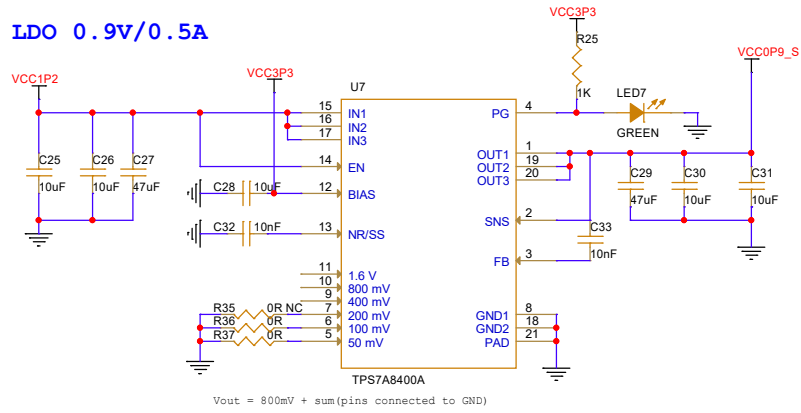


Title		
DK_EDP_GW5AT-LV15MG132_V1.0		
Size	Document Number	Rev
A3	POWER I	V1.0
Date:	Monday, September 09, 2024	Sheet 4 of 9

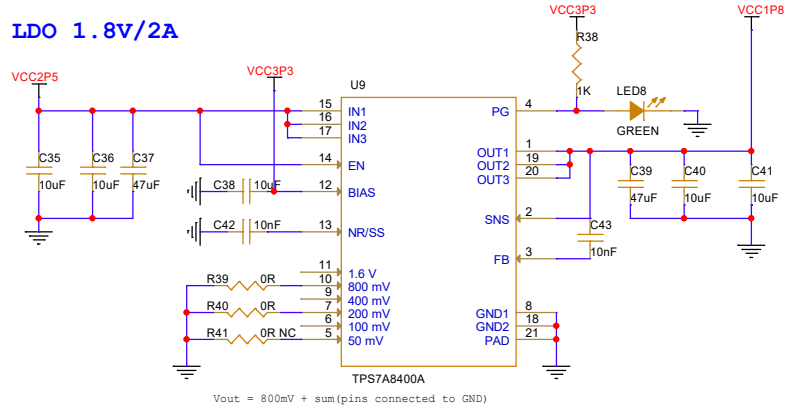
LDO 0.9V/1A



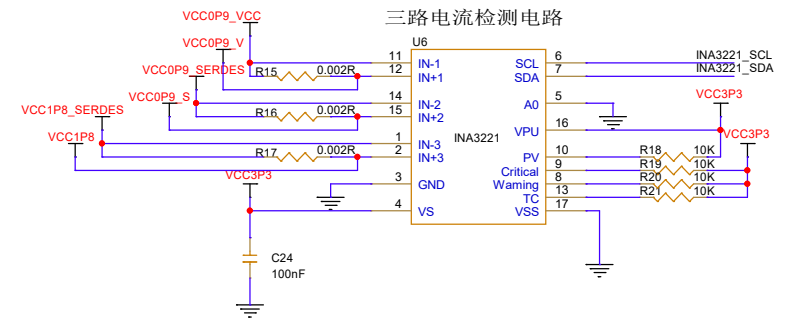
LDO 0.9V/0.5A



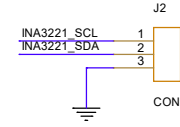
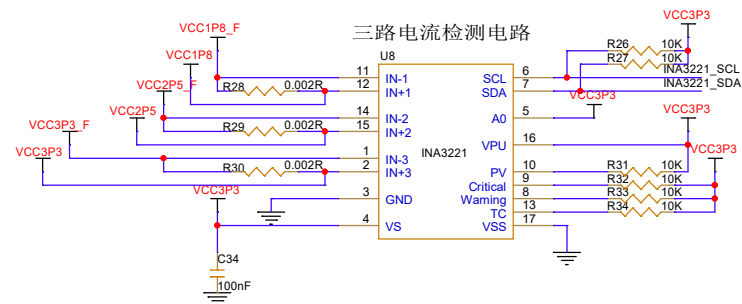
LDO 1.8V/2A



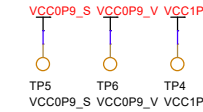
三路电流检测电路



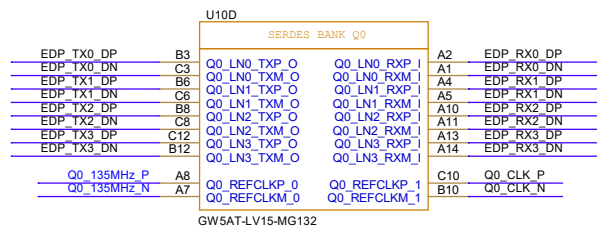
三路电流检测电路



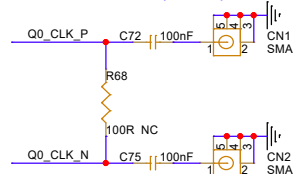
Power Test Hole



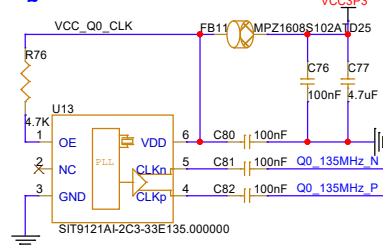
Title			DK_EDP_GW5AT-LV15MG132_V1.0
Size	A3	Document Number	POWER II
Date:	Monday, September 09, 2024	Sheet	5 of 9



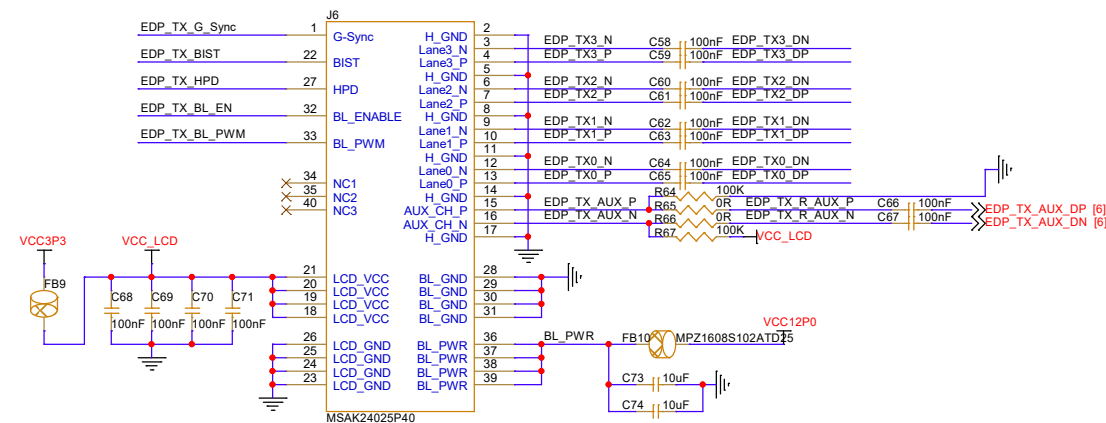
CLOCK IN (SMA)



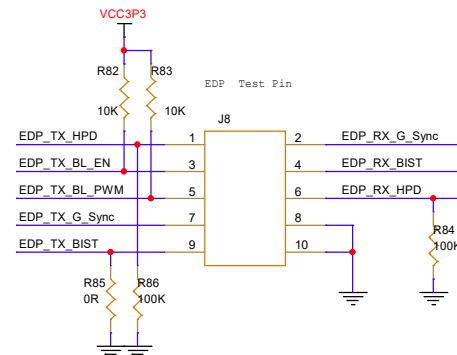
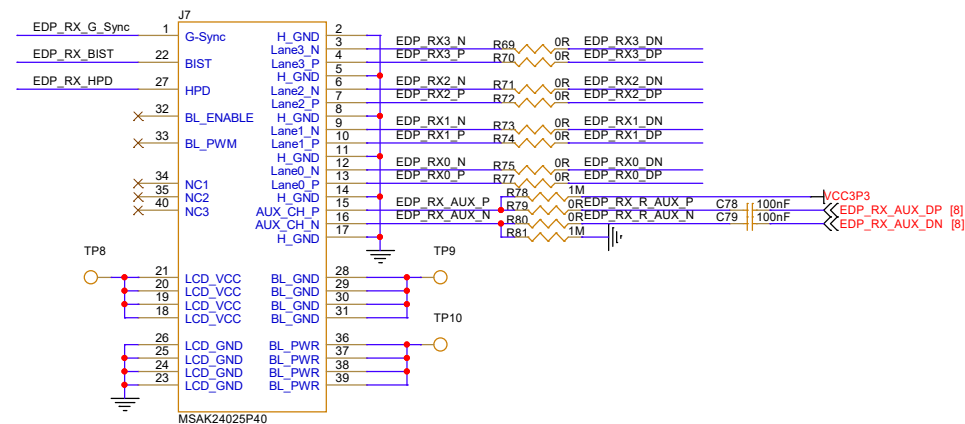
Q0_CLK135MHz



EDP-TX



EDP-RX



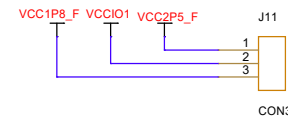
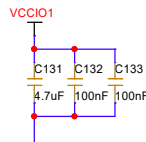
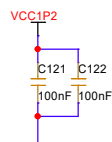
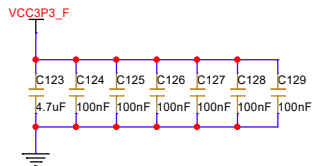
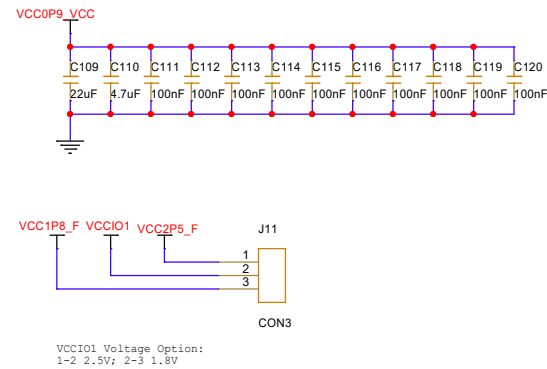
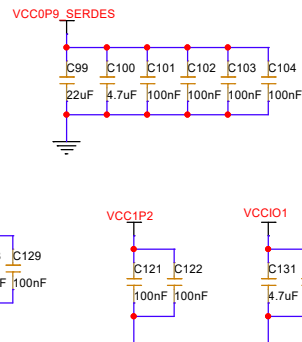
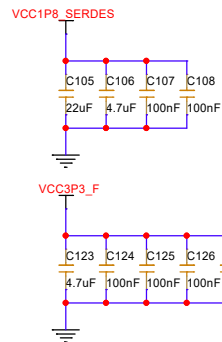
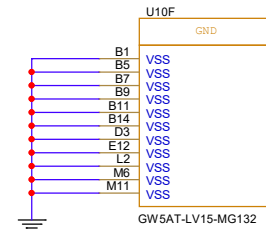
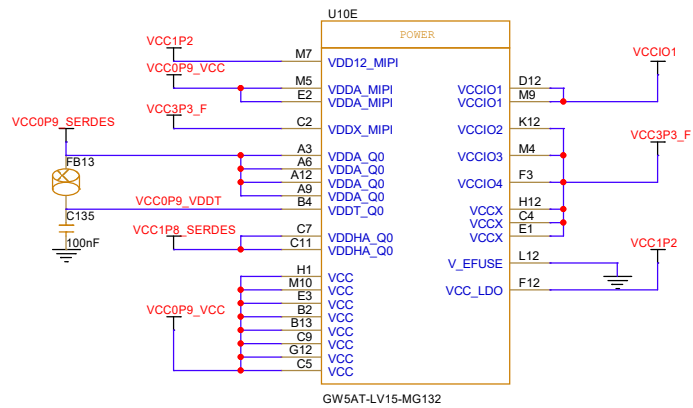
5

4

3

2

1



VCCIO1 Voltage Option:
1-2 2.5V; 2-3 1.8V