



Gowin BCDR IP

User Guide

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Revision History

Date	Version	Description
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1 About This Guide

1.1 Purpose

The purpose of Gowin BCDR IP User Guide is to help you learn the features and usage of Gowin BCDR IP by providing the descriptions of functions, GUI, and reference design, etc. The software screenshots and the supported products listed in this manual are based on Gowin Software V1.9.10.01 (64-bit). As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at www.gowinsemi.com:

- [SUG100, Gowin Software User Guide](#)
- [DS1228, Arora V FPGA Products Overview](#)
- [DS981, Arora V 138K & 75K FPGA Products Data Sheet](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
BCDR	Burst Clock Data Recovery
CDR	Clock Data Recovery
IP	Intellectual Property
FPGA	Field Programmable Gate Array
OLT	Optical Line Terminal
PON	Passive Optical Network
SerDes	Serializer/Deserializer

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

Gowin BCDR IP implements PHY layer functions of the PON protocol, achieving TX 2.48832 Gbps and RX 1.24416 Gbps. In the receive direction, it provides Burst Clock Data Recovery (BCDR) function. This IP can be applied in Optical Line Terminal (OLT) equipment for Passive Optical Network (PON) communication.

Table 2-1 Gowin BCDR IP Overview

Gowin BCDR IP	
Logic Resource	See Table 2-2.
Delivered Doc.	
Design Files	Verilog (encryption)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.1 Features

- Supports TX 2.48832 Gbps and RX 1.24416 Gbps
- Supports BCDR in the receive direction
- Supports 16-bit user interface

2.2 Operating Frequency

Gowin BCDR IP operates at 155.52 MHz.

2.3 Resource Utilization

Gowin BCDR IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW5AT series of FPGA as an instance, the resource utilization is as shown in Table 2-2. For the resource utilization of other devices, see the later release information.

Table 2-2 Resource Utilization

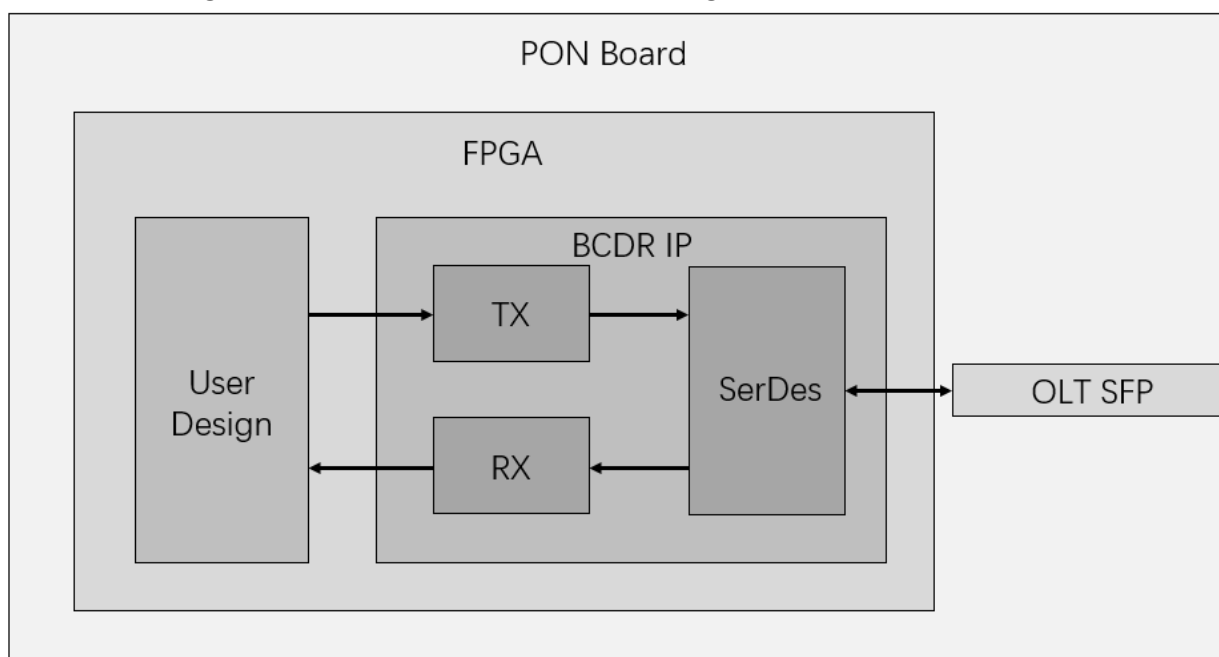
LUTs	REGs	Device	Speed
177	162	GW5AT-138	ES

3 Functional Description

3.1 Structure

Gowin BCDR IP block diagram is as shown in Figure 3-1, and it mainly includes the RX, TX, and SerDes modules. The User Design in Figure 3-1 refers to the User Design in the FPGA, and OLT SFP is the OLT-specific optical module.

Figure 3-1 Gowin BCDR IP Structure Diagram



- SerDes: Implements data serialization and deserialization, serving as a high-speed data transceiver channel.
- TX: Implements user data transmission, transmitting user data to SerDes.
- RX: Implements BCDR and transmits the received valid data to the user.
- OLT SFP: An OLT-specific optical module with TX 2.48832 Gbps and

RX 1.24416 Gbps.

3.2 BCDR Function

This IP implements the BCDR in the receive direction. According to the PON definition, OLT receives data in time-division multiplexing, with idle periods between frames. Traditional Clock Data Recovery (CDR) relies on continuous edge changes in the received data to ensure that the CDR can lock the data consistently. However, traditional CDR cannot quickly lock the burst data to meet the format requirements of the data received by OLT. This IP implements BCDR function, which allows the IP to lock the data upon receiving the preamble of each frame. It simultaneously transmits the valid data to the user, ensuring correct alignment and reception of the data on the user side.

3.3 User Interface

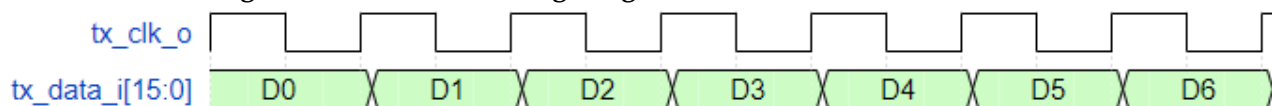
3.3.1 Transmit Data

The TX data width is 16 bits, with the LSB transmitted first. The descriptions of the TX port are as shown in Table 4-1.

The transmit timing diagram is as shown in Figure 3-2 . On the user side, data is continuously transmitted using tx_clk_o as the TX clock. The serial data output sequence is as follows:

D0[0],D0[1],D0[2].....,D0[15],D1[0],D1[1] ,D1[2].....,D1[15]
D6[0],D6[1],D6[2].....,D6[15]

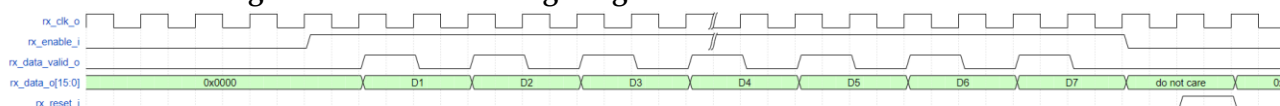
Figure 3-2 Transmit Timing Diagram



3.3.2 Receive Data

The RX data width is 16 bits, with the first received data at the LSB. The descriptions of the RX port are as shown in Table 4-1, and the receive timing diagram is as shown in Figure 3-3.

Figure 3-3 Receive Timing Diagram



The rx_clk_o clock frequency is 156.25 MHz, and all received data is synchronized to rx_clk_o. When the data is ready to be received, the user pulls rx_enable_i high to enable the BCDR function. While rx_enable_i is 1, rx_data_valid_o = 1 indicates that the rx_data_o data is valid. After the valid data has been received, the user pulls rx_enable_i low to disable the BCDR function. After a frame of data has been received, the user can pull rx_reset_i high for one cycle to clear the rx_data_o data to 0. The first received data in rx_data_o is at the LSB.

4 Port List

The IO port of Gowin BCDR IP is as shown in Figure 4-1.

Figure 4-1 Gowin BCDR IP IO Port Diagram

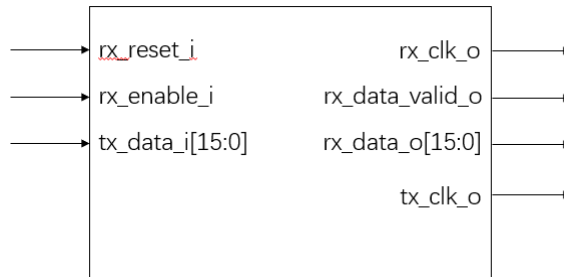


Table 4-1 Gowin BCDR IP IO Port List

Signal	I/O	Data Width	Description
TX Path			
tx_clk_o	output	1	Parallel data TX clock with a frequency of 155.52 MHz
tx_data_i	input	16	Transmits parallel data, synchronized to tx_clk_o, with the LSB transmitted first.
RX Path			
rx_clk_o	output	1	Parallel data RX clock with a frequency of 155.52 MHz
rx_data_valid_o	output	1	Reception parallel data valid indicator, synchronized to rx_clk_o. 1: Parallel data RX is valid 0: Parallel data RX is invalid
rx_data_o	output	16	Receives parallel data, synchronized to rx_clk_o, with the first received data at the LSB.
rx_enable_i	input	1	RX enable BCDR Set to 1 to enable the BCDR; set to 0 to disable the BCDR.
rx_reset_i	input	1	RX synchronous reset When the reset is active, rx_data_o outputs 0; when the reset is inactive, rx_data_o outputs valid data. This reset is active high.

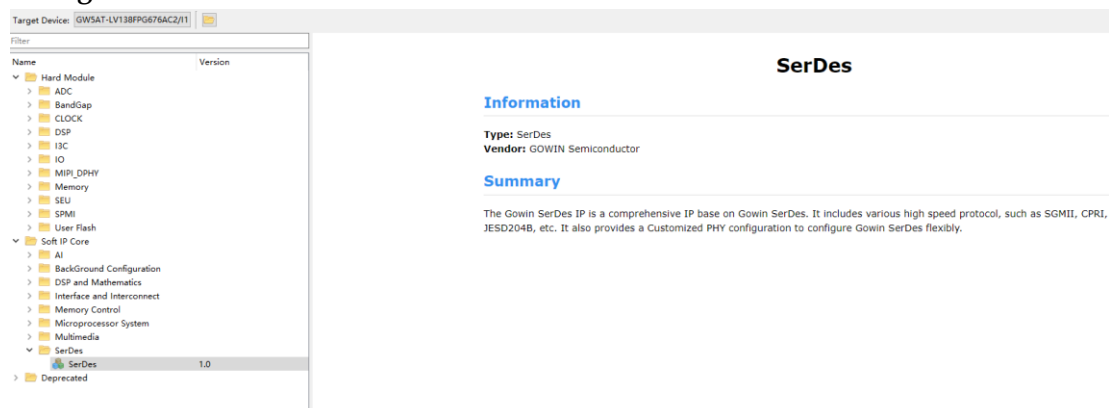
5 Interface Configuration

You can invoke and configure Gowin BCDR IP using the IP Core Generator tool in the IDE. This section will introduce the configuration interface, the configuration process, and the configuration options.

1. Open IP Core Generator

After creating the project, click the "Tools" tab in the upper left, click "IP Core Generator" to open Gowin IP Core Generator via the drop-down list, as shown in Figure 5-1.

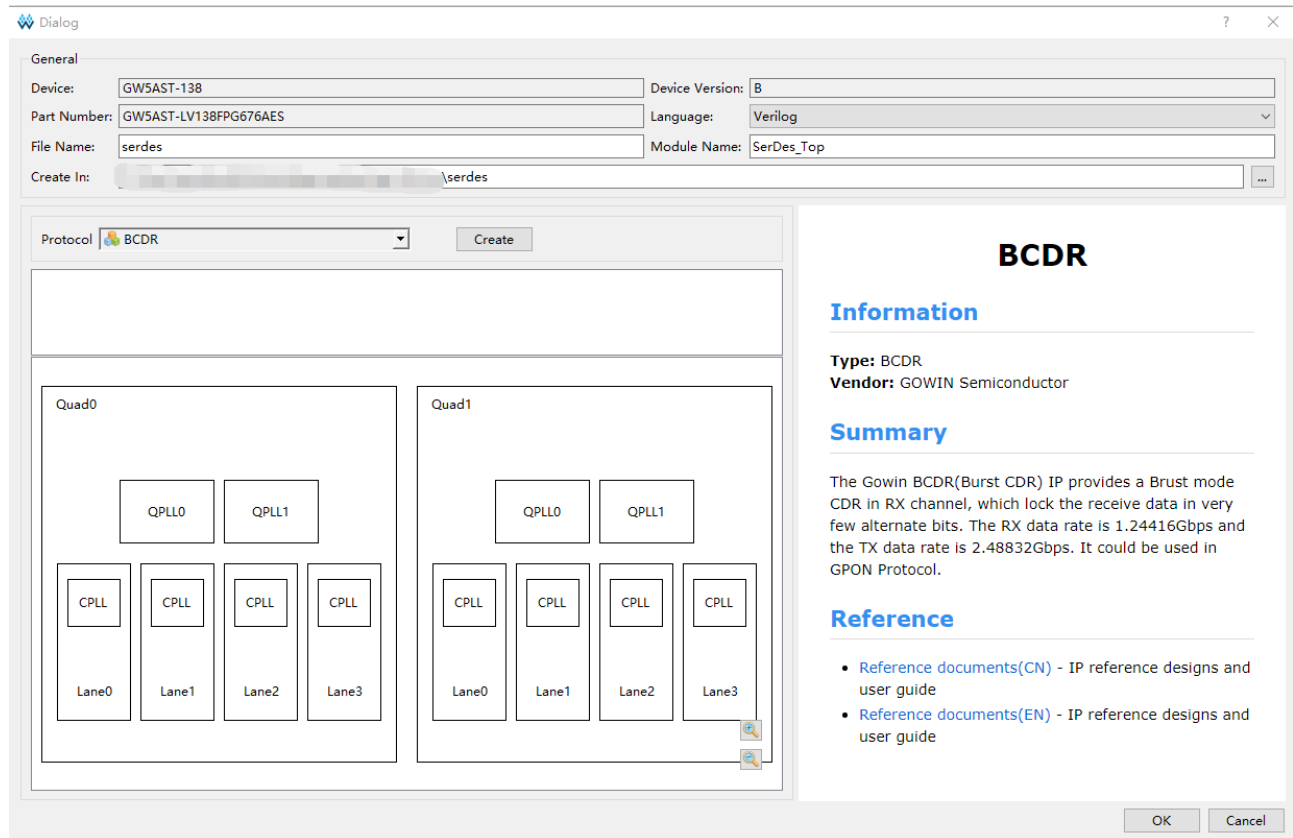
Figure 5-1 IP Core Generator



2. Open SerDes IP Configuration Interface

Select "SerDes" in IP Core Generator to open SerDes IP configuration interface, as shown in Figure 5-2.

Figure 5-2 SerDes IP Configuration Interface



First configure "General" tab in the SerDes IP interface.

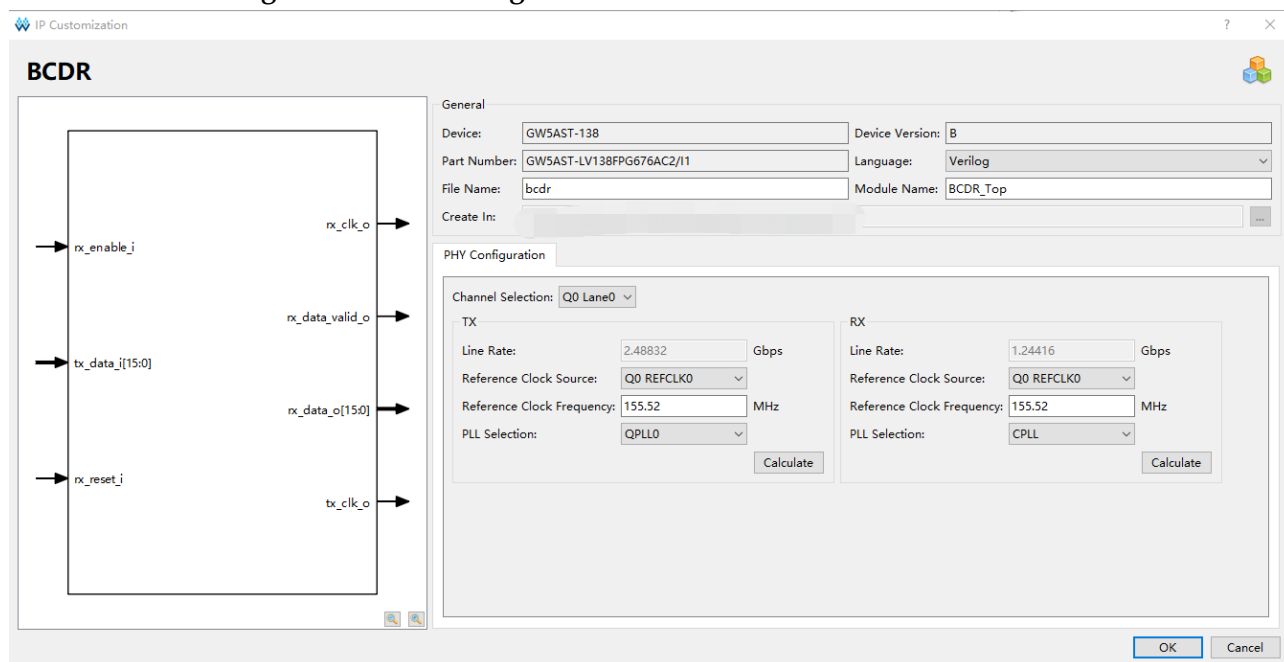
- Device, Device Version, Part Number: Used to set Part number, determined by the current project, and the user can not set it.
- Language: Support Verilog and VHDL; choose the language as requirements, and the default is Verilog.
- File Name, Module Name, Create In options: Used to set SerDes file name, module name and the generated file path.

You can select the protocol in "Protocol" option according to your needs. Click "Create" button on the right to open the protocol configuration, and it displays the current protocols supported by SerDes IP and the corresponding Quad, PLL and Lane usage; on the right side, it displays the information about the selected protocol, including "Information", "Summary", and "Reference".

3. Open BCDR IP Configuration Interface

Select "BCDR" in the "Protocol" option, and click "Create" button to open the BCDR IP configuration interface, as shown in Figure 5-3.

Figure 5-3 PHY Configuration



The BCDR port diagram is on the left, and the parameter configuration options are on the right.

Configure "PHY Configuration" tab as shown in Figure 5-3.

- Channel Selection: Select the required lane from the drop-down list, including eight lanes, Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2 and Q1 Lane3; if the lane is already in use, it will not be displayed.
- TX Options
 - Line Rate: The default rate is 2.48832Gbps, which cannot be configured.
 - Reference Clock Source: You can select REFCLK0 and REFCLK1 of Quad0, or REFCLK0 and REFCLK1 of Quad1.
 - Reference Clock Frequency: Used to configure the reference clock frequency.
 - PLL Selection: You can select QPLL0, QPLL1, and CPLL.
- RX Options
 - Line Rate: The default rate is 1.24416Gbps, which cannot be configured.
 - Reference Clock Source: You can select REFCLK0 and REFCLK1 of Quad0, or REFCLK0 and REFCLK1 of Quad1.
 - Reference Clock Frequency: Used to configure the reference clock frequency.
 - PLL Selection: You can select QPLL0 or CPLL.

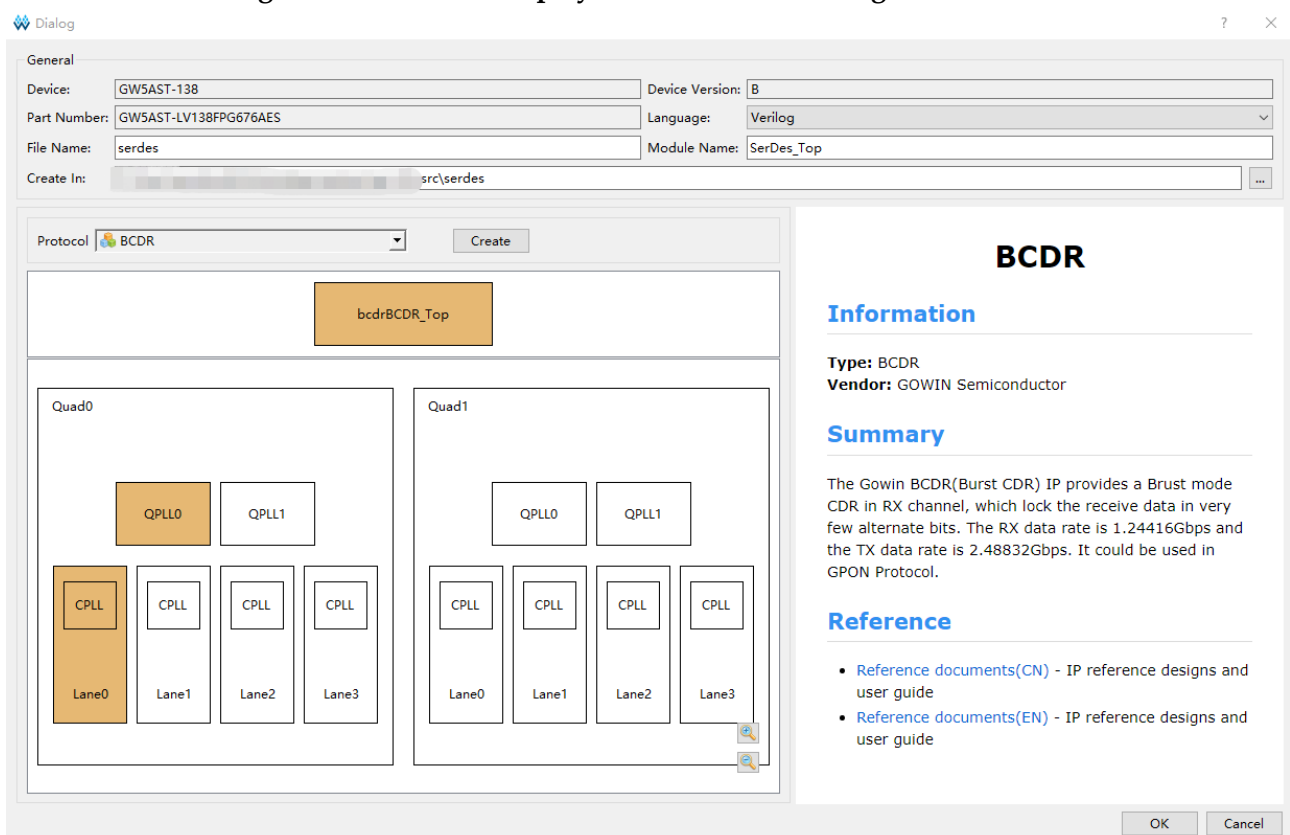
Note!

- There is a limitation between the line rate and the reference clock frequency. It is essential to ensure that the reference clock can generate the above line rate, which can also be verified using the "Calculate" button.
- It must select different PLLs in the PLL Selection options for TX and RX.
- It is recommended to choose the same clock source for the TX Reference Clock Source and the RX Reference Clock Source. In this configuration mode, tx_clk_o and rx_clk_o operate at the same frequency.

4. IP Generation

After completing BCDR IP configuration, click "OK" button at the bottom right corner of the interface to generate files of the BCDR IP, then return to the SerDes IP configuration interface, and then the SerDes IP configuration interface displays the current generated IP and the corresponding Quad, PLL, and Lane usage, as shown in Figure 5-4.

Figure 5-4 BCDR IP Displayed in SerDes IP Configuration Interface



Then, click "OK" button at the bottom right corner of the interface to generate SerDes IP files and complete the whole BCDR IP generation.

