



Gowin AHB to AHB 16 Bridge IP

User Guide

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Revision History

Date	Version	Description
07/30/2024	1.0E	Initial version published.
12/31/2024	1.1E	● The IP category updated from Bus Bridge to Bus Interconnect. ● The software programming reference design and hardware reference design updated.

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1 About This Guide

1.1 Purpose

The purpose of Gowin AHB to AHB 16 Bridge IP User Guide is to help you learn the features and usage of Gowin AHB to AHB 16 Bridge IP by providing the descriptions of the functions, signals, parameters, and reference design, etc. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.11 (64-bit). As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at www.gowinsemi.com:

- [SUG100, Gowin Software User Guide](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1104, GW5AST series of FPGA Products Data Sheet](#)

1.3 Terminology and Abbreviation

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
AHB	Advanced High Performance Bus
FPGA	Field Programmable Gate Array
IP	Intellectual Property
MCU	Micro Control Unit

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 IP Overview

Gowin AHB to AHB 16 Bridge IP includes 16 AHB slave device interfaces and 1 AHB master device interface. The master device interface can be connected to the AHB bus interface of MCU (e.g., the Extended AHB Slave of RiscV_AE350_SOC). Each of the 16 slave Interfaces can be connected to a slave device that has an AHB bus interface and thus acts as a peripheral to the master device MCU.

The base address of the AHB bus interface can be specified, which is the memory-mapped address of the AHB bus interface of the MCU used. The memory-mapped address size for each slave device interface can be configured, such as 1 MB, 2 MB, 4 MB, or 8 MB.

Table 2-1 Gowin AHB to AHB 16 Bridge IP Overview

Gowin AHB to AHB 16 Bridge IP	
Logic Resource	See Table 2-2
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog and C
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	● Gowin Software (V1.9.11 (64-bit) and above) ● RiscV_AE350_SOC RDS (V1.2 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features

The features of Gowin AHB to AHB 16 Bridge IP include:

- Supports up to 16 AHB slave device interfaces
- AHB bus base address can be specified
- Memory-mapped address size for each AHB slave device can be configured

2.3 Resource Utilization

Gowin AHB to AHB 16 Bridge IP can be implemented by Verilog language. Its performance and resource utilization may vary when the design is employed in different devices, or at different density, speed, or grade. Using Gowin GW5AST series of FPGA as an instance, the resource utilization of Gowin AHB to AHB 16 Bridge IP is as shown in Table 2-2.

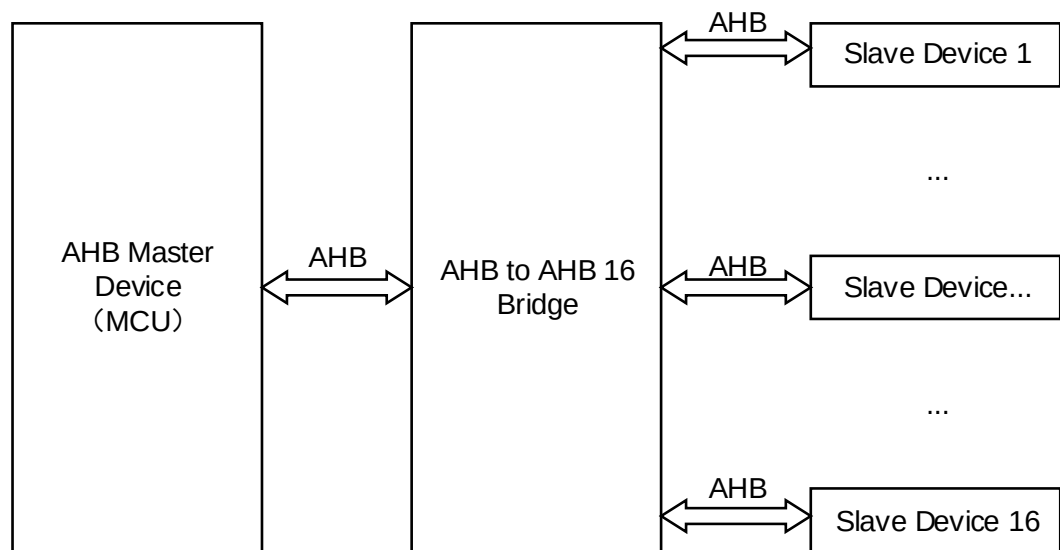
Table 2-2 Gowin AHB to AHB 16 Bridge IP Resource Utilization

Device	Speed Grade	Name	Resource Utilization	Note
GW5AST-138 Version B	C1/I0	LUT	48	Slave 1 and Slave 2
		REG	4	

3 Functional Description

Gowin AHB to AHB 16 Bridge IP includes 16 AHB Slave device interfaces and 1 AHB master device interface, as shown in Figure 3-1. The master device can be connected to MCU. Up to 16 AHB slave devices can be connected to the slave device interface, acting as a peripheral to the master device MCU.

Figure 3-1 Gowin AHB to AHB 16 Bridge IP Block Diagram



4 Port Description

The details of Gowin AHB to AHB 16 Bridge IP I/O ports are shown in Table 4-1.

Table 4-1 Gowin AHB to AHB 16 Bridge IP Port List

Signal Name	I/O	Width	Description	Note
hclk	input	1	Bus clock signal	-
hresetn	input	1	Bus reset signal	-
us_haddr	input	[31:0]	Bus address signal	-
us_hsel	input	1	Bus chip selected signal	-
us_htrans	input	[1:0]	Bus transmission type signal	-
us_hrdata	output	[31:0]	Bus read data signal	-
us_hready	input	1	Slave ready signal	-
us_hreadyout	output	1	Master ready signal	-
us_hresp	output	1	Bus transmission response signal	-
ds_hready	output	1	Master ready signal	-
ds0_hsel	output	1	The first slave chip selected signal	Slave 0
ds0_hrdata	input	[31:0]	The first slave read data signal	
ds0_hreadyout	input	1	The first slave ready signal	
ds0_hresp	input	1	The first slave transmission response signal	
ds1_hsel	output	1	The second slave chip selected signal	Slave 1
ds1_hrdata	input	[31:0]	The second slave read data signal	
ds1_hreadyout	input	1	The second slave ready signal	

Signal Name	I/O	Width	Description	Note
ds1_hresp	input	1	The second slave transmission response signal	
ds2_hsel	output	1	The third slave chip selected signal	Slave 2
ds2_hrdata	input	[31:0]	The third slave read data signal	
ds2_hreadyout	input	1	The third slave ready signal	
ds2_hresp	input	1	The third slave transmission response signal	
ds3_hsel	output	1	The fourth slave chip selected signal	Slave 3
ds3_hrdata	input	[31:0]	The fourth slave read data signal	
ds3_hreadyout	input	1	The fourth slave ready signal	
ds3_hresp	input	1	The fourth slave transmission response signal	
ds4_hsel	output	1	The fifth slave chip selected signal	Slave 4
ds4_hrdata	input	[31:0]	The fifth slave read data signal	
ds4_hreadyout	input	1	The fifth slave ready signal	
ds4_hresp	input	1	The fifth slave transmission response signal	
ds5_hsel	output	1	The sixth slave chip selected signal	Slave 5
ds5_hrdata	input	[31:0]	The sixth slave read data signal	
ds5_hreadyout	input	1	The sixth slave ready signal	
ds5_hresp	input	1	The sixth slave transmission response signal	
ds6_hsel	output	1	The seventh slave chip selected signal	Slave 6
ds6_hrdata	input	[31:0]	The seventh slave read data signal	
ds6_hreadyout	input	1	The seventh slave ready signal	
ds6_hresp	input	1	The seventh slave transmission response signal	
ds7_hsel	output	1	The eighth slave chip selected signal	Slave 7

Signal Name	I/O	Width	Description	Note
ds7_hrdata	input	[31:0]	The eighth slave read data signal	
ds7_hreadyout	input	1	The eighth slave ready signal	
ds7_hresp	input	1	The eighth slave transmission response signal	
ds8_hsel	output	1	The ninth slave chip selected signal	Slave 8
ds8_hrdata	input	[31:0]	The ninth slave read data signal	
ds8_hreadyout	input	1	The ninth slave ready signal	
ds8_hresp	input	1	The ninth slave transmission response signal	
ds9_hsel	output	1	The tenth slave chip selected signal	Slave 9
ds9_hrdata	input	[31:0]	The tenth slave read data signal	
ds9_hreadyout	input	1	The tenth slave ready signal	
ds9_hresp	input	1	The tenth slave transmission response signal	
ds10_hsel	output	1	The eleventh slave chip selected signal	Slave 10
ds10_hrdata	input	[31:0]	The eleventh slave read data signal	
ds10_hreadyout	input	1	The eleventh slave ready signal	
ds10_hresp	input	1	The eleventh slave transmission response signal	
ds11_hsel	output	1	The twelfth slave chip selected signal	Slave 11
ds11_hrdata	input	[31:0]	The twelfth slave read data signal	
ds11_hreadyout	input	1	The twelfth slave ready signal	
ds11_hresp	input	1	The twelfth slave transmission response signal	
ds12_hsel	output	1	The thirteenth slave chip selected signal	Slave 12
ds12_hrdata	input	[31:0]	The thirteenth slave read data signal	
ds12_hreadyout	input	1	The thirteenth slave ready signal	

Signal Name	I/O	Width	Description	Note
ds12_hresp	input	1	The thirteenth slave transmission response signal	
ds13_hsel	output	1	The fourteenth slave chip selected signal	Slave 13
ds13_hrdata	input	[31:0]	The fourteenth slave read data signal	
ds13_hreadyout	input	1	The fourteenth slave ready signal	
ds13_hresp	input	1	The fourteenth slave transmission response signal	
ds14_hsel	output	1	The fifteenth slave chip selected signal	Slave 14
ds14_hrdata	input	[31:0]	The fifteenth slave read data signal	
ds14_hreadyout	input	1	The fifteenth slave ready signal	
ds14_hresp	input	1	The fifteenth slave transmission response signal	
ds15_hsel	output	1	The sixteenth slave chip selected signal	Slave 15
ds15_hrdata	input	[31:0]	The sixteenth slave read data signal	
ds15_hreadyout	input	1	The sixteenth slave ready signal	
ds15_hresp	input	1	The sixteenth slave transmission response signal	

5 Parameter Description

The ports of Gowin AHB to AHB 16 Bridge IP are as shown in Table 5-1.

Table 5-1 Parameter Description

Name	Description	Value
Bus Base Address	Memory-mapped address of the master device AHB bus interface	32-bit address
Slave Address Size	Memory-mapped address size for slave device	1/2/4/8 MB
Slave 0	AHB bus interface for the first slave	Enable/Disable
Slave 1	AHB bus interface for the second slave	Enable/Disable
Slave 2	AHB bus interface for the third slave	Enable/Disable
Slave 3	AHB bus interface for the fourth slave	Enable/Disable
Slave 4	AHB bus interface for the fifth slave	Enable/Disable
Slave 5	AHB bus interface for the sixth slave	Enable/Disable
Slave 6	AHB bus interface for the seventh slave	Enable/Disable
Slave 7	AHB bus interface for the eighth slave	Enable/Disable
Slave 8	AHB bus interface for the ninth slave	Enable/Disable
Slave 9	AHB bus interface for the tenth slave	Enable/Disable
Slave 10	AHB bus interface for the eleventh slave	Enable/Disable
Slave 11	AHB bus interface for the twelfth slave	Enable/Disable
Slave 12	AHB bus interface for the thirteenth slave	Enable/Disable
Slave 13	AHB bus interface for the fourteenth slave	Enable/Disable
Slave 14	AHB bus interface for the fifteenth	Enable/Disable

Name	Description	Value
	slave	
Slave 15	AHB bus interface for the sixteenth slave	Enable/Disable

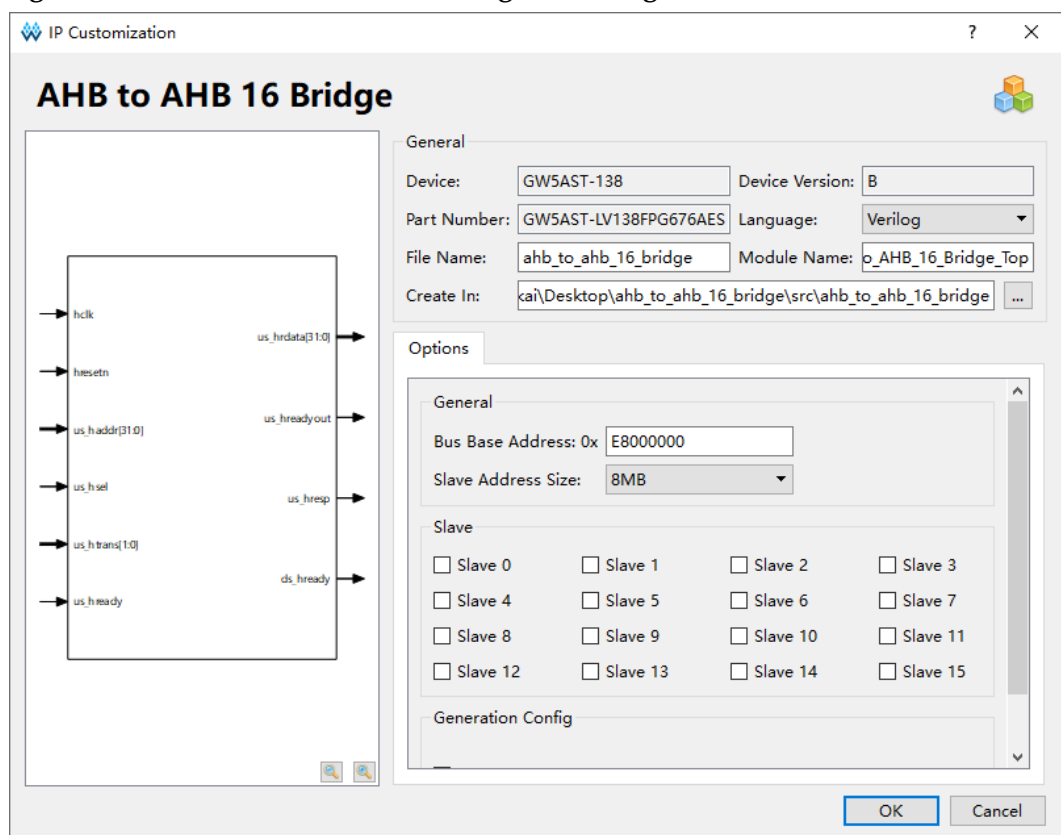
6 Interface Configuration

You can select IP Core Generator Tool in Gowin Software to call and configure Gowin AHB to AHB 16 Bridge IP.

Select "Tools > IP Core Generator" on the menu bar or click the "🧩" on the tool bar to open IP Core Generator; then select "Soft IP Core > Microprocessor System > Bus Interconnect > AHB to AHB 16 Bridge 1.1".

Gowin AHB to AHB 16 Bridge IP interface configuration is as shown in Figure 6-1.

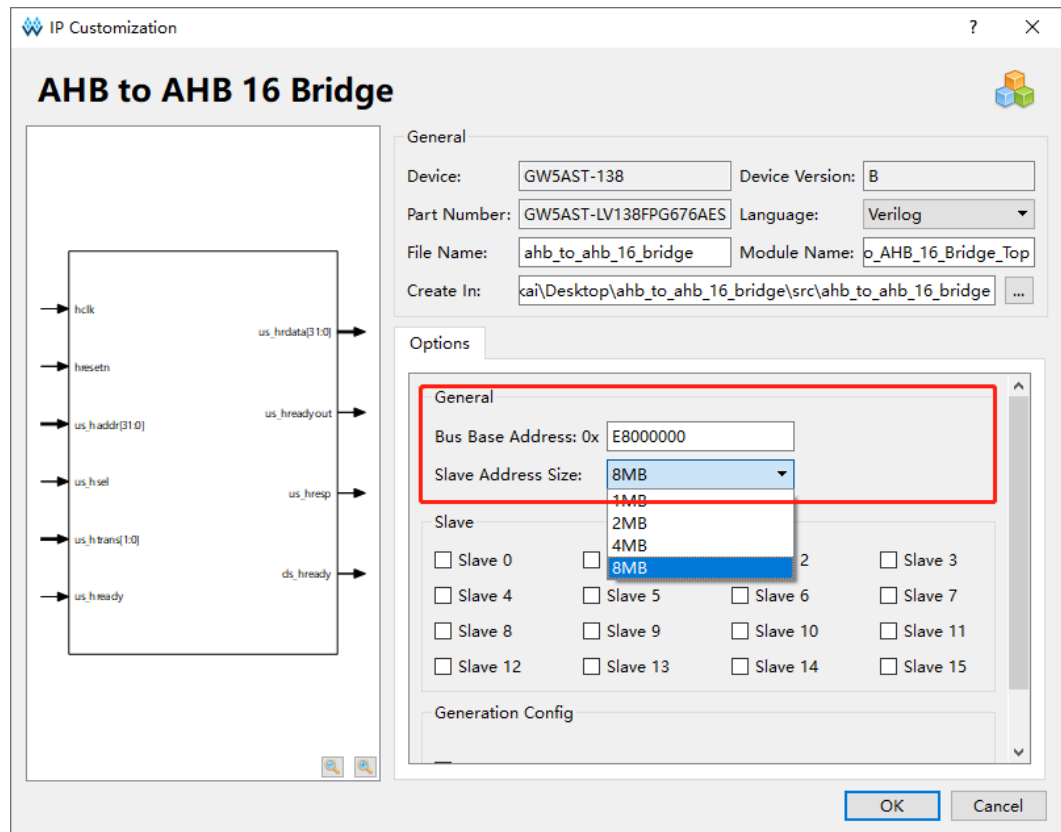
Figure 6-1 Gowin AHB to AHB 16 Bridge IP Configuration Interface



6.1 General Configuration

General configuration includes the "Bus Base Address" option and the "Slave Address Size" options, as shown in Figure 6-2.

Figure 6-2 General Configuration



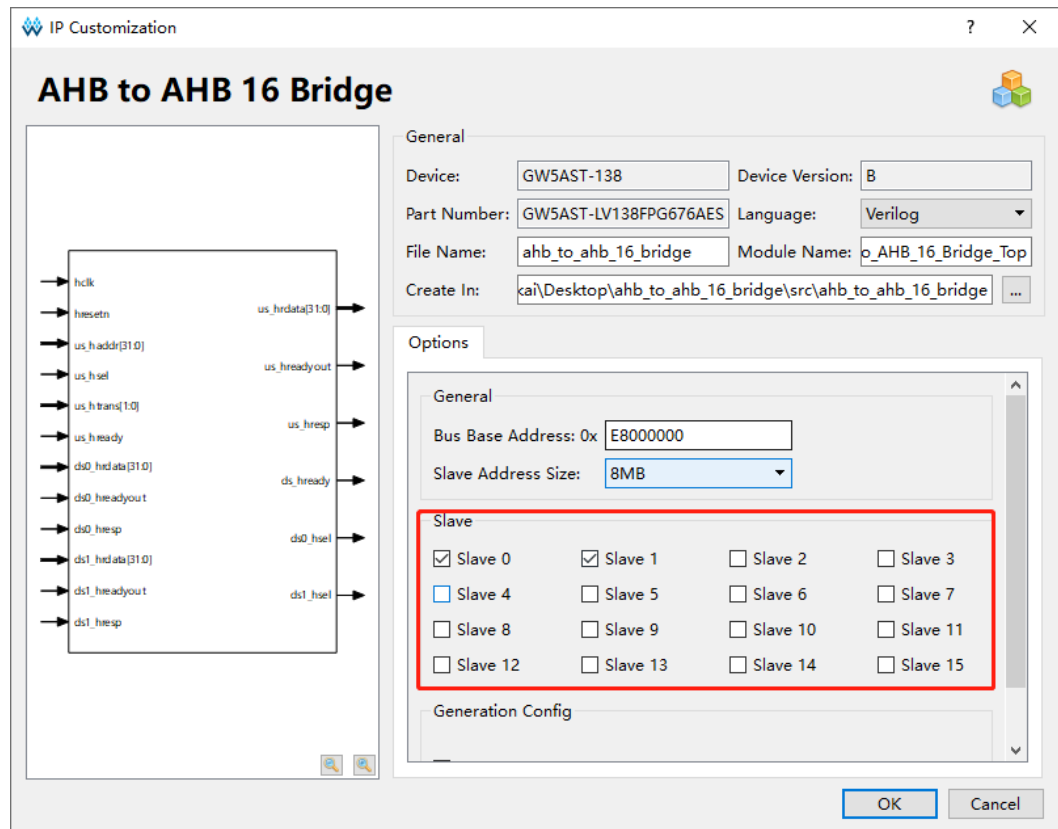
The Bus Base Address is used to specify the memory-mapped address of the AHB bus interface of the accessed master device (MCU), and the default is 0xE8000000 (the memory-mapped address of the Extended AHB Slave of RiscV_AE350_SOC), and it can be modified with reference to the application requirements.

Slave Address Size is used to configure the memory-mapped address size for each slave device, including 1 MB, 2 MB, 4 MB, and 8 MB, and the default is 8 MB.

6.2 Slave Configuration

Slave configuration includes 16 AHB bus interfaces for slave devices Slave 0~15, which are used to connect to 16 slave devices as AHB peripherals to the master device (MCU), as shown in Figure 6-3.

Figure 6-3 Slave Configuration



- If "Slave 0" is selected, the AHB bus interface of the first slave device is enabled, and it is disabled by default.
- If "Slave 1" is selected, the AHB bus interface of the second slave device is enabled, and it is disabled by default.
- If "Slave 2" is selected, the AHB bus interface of the third slave device is enabled, and it is disabled by default.
- If "Slave 3" is selected, the AHB bus interface of the fourth slave device is enabled, and it is disabled by default.
- If "Slave 4" is selected, the AHB bus interface of the fifth slave device is enabled, and it is disabled by default.
- If "Slave 5" is selected, the AHB bus interface of the sixth slave device is enabled, and it is disabled by default.
- If "Slave 6" is selected, the AHB bus interface of the seventh slave device is enabled, and it is disabled by default.

device is enabled, and it is disabled by default.

- If "Slave 7" is selected, the AHB bus interface of the eighth slave device is enabled, and it is disabled by default.
- If "Slave 8" is selected, the AHB bus interface of the ninth slave device is enabled, and it is disabled by default.
- If "Slave 9" is selected, the AHB bus interface of the tenth slave device is enabled, and it is disabled by default.
- If "Slave 10" is selected, the AHB bus interface of the eleventh slave device is enabled, and it is disabled by default.
- If "Slave 11" is selected, the AHB bus interface of the twelfth slave device is enabled, and it is disabled by default.
- If "Slave 12" is selected, the AHB bus interface of the thirteenth slave device is enabled, and it is disabled by default.
- If "Slave 13" is selected, the AHB bus interface of the fourteenth slave device is enabled, and it is disabled by default.
- If "Slave 14" is selected, the AHB bus interface of the fifteenth slave device is enabled, and it is disabled by default.
- If "Slave 15" is selected, the AHB bus interface of the sixteenth slave device is enabled, and it is disabled by default.

7 Reference Design

See Gowin AHB to AHB 16 Bridge IP [Reference Design](#) for details at Gowinsemi website.

- Hardware Reference Design:
 ...\ref_design\FPGA_RefDesign\DK_START_GW5AST138_V1.0\ahb_to_ahb_16_bridge
- Software Programming Reference Design:
 ...\ref_design\MCU_RefDesign\ahb_to_ahb_16_bridge

