



Gowin DDS II IP

User Guide

IPUG1041-1.0E, 07/30/2024

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Revision History

Date	Version	Description
07/30/2024	1.0E	Initial version published.

Contents

Contents	i
List of Figures	iii
List of Tables	iv
1 About This Guide	1
1.1 Purpose	1
1.2 Related Documents	1
1.3 Terminology and Abbreviations	1
1.4 Support and Feedback	2
2 Function Overview	3
2.1 Overview	3
2.2 Features	3
2.3 Resource Utilization	4
3 Functional Description	5
3.1 System Block Diagram	5
3.2 Port List	6
3.3 Interface Timing	8
3.3.1 CONFIG Interface	8
3.3.2 PHASE Interface	9
3.3.3 OUTPUT Interface	9
4 Design Notes	10
4.1 Basic Principles	10
4.1.1 Phase Truncation DDS	10
4.1.2 Phase Dithered DDS	12
4.1.3 Taylor Series Corrected DDS	14
4.2 DDS Type Selection	14
4.3 Multi-channel Design	15
4.4 Latency	15
4.5 Parameter Conversion	16
5 Interface Configuration	17
6 Reference Design	22
6.1 Reference Design	22

6.2 Operating Flow 22

7 File Delivery 23

7.1 Documentation..... 23

7.2 Design Source Code (Encryption) 23

7.3 Reference Design 23

List of Figures

Figure 3-1 Gowin DDS II IP Structure Diagram	5
Figure 3-2 Gowin DDS II IP Port Diagram	7
Figure 3-3 CONFIG Interface Timing	8
Figure 3-4 Flash Interface Timing	9
Figure 3-5 OUTPUT Interface Timing	9
Figure 4-1 Phase Truncation DDS Structure Diagram	10
Figure 4-2 SFDR Simulation Analysis when $N = 27$, $M = 16$, $D = 16$	12
Figure 4-3 SFDR Simulation Analysis when $N = 27$, $M = 16$, $D = 20$	12
Figure 4-4 Phase Truncation DDS SFDR Simulation Analysis when $N = 27$, $M = 16$, $D = 16$	13
Figure 4-5 Phase Dithered DDS SFDR Simulation Analysis when $N = 27$, $M = 14$, $D = 16$	13
Figure 4-6 Taylor Series Corrected DDS Simulation Analysis when $N = 27$, $M=22$ (SFDR = 132dB)	14
Figure 4-7 Noise Shaping Area Diagram	15
Figure 4-8 Output Delay Diagram	16
Figure 5-1 Open DDS II IP	17
Figure 5-2 Implementation Tab	18
Figure 5-3 System Parameters Selected	20
Figure 5-4 Hardware Parameters Selected	21
Figure 6-1 Capture DDS Data	22
Figure 6-2 Waveform Reading and Analysis	22

List of Tables

Table 1-1 Terminology and Abbreviations	1
Table 2-1 Gowin DDS II IP Overview	3
Table 2-2 Gowin DDS II IP Resource Utilization	4
Table 3-1 I/O List	7
Table 7-1 Document List	23
Table 7-2 Gowin DDS II IP Design Source Code List	23
Table 7-3 Gowin DDS II IP RefDesign Folder Content List.....	23

1 About This Guide

1.1 Purpose

The purpose of Gowin DDS II IP User Guide is to help you learn the features and usage of Gowin DDS II IP by providing the descriptions of functions, GUI, and reference design, etc. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.9 Beta-3. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find related documents at www.gowinsemi.com

- [SUG100, Gowin Software User Guide](#)
- [DS1228, Arora V FPGA Products Overview](#)
- [DS981, Arora V 138K & 75K FPGA Products Data Sheet](#)

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
DDS	Direct Digital Synthesizer
FPGA	Field Programmable Gate Array
FSK	Frequency Shift Keying
IP	Intellectual Property
LUT	Look-up Table
NCO	Numerically Controlled Oscillator
PINC	Phase Increment
POFF	Phase Offset
PSK	Phase Shift Keying

Terminology and Abbreviations	Meaning
SFDR	Spurious Free Dynamic Range

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Function Overview

2.1 Overview

The Direct Digital Synthesizer (DDS) or Numerically Controlled Oscillator (NCO) is a critical component in many digital communication systems. Quadrature synthesizers are used to construct digital downconverters and upconverters, demodulators, and implement various types of modulation schemes, including Phase Shift Keying (PSK) and Frequency Shift Keying (FSK). Look-up tables are commonly used for digitally generating complex or real sine waves. The look-up table stores samples of the sine wave. A digital integrator is used to generate the appropriate phase variable, which the look-up table maps to the desired waveform. A simple user interface provides system-level parameters, such as the desired output frequency and the spurious suppression of the generated waveform.

Table 2-1 Gowin DDS II IP Overview

Gowin DDS II IP	
Logic Resource	See Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9.Beta-3 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features

- Phase generator and SIN/COS look-up table can be generated separately or together with optional dithering to provide a complete DDS solution
- Supports sine, cosine or quadrature output
- Optional per-channel cumulative phase resynchronization

- Optional phase dithering can expand spectral line energy to achieve greater spurious-free dynamic range (SFDR)
- Phase dithering or Taylor series correction options provide high dynamic range signals with minimal FPGA resources, supporting SFDR from 24dB to 150dB
- Up to 16 independent time-division multiplexing channels
- Use up to 48-bit phase accumulator to achieve fine frequency resolution
- Supports 4-bit to 25-bit signed output sample precision

2.3 Resource Utilization

Gowin DDS II IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW5AT series of FPGA as an instance, the resource utilization of Gowin DDS II IP is as shown in Table 2-2.

Table 2-2 Gowin DDS II IP Resource Utilization

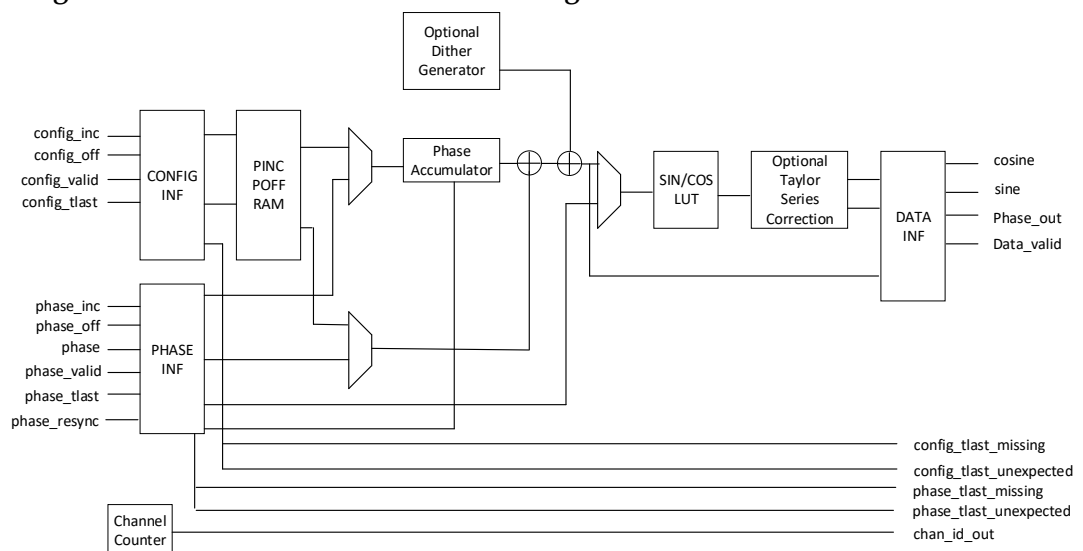
Setting	Noise Shaping	Resource					
		Register	LUT	ALU	BSRAM	SSRAM	DSP
Clock:100MHz channels: 1 SFDR:96dB Freq Resolution:1Hz	None	580	266	54	15	0	0
	Phase Dither	645	274	81	4	0	0
	Taylor Series Corrected	646	312	86	1	0	3

3 Functional Description

3.1 System Block Diagram

The structure diagram of Gowin DDS II IP is shown in Figure 3-1.

Figure 3-1 Gowin DDS II IP Structure Diagram



Phase Generator

The phase generator consists of an accumulator and an optional adder for providing phase offset addition. Phase increment (PINC) and phase offset (POFF) can be independently configured as fixed, programmable (using the CONFIG interface), or streaming (using the input PHASE interface).

- When PINC or POFF is set to fixed, the DDS output frequency is set in the GUI and cannot be adjusted after configuration.
- When PINC or POFF is set to programmable, the CONFIG interface is used to configure PINC or POFF. If neither PINC nor POFF is set to programmable, there is no CONFIG interface.
- When PINC or POFF is set to streaming, the PHASE interface is used to configure PINC or POFF. If neither PINC nor POFF is set to

streaming, there is no PHASE interface.

- When PINC is set to streaming, an optional phase_resync can be configured. When phase_resync is high, the accumulated phase of the corresponding channel will be reset.

When using system parameters, PINC and POFF are not directly input but are calculated based on the output frequency and phase angle. Note that when the calculated PINC and POFF are not integers, rounding will occur, resulting in some error between the actual output frequency and phase angle and the inputted output frequency and phase angle.

SIN/COS LUT

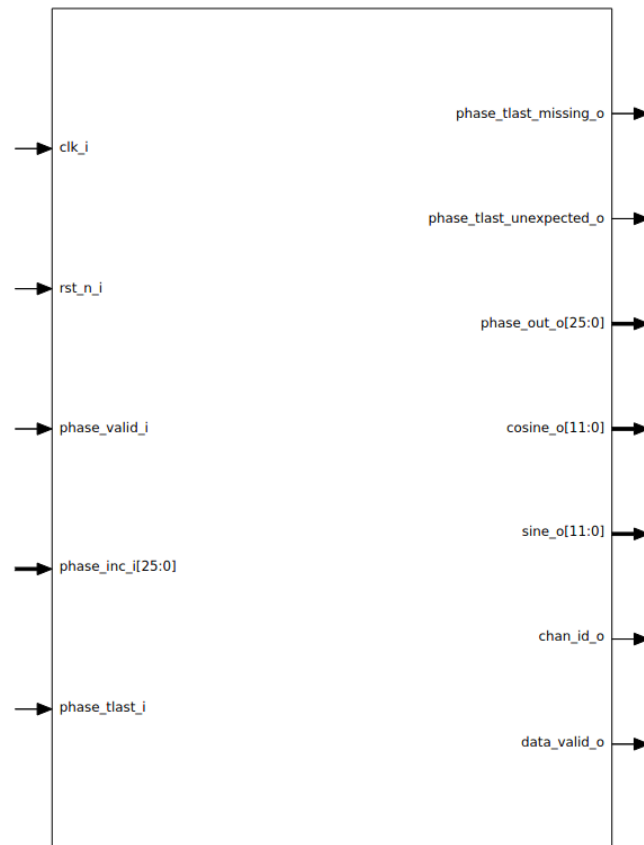
When configured as SIN/COS LUT Only, the phase generator is not implemented. The phase is input through the PHASE interface's phase port, and the look-up table converts it to sine and cosine outputs. Efficient memory usage is achieved by exploiting the symmetry of the sine waveform. The core can be configured for sine output only, cosine output only, or both (quadrature) outputs. Optional Taylor series correction can improve accuracy by utilizing DSP resources on the FPGA, supporting higher SFDR.

Phase Generator and SIN/COS LUT (DDS)

The phase generator, combined with the SIN/COS LUT, can provide phase-truncated DDS or Taylor series corrected DDS. An optional dithering generator can be added between the two blocks to achieve phase-dithered DDS.

3.2 Port List

Gowin DDS II IP has different ports depending on the configuration mode. The IO ports of Gowin DDS II IP are as shown in Figure 3-2.

Figure 3-2 Gowin DDS II IP Port Diagram**Table 3-1 I/O List**

Signal Name	I/O	Description
<code>clk_i</code>	IN	System clock
<code>rst_n_i</code>	IN	Reset signal 0: Reset 1: Operating
<code>phase_valid_i</code>	IN	PHASE interface input valid, active-high
<code>phase_i[N^[1]-1 : 0]</code>	IN	Directly setting the phase, and it only exists when set to SIN/COS LUT Only mode.
<code>phase_inc_i[N^[1]-1 : 0]</code>	IN	Used to set phase increment
<code>phase_off_i[N^[1]-1 : 0]</code>	IN	Used to set phase offset
<code>phase_resync_i</code>	IN	Used to reset the phase accumulator, active when it is set to 1.
<code>phase_tlast_i</code>	IN	Exists when set to multi-channel mode; indicates the last channel.
<code>phase_tlast_missing_o</code>	OUT	Exists when set to multi-channel mode; sets to 1 if <code>phase_tlast_i</code> is missing.
<code>phase_tlast_unexpected_o</code>	OUT	Exists when set to multi-channel mode; sets to 1 if <code>phase_tlast_i</code> is misplaced.
<code>config_valid_i</code>	IN	CONFIG interface input valid, active-high
<code>config_inc_i[N^[1]-1 : 0]</code>	IN	Used to set phase increment

Signal Name	I/O	Description
config_off_i[N ^[1] -1 : 0]	IN	Used to set phase offset
config_tlast_i	IN	Exists when set to multi-channel mode; indicates the last channel.
config_tlast_missing_o	OUT	Exists when set to multi-channel mode; sets to 1 if config_tlast_i is missing.
config_tlast_unexpected_o	OUT	Exists when set to multi-channel mode; sets to 1 if config_tlast_i is misplaced.
data_valid_o	OUT	Data output, active-high
phase_out_o[N ^[1] -1 : 0]	OUT	Phase output
cosine_o[D ^[2] -1 : 0]	OUT	Cosine signal output
sine_o[D ^[2] -1 : 0]	OUT	Sine signal output
chan_id_o[ceil(log2(X ^[3]))-1 : 0]	OUT	Optional channel ID output in multi-channel mode

Note!

^[1] N indicates the bit width of phase accumulator.

^[2] D indicates the bit width of output sine and cosine signal.

^[3] X indicates the number of channels.

3.3 Interface Timing

3.3.1 CONFIG Interface

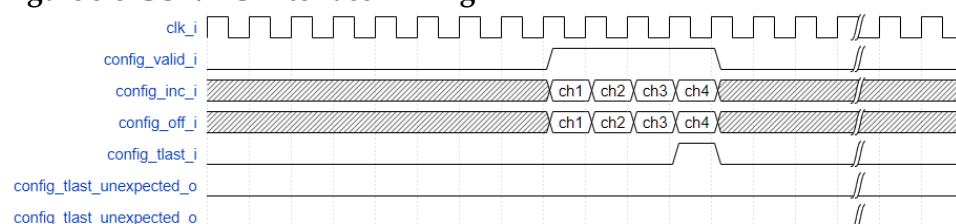
The CONFIG interface includes signals such as config_valid_i, config_inc_i, config_off_i, config_tlast_i, config_tlast_missing_o, and config_tlast_unexpected_o.

This interface exists only when either PINC or POFF is configured as Programmable, and config_tlast_i, config_tlast_missing_o, and config_tlast_unexpected_o exists only in multi-channel mode.

To program the CONFIG channel, N transmissions must be performed, where N is the number of channels. Each transmission includes the PINC and/or POFF values for each channel, starting from channel 0. For only the last transmission for the channel (index N-1), tlast must be set. Failure to do so will cause the config_tlast_missing or config_tlast_unexpected outputs to be set within one cycle.

The CONFIG interface is non-blocking, meaning output signals will not stop during configuration. The CONFIG interface is suitable for applications where PINC and POFF changes are infrequent, such as system mode switching or frequency switching.

Figure 3-3 CONFIG Interface Timing



3.3.2 PHASE Interface

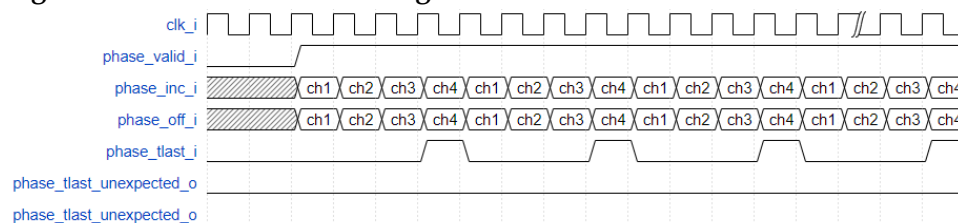
The PHASE interface includes signals such as `phase_valid_i`, `phase_inc_i`, `phase_off_i`, `phase_tlast_i`, `phase_tlast_missing_o`, `phase_tlast_unexpected_o`, and a `phase_i` signal exists only in COS SIN LUT Only mode.

This interface exists only when either PINC or POFF is configured as Streaming, and `phase_tlast_i`, `phase_tlast_missing_o`, `phase_tlast_unexpected_o` exists only in multi-channel mode.

To program the PHASE channel, N cycles of transmissions are required, where N is the number of channels. Each transmission includes the PINC and/or POFF values for each channel, starting from channel 0. For only the last transmission for the channel (index N-1), `tlast` must be set. Failure to do so will cause the `phase_tlast_missing` and `phase_tlast_unexpected` outputs to be set within one cycle.

The PHASE interface is suitable for applications where the DDS compiler performs dynamic functions such as phase or frequency modulation, with real-time changes in PINC or POFF, and each input sample corresponds to an output sample. There is a one-to-one relationship between input and output, indicating that invalid input data on the PHASE channel will transfer as invalid output data on the output channel.

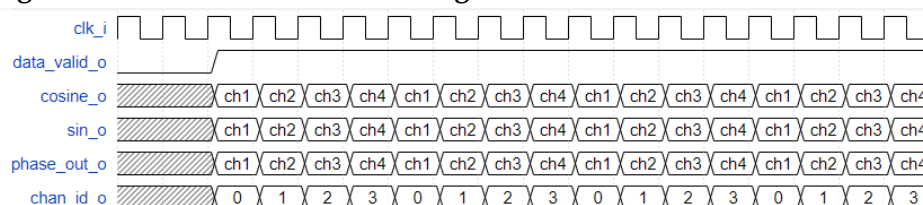
Figure 3-4 Flash Interface Timing



3.3.3 OUTPUT Interface

The OUTPUT interface includes signals such as `data_valid_o`, `cosine_o`, `sine_o`, `phase_out_o`, and `chan_id_o`; `cosine_o`, `sine_o`, `phase_out_o`, and `chan_id_o` are optional outputs, and `chan_id_o` is optional only in multi-channel configuration.

Figure 3-5 OUTPUT Interface Timing



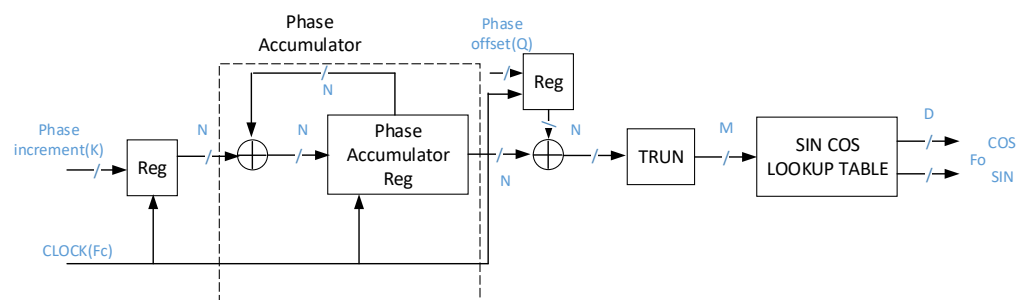
4 Design Notes

4.1 Basic Principles

4.1.1 Phase Truncation DDS

The structure of Phase Truncation DDS is illustrated in the figure below, which represents the most fundamental DDS structure.

Figure 4-1 Phase Truncation DDS Structure Diagram



In the diagram, F_c represents the reference clock frequency for each channel; K denotes the frequency increment, also known as the frequency control word; N signifies the bits of the phase accumulator; M indicates the bits used for addressing the waveform look-up table memory; F_o is the frequency of the DDS output orthogonal signal, and D represents the amplitude bit width of the output signal.

1. DDS Frequency Resolution

Frequency resolution is a function of the DDS operating clock and the width of the accumulator. When the operating clock is fixed, the width of the accumulator determines the DDS frequency resolution. To achieve higher frequency resolution, an accumulator with sufficiently width is required. The formula for frequency resolution is as follows:

$$\Delta f = F_c / 2^N$$

For example, if $F_c = 100$ MHz and $N = 27$, then $\Delta f = 0.745$ Hz

2. DDS Output Frequency

The formula for DDS output frequency is as follows:

$$F_o = F_c \cdot K / 2^N$$

Due to the constraints of frequency resolution, the set output frequency may deviate from the actual output frequency, but not by more than $\Delta f / 2$.

3. DDS Spectral Purity

There are 2 sources of spuriousness in DDS.

- The first is Phase truncation. To achieve high frequency resolution, the width of the phase accumulator N is typically large. However, due to the limited capacity of the waveform look-up table memory, the bits of M used for addressing is typically smaller than the N . Phase truncation produces phase dither, resulting in phase truncation errors. Phase truncation errors generate numerous harmonic signals, resulting in discrete spurious spectral lines. The maximum spuriousness is determined by M , approximately equal to $6 \times M$.
- The second is amplitude quantization. The orthogonal amplitude values stored in the waveform look-up table are represented in binary format. Values exceeding M bits require quantization, introducing quantization error. Quantization typically uses rounding, and amplitude quantization error appears as background noise in the DDS output spectrum. The empirical formula $\text{SNR}(\text{dB}) = 6.02 \times D + 1.76$ can be used for estimation.

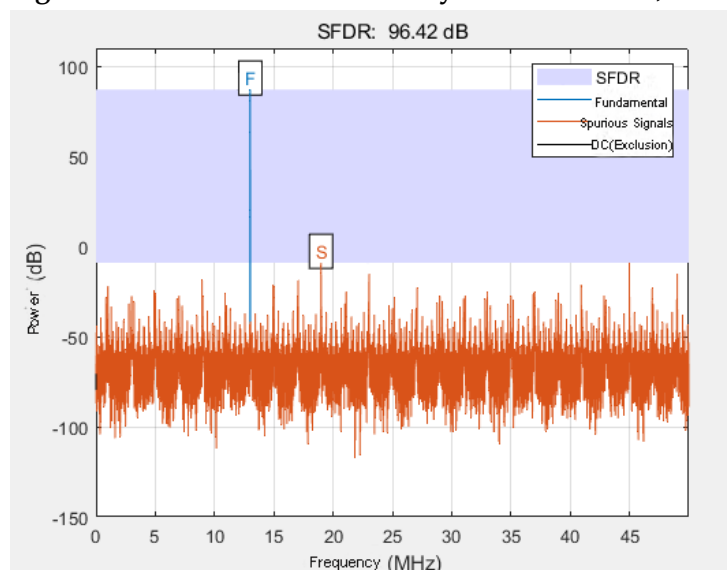
In summary, if the desired SFDR of DDS is Q , then $M = \text{ceil}(Q/6)$ and approximately $D = \text{ceil}(Q/6)$.

Assuming a required DDS frequency resolution of 1 Hz and SFDR = 96 dB, with a DDS channel operating clock of 100 MHz, the required width of the accumulator N is as follows:

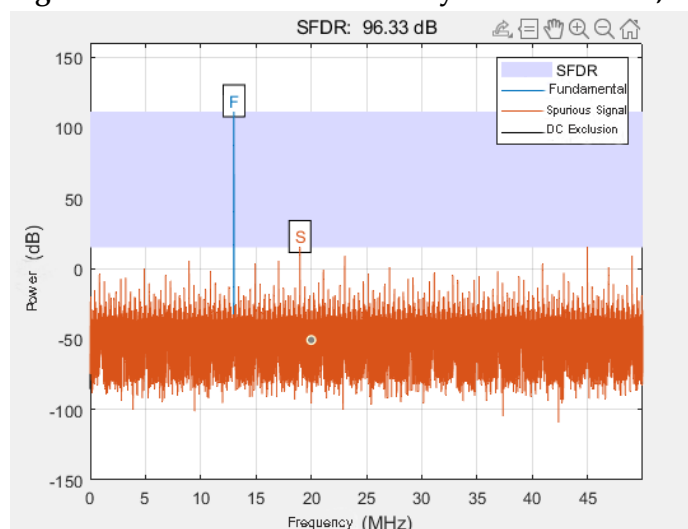
$$N = \text{ceil}(\log_2(10^8/1)) = 27.$$

Due to excessive data storage, it is challenging to use a full-precision phase accumulator as an index address for the waveform look-up table. A look-up table with a width of 27 bits has a depth of 2^{27} . Therefore, based on the SFDR requirement of 96, you can derive $M = 16$ and $D = 16$.

When $N = 27$, $M = 16$, and $D = 16$, the SFDR simulation analysis is shown in the following figure.

Figure 4-2 SFDR Simulation Analysis when $N = 27$, $M = 16$, $D = 16$ 

When $N = 27$, $M = 16$, and $D = 20$, the SFDR simulation analysis is shown in the following figure.

Figure 4-3 SFDR Simulation Analysis when $N = 27$, $M = 16$, $D = 20$ 

From the two figures above, it can be observed that both SFDR values are equal to 96. This indicates that phase truncation DDS can not improve SFDR performance by increasing the output magnitude bit width.

4.1.2 Phase Dithered DDS

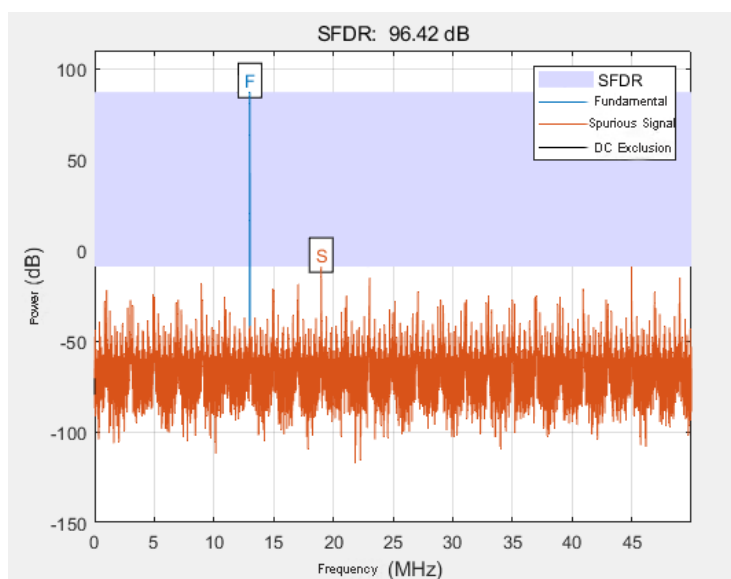
Phase Dithered DDS is an optimization of Phase Truncation DDS. The phase truncation error in Phase Truncation DDS has a periodicity, and if its periodicity can be disrupted, the level of spuriousness in DDS can be reduced. Phase Dithered DDS primarily transforms the periodic, regular, and deterministic spurious signals into random, irregular phase noise. This is achieved by adding a random signal with certain statistical characteristics to the output of the phase accumulator every clock cycle, thereby disrupting the periodic nature of the phase error.

Compared to Phase Truncation DDS design, dithered DDS provides an additional SFDR of 12 dB or higher. This is achieved by spreading the spectral energy of the phase error signal, and the additional logic resources required to implement the dither sequence generator are minimal.

If the desired SFDR of the DDS is Q , when using Phase Dithered DDS, $M = \text{ceil}(Q/6) - 2$ and $D = \text{ceil}(Q/6)$.

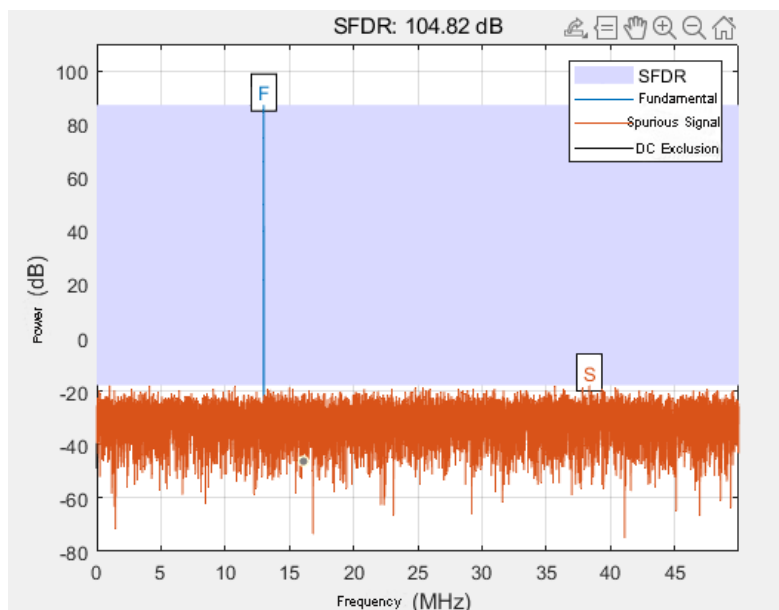
When $N = 27$, $M = 16$, and $D = 16$, Phase Truncation DDS SFDR simulation analysis is shown in the following figure.

Figure 4-4 Phase Truncation DDS SFDR Simulation Analysis when $N = 27$, $M = 16$, $D = 16$



When $N = 27$, $M = 14$, and $D = 16$, Phase Dithered DDS SFDR simulation analysis is shown in the following figure.

Figure 4-5 Phase Dithered DDS SFDR Simulation Analysis when $N = 27$, $M = 14$, $D = 16$



For $N = 27$, $M = 16$, $D = 16$, 15 BSRAMs are required for compilation in GW5AT FPGAs.

For $N = 27$, $M = 14$, $D = 16$, 4 BSRAMs are required for compilation in GW5AT FPGAs.

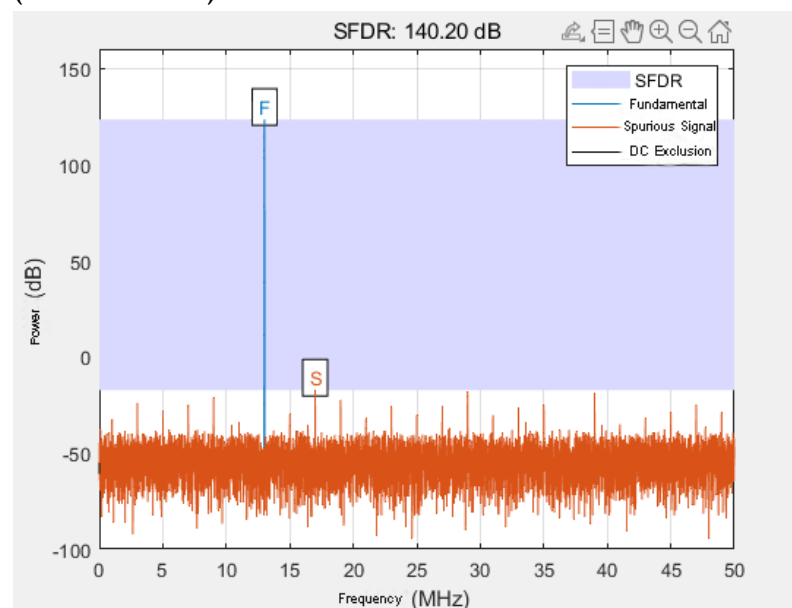
From the two figures above, it can be seen that Phase Dithered DDS achieves or exceeds the SFDR performance level of Phase Truncation DDS, while requiring only about 1/4 of the memory resources.

4.1.3 Taylor Series Corrected DDS

Phase Dithered DDS saves memory resources compared to Phase Truncation DDS, but the depth of memory will still be large if higher performance for SFDR are required. Due to the abundant multiplier resources available in FPGA devices, we can adopt a method to use discarded fractional bits for correcting the look-up table output values, achieving a very high SFDR. This introduces the Taylor series correction algorithm, known as Taylor Series Corrected DDS.

When $N = 27$, $M = 22$ (SFDR = 132dB) is required, the simulation analysis of Taylor Series Corrected DDS is shown in the following figure.

Figure 4-6 Taylor Series Corrected DDS Simulation Analysis when $N = 27$, $M=22$ (SFDR = 132dB)



In the GW5AT FPGA, only 1 BSRAM and 3 DSP resources are required for compilation, significantly optimizing storage resources.

4.2 DDS Type Selection

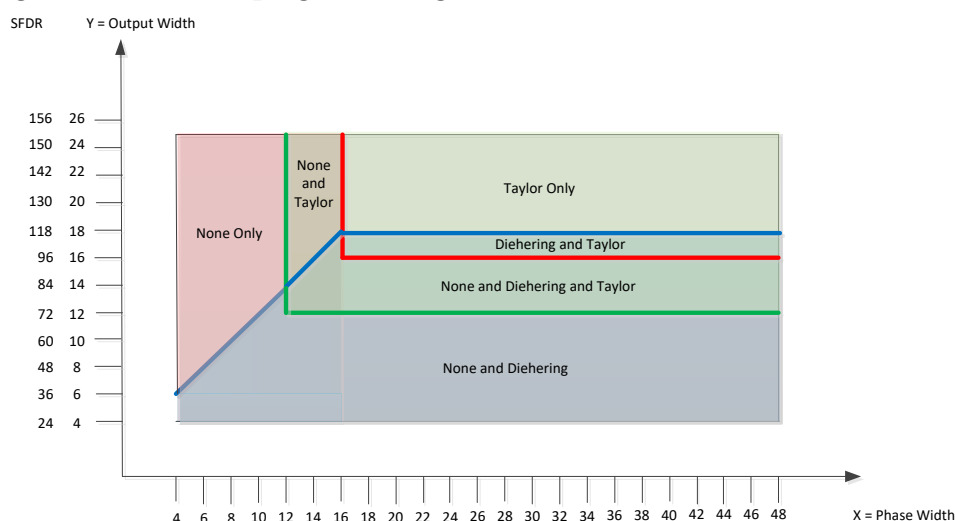
The selection among the three DDS types mentioned above depends on the performance requirements, resource usage, and other factors.

- When the SFDR requirement is low, it occupies very little memory resources, and Phase Truncation DDS can be used to fulfill the requirement.

- When the SFDR requirement is medium, Phase Dithered DDS can be considered if it does not consume too much memory resources; and it does not use DSP resources.
- When SFDR requirements are high, then Taylor Series Corrected DDS must be used, effectively reducing memory resource consumption by using DSP resources.

The following diagram shows the applicable range of SFDR and phase width for these three options. The overlapping areas indicate that multiple options are available.

Figure 4-7 Noise Shaping Area Diagram

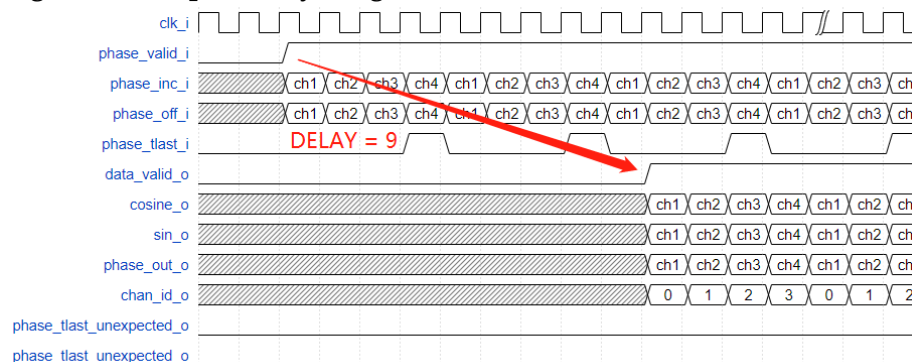


4.3 Multi-channel Design

When configured as multiple channels, the DDS or phase generator generates output for each channel in a time-multiplexed manner. Therefore, the output for a specific channel occurs every N cycles, where N is the number of channels selected when customizing the core, with the output for channel 0 first.

4.4 Latency

The core latency can be specified through the user interface, which can be used to adjust timing or optimize timing performance. For the PHASE interface, this latency is explicitly indicated; for streaming input, the latency specifies the number of cycles between the input and the output.

Figure 4-8 Output Delay Diagram

For the CONFIG interface, this latency is solely used to enhance timing performance and is not intended to establish a correlation between the input and output.

4.5 Parameter Conversion

In Parameter Selection option, System Parameters and Hardware Parameters can be converted interchangeably.

If the clock frequency for each channel is F_c (Hz),

In System Parameters option, setting $SFDR = A$ (dB), $FreqResolution = B$ (Hz), converts to Hardware Parameters as follows:

$$PhaseWidth = \text{Ceil}(\log_2(F_c / B))$$

$$OutputWidth = \text{Ceil}(A / 6)$$

Similarly, in Hardware Parameters option, setting $PhaseWidth = A$ (bit), $OutputWidth = B$ (bit), converts to System Parameters as follows:

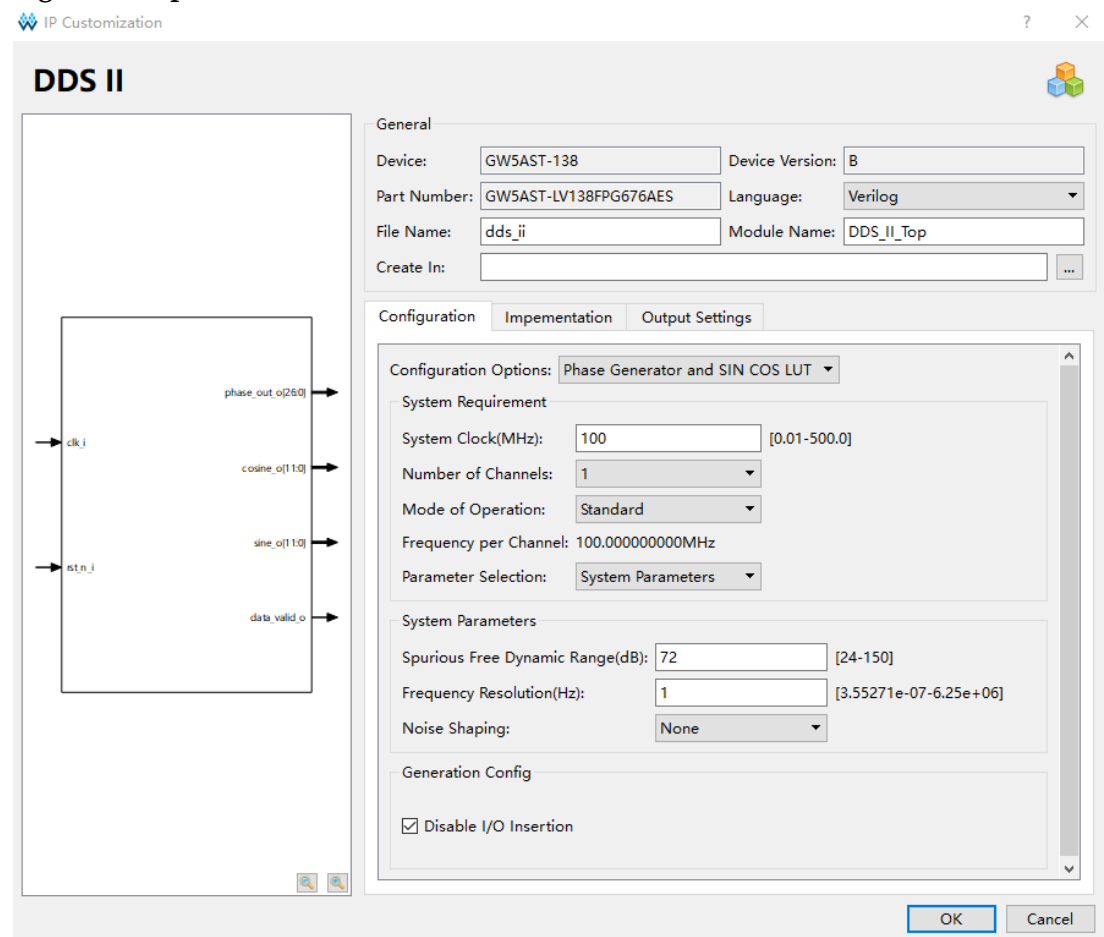
$$SFDR = B \times 6$$

$$FreqResolution = F_c / 2^A$$

5 Interface Configuration

You can click "Tools > IP Core Generator" on the menu bar in Gowin Software to call and configure DDS II IP.

Figure 5-1 Open DDS II IP



Configuration Tab

- Configuration Options: Includes "Phase Generator and SIN COS LUT", "Phase Generator Only", and "SIN COS LUT Only".
- System Clock (MHz): Input clock.

- Number of Channels: Indicates how many channels are included in the core, with a range of 1-16.
- Frequency per Channel: Displays the frequency per channel, calculated as System Clock (MHz) / Number of Channels.
- Parameter Selection: Includes System Parameters and Hardware Parameters. System Parameters can be set according to performance requirements, and Hardware Parameters can be set based on actual hardware specifications.

When System Parameters is selected:

- Spurious Free Dynamic Range (dB): Ranges from 24dB to 150dB, and this parameter is used to calculate the output width.
- Frequency Resolution (Hz): The range is [Frequency per Channel / 2^{48} , Frequency per Channel / 2^4], and this parameter is used to calculate the width of the accumulator.
- Noise Shaping: Includes None, Phase Dithering, Taylor Series Corrected.

When Hardware Parameters is selected:

- Noise Shaping: Includes None, Phase Dithering, Taylor Series Corrected.
- Phase Width: Ranges from 4 to 48.
- Output Width: Ranges from 4 to 25.

Implementation Tab

Figure 5-2 Implementation Tab

The screenshot shows the 'Implementation' tab of a configuration window. At the top, there are three tabs: 'Configuration', 'Implementation' (which is active), and 'Output Settings'. The main content area is divided into three sections:

- Phase Increment Programmability:** Contains three radio buttons: 'Fixed' (selected), 'Programmable', and 'Streaming'. Below them is a checkbox labeled 'resync' which is unchecked.
- Phase Offset Programmability:** Contains four radio buttons: 'None' (selected), 'Fixed', 'Programmable', and 'Streaming'.
- Output:** Contains three radio buttons: 'Sine', 'Cosine', and 'Sine and Cosine' (selected). Below these are two checkboxes: 'has Phase Out' (checked) and 'Channel ID out' (unchecked). At the bottom of this section is a 'Latency:' label followed by a dropdown menu currently showing the value '7'.

- Phase Increment Programmability: Used to select the method for setting the PINC value.
 - Fixed: The PINC is fixed when generated and cannot be changed during operation. "Fixed" requires the least resources.
 - Programmable: The PINC value can be changed during operation using the CONFIG channel. This option is recommended when the DDS frequency needs to change between different operating modes.
 - Streaming: The PINC value is taken directly from the input PHASE channel. This option is recommended when the PINC value needs to be changed frequently or when frequency modulation is required.
- Resync: When it is selected, the PHASE channel has a Resync port. When set to 1, the phase accumulator of the channel corresponding to this bit is reset. The accumulated phase value for that cycle is the PINC value plus the POFF value when RESYNC is set to 1.
- Phase Offset Programmability: Used to select the method for setting the POFF value.
 - None: No phase offset generation, and no hardware required for the generation, saving FPGA resources.
 - Fixed: POFF is fixed when generated and cannot be changed during operation.
 - Programmable: POFF value can be changed using the CONFIG channel. This option is recommended when the DDS phase changes between different operating modes.
 - Streaming: The POFF value can be changed using the input CONFIG channel. This option is recommended when the POFF value needs to be frequently changed, or for applications requiring phase modulation.
- Output: Can be Sine, Cosine, or both.
 - Has Phase Out: Whether to output of the current phase value or not.
 - Chan ID Out: When configured as multiple channels, the current channel ID indication can be output.
- Latency: Used to set the latency value. Reducing the latency value will decrease the number of pipeline stages and typically save resources. Increasing the latency value will increase the number of pipeline stages, which may optimize timing. The latency cycles are generated by the followings:
 - Streaming phase increment
 - Block ROM in the SIN/COS LUT
 - Latency processing of the Taylor series correction

Output Setting Tab

When the phase increment or phase offset is fixed or programmable, the following options will appear for inputting parameters. If it is set to programmable, the initial values of the registers are specified through the parameters.

When Parameter Selection is set to System Parameters, the display is as shown below.

Figure 5-3 System Parameters Selected

ConfigurationImpementationOutput Settings

Channel	Output Frequency(MHz)		Phase Offset Angle(*2 pi Radians)
1	1	—	0
2	0	—	0
3	0	—	0
4	0	—	0
5	0	—	0
6	0	—	0
7	0	—	0
8	0	—	0
9	0	—	0
10	0	—	0
11	0	—	0
12	0	—	0
13	0	—	0
14	0	—	0
15	0	—	0
16	0	—	0

- Output Frequency: This option appears when "Parameter Selection" is set to "System Parameters" and "Phase Offset Programmability" is set to "Fixed" or "Programmable". For each channel, independent frequencies (MHz) can be entered in the table. The allowable range is from 0 to Fs, and Fs is the frequency per channel. Values from Fs/2 to Fs map to -Fs/2 to 0 respectively, which can be used to input negative frequencies.
- Phase Offset Angle: This option appears when "Parameter Selection" is set to "System Parameters" and "Phase Offset Programmability" is set to "Fixed" or "Programmable". The table allows the phase offset of each channel to be specified as a fraction of a period. The valid range for the standard mode is from 0 to 1.0. For example, an input of 0.5 represents 180° (i.e., π radians).

When Parameter Selection is set to Hardware Parameters, the display is as shown below.

Figure 5-4 Hardware Parameters Selected

Configuration		Implementation		Output Settings	
Channel	Phase Increment Value(Hex)			Phase Offset Value(Hex)	
1	147AE1	—		0	
2	0	—		0	
3	0	—		0	
4	0	—		0	
5	0	—		0	
6	0	—		0	
7	0	—		0	
8	0	—		0	
9	0	—		0	
10	0	—		0	
11	0	—		0	
12	0	—		0	
13	0	—		0	
14	0	—		0	
15	0	—		0	
16	0	—		0	

- **Phase Increment Value:** This option appears when "Parameter Selection" is set to "Hardware Parameters" and "Phase Offset Programmability" is set to "Fixed" or "Programmable". Values must be entered in hexadecimal form. The range is from 0 to $2^{\text{PhaseWidth}}-1$.
- **Phase Offset Value:** This option appears when "Parameter Selection" is set to "Hardware Parameters" and "Phase Offset Programmability" is set to "Fixed" or "Programmable". Values must be entered in hexadecimal form. The range is from 0 to $2^{\text{PhaseWidth}}-1$.

6 Reference Design

For detailed information, see DDS II IP [reference design](#) at Gowinsemi website.

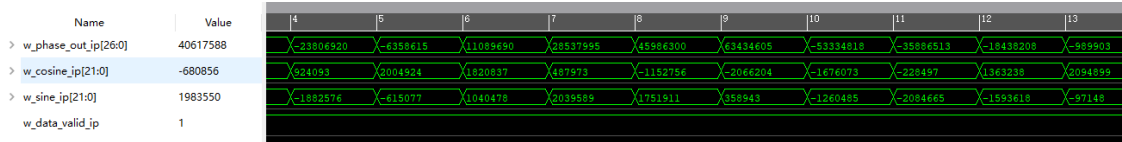
6.1 Reference Design

This chapter focuses on the usage and structure of the reference design instance of DDS II IP. The DDS II design example has only one module. Please refer to the DDS IP reference design for details.

6.2 Operating Flow

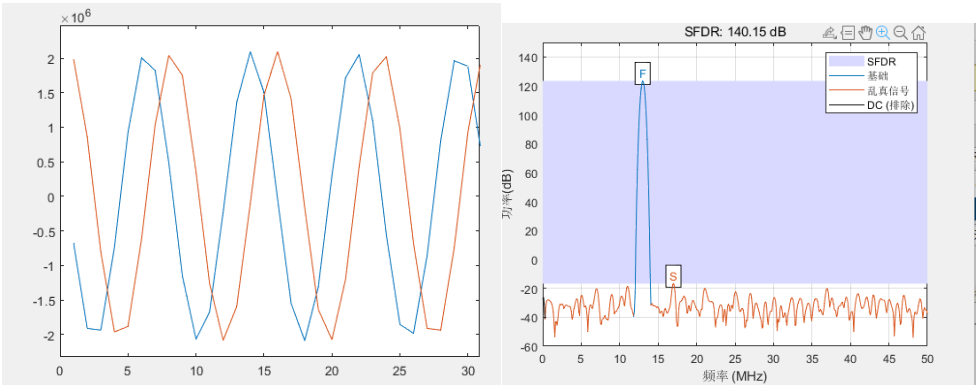
- 1. Capture DDS data through GAO and export it as a scv file.

Figure 6-1 Capture DDS Data



- 2. Extract the values from the scv file and use software like MATLAB for waveform reading and analysis.

Figure 6-2 Waveform Reading and Analysis



7 File Delivery

The delivery files for Gowin DDS II IP includes the documents, the design source code, and the reference design.

7.1 Documentation

The folder mainly contains the user guide in PDF version.

Table 7-1 Document List

Name	Description
IPUG1019, Gowin DDS II IP User Guide	Gowin DDS II IP User Guide, namely this one

7.2 Design Source Code (Encryption)

The Encryption Code Folder contains the RTL encryption code of Gowin DDS II IP, used for the GUI, and it is used with Gowin Software to generate the IP core as needed.

Table 7-2 Gowin DDS II IP Design Source Code List

Name	Description
dds_ii_core.v	The top-level file of the IP core, which provides users with interface information, encrypted.

7.3 Reference Design

Gowin DDS II RefDesign folder contains the netlist file for Gowin DDS II IP, user reference design, constraints file, top-level file, and project file, etc.

Table 7-3 Gowin DDS II IP RefDesign Folder Content List

Name	Description
top.v	The top module of reference design
top.cst	Project physical constraints file
top.sdc	Project timing constraints file
top.gao	Project data capture file
dds_ii.v	DDS II module, encrypted

