



DK_START_GW5AST-
LV138FPG676A_V1.0

User Guide

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1 About This Guide

1.1 Purpose

The DK_START_GW5AST-LV138FPG676A_V1.0 development board (hereinafter referred to as “the development board”) user guide consists of following three parts:

- A brief introduction to the features of the development board
- An introduction to the development board system architecture and hardware resources
- An introduction to the hardware circuits, functions and pinout

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- [DS981, Arora V 138K & 75K FPGA Products Data Sheet](#)
- [UG986, GW5AST-138 Pinout](#)
- [UG1102, GW5AST series of FPGA Products Package & Pinout User Guide](#)
- [UG704, Arora V 138K FPGA Product Programming and Configuration Guide](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
BSRAM	Block Static Random Access Memory
DDR	Double Data Rate
DSP	Digital Signal Processing
FLASH	Flash Memory
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
LDO	Low Dropout Regulator
LUT4	Four-input Look-up Table
LVDS	Low-Voltage Differential Signaling
SSRAM	Shadow Static Random Access Memory

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

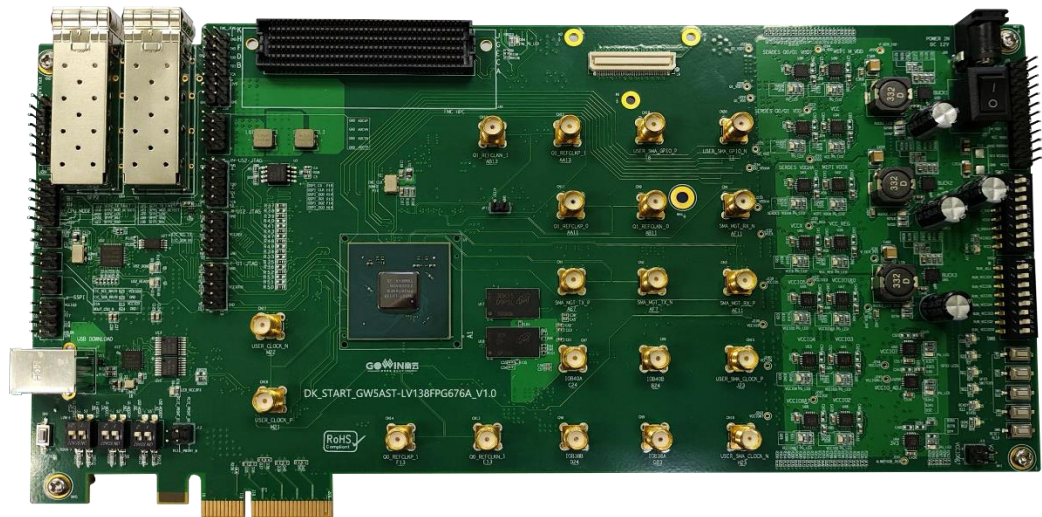
Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Development Board Introduction

2.1 Overview

Figure 2-1 DK_START_GW5AST-LV138FPG676A_V1.0 Development Board



DK_START_GW5AST-LV138FPG676A_V1.0 development board applies to high-speed data storage based on DDR3, high-speed communication test based on MIPI, LVDS, SERDES, and FMC, GW5AST-138 series of FPGA function evaluation, hardware verification, and software learning and debugging, etc.

The development board uses the GW5SAT-LV138FPG676A FPGA device, which is one of the Gowin GW5SAT series of FPGA products. Gowin GW5AST series of FPGA products include abundant internal resources, high-performance DSP with a new architecture that supports AI operations, high-speed LVDS interface and abundant BSRAM resources. At the same time, it integrates self-developed DDR3, 12.5Gbps SerDes supporting multiple protocols (supported by GW5AST-138), and provides a variety of packages. It is suitable for applications such as low power, high performance and compatibility design. The 22nm process makes Arora V

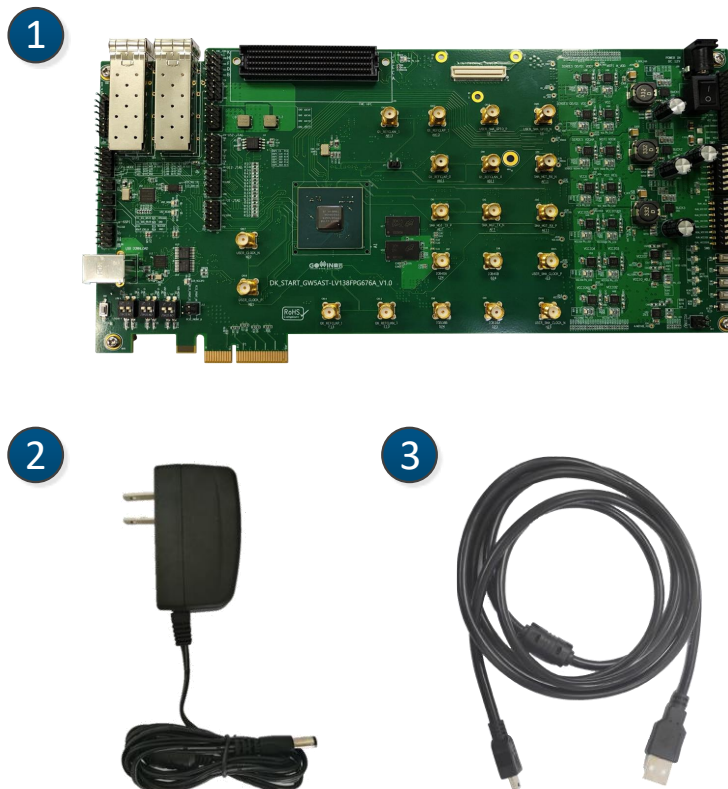
FPGA products suitable for high-speed, low-cost applications.

2.2 A Development Board Kit

The development board kit includes the following items:

1. DK_START_GW5AST-LV138FPG676A_V1.0 development board
2. 12V power (Input: 100-240V~50/60Hz 0.6A, output: DC 12V 2A)
3. USB 2.0 download cable

Figure 2-2 A Development Board Kit



- ① DK_START_GW5AST-LV138FPG676A_V1.0 development board
- ② 12V power supply
- ③ USB 2.0 download cable

2.3 PCB Components

Figure 2-3 PCB Components

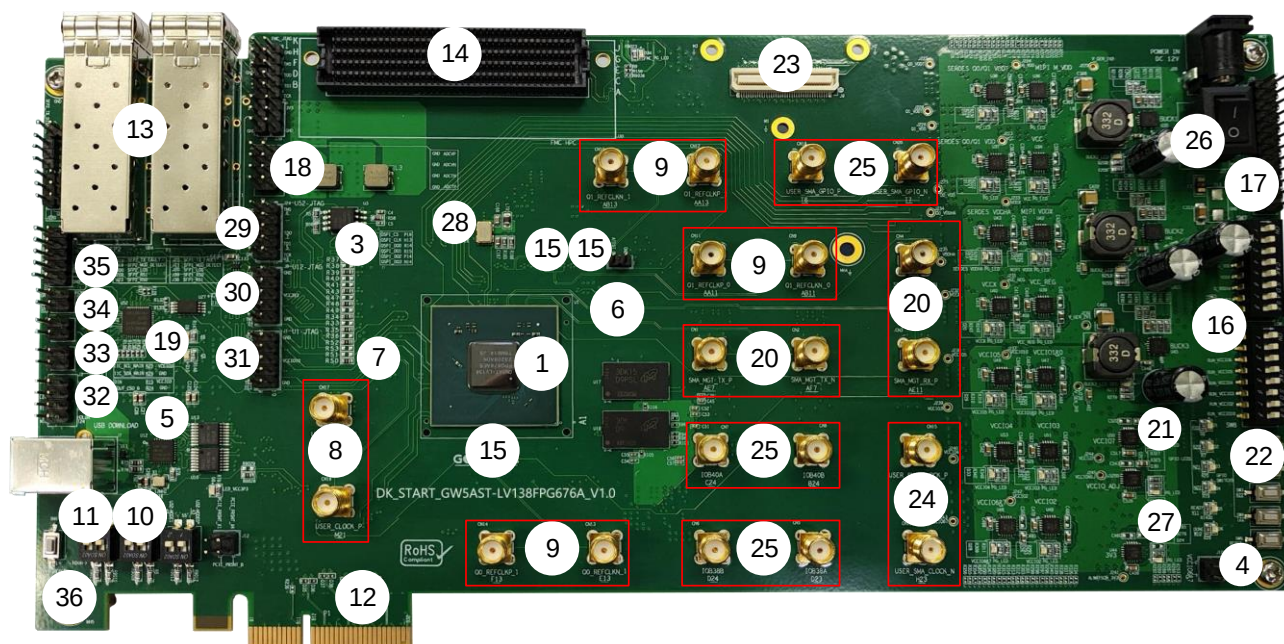


Table 2-1 PCB Components

No.	Designator	Device	Description	Schematic Page
1	U1	Arora V FPGA	GW5AST-LV138FPG676A	1
2	U16, U17	DDR3	Micron MT41J128M16JT-125:K	6
3	U3	Quad SPI flash memory	Gigadevice GD25Q128ESIG	3
4	SW5	FPGA Reconfig Switch	HRO K2-1107ST-A4SW-06	3
5	U12	USB-JTAG module	GOWIN GWU2X 2136A1A1N PAX486.00 (version A)	4
6	U33	System clock source (back of the board)	SiTime SIT9102AI-243N33E200.00000	14
7	Y3	Programmable user clock source (back of the board)	SiTime SIT3521AC-2C1331GG156.250000T	14
8	CN16, CN17	SMA user clock input	Rosenberger 32K 10K-400L5	14
9	CN9,CN11,CN13, CN14,CN10,CN12	SMA GTP reference clock input	Rosenberger 32K 10K-400L5	14
10	S2, S3	FPGA (U1) Configuration mode switch	C&K SDA02H1SBD	3
11	S5	FPGA (U52) Configuration mode switch	C&K SDA02H1SBD	10
12	P1	PCI Express edge connector	4-lane card edge connector	7

No.	Designator	Device	Description	Schematic Page
13	P3, U24	SFP/SFP+ connector	Molex 74441-0010	8.9
14	J30	FMC HPC connector	Samtec ASP_134486_01	11,12, 13
15	U30, U31, U32	GTP transceiver clock generator	SiTime SIT9102AI-243N33E100.00000	14
16	SW7, SW8	LDO EN pin switch	C&K SDA08H1BD	17
17	J28	LDO EN pin	HCTL PZ254-2-12-Z-8.5	17
18	J2	XADC	HCTL PZ254-2-02-Z-8.5	3
19	U52	I2C bus switch	GOWIN GW1NZ-LV1QN48C6/I5	10
20	CN1,CN2,CN3,CN4	MGT Transmit, receive SMA	-	8
21	D1,D2,D3,D4	User GPIO LEDs	Lite-On LTST-C190GKT	3
22	SW1,SW2,SW3,SW4	User GPIO switch	HRO K2-1107ST-A4SW-06	3
23	J9	MIPI	Panasonic AXK580137YG	5
24	CN15, CN18	User Clock SMA	-	14
25	CN19,CN20,CN5,CN6,CN7,CN8	SMA user GPIO	Rosenberger 32K 10K-400L5	13.14
26	J27	Power on/off switch	HCTL RS601HL-1010011BB	17
27	D5, D6	READY/DONE LED	Lite-On LTST-C190GKT	3
28	Y2	FPGA Clock 50Mhz	JGHC O5350000153350	14
29	J24	FPGA (U52) JTAG	HCTL PZ254-2-05-Z-8.5	10
30	J8	FPGA(U12) JTAG	HCTL PZ254-2-05-Z-8.5	4
31	J1	FPGA (U1) JTAG	HCTL PZ254-2-05-Z-8.5	3
32	J3	FPGA(U1) SSPI	HCTL PZ254-2-04-Z-8.5	3
33	J60	FPGA(U1) SERIAL	HCTL PZ254-2-02-Z-8.5	3
34	J5	FPGA(U1) IIC	HCTL PZ254-2-02-Z-8.5	3
35	J4, J222	FPGA(U1) CPU MODE	HCTL PZ254-2-05-Z-8.5 HCTL PZ254-2-02-Z-8.5	3
36	SW6	CPU RESET SWITCH	HRO K2-1107ST-A4SW-06	14

2.4 PCB Silkscreen

You can find the devices on the development board faster through the PCB silkscreen, please see [Chapter 4](#) Appendix for the PCB silkscreen.

2.5 Features

The key features are as follows:

1. FPGA Device
 - The development board uses the GW5AST-LV138FPG676A FPGA device, which is the fifth generation products of Gowin Arora family.
 - Max. user I/O: 312
2. Download and Boot
 - Integrate download module on the board, download through USB 2.0 cable
 - External Flash boot
 - The DONE light is on after loading
3. Power
 - External DC 12V 2A Power
 - The POWER light is on after power on
 - The board generates 0.9V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V power supplies and the power supplies required for FMC interfaces, MIPI interfaces, and SFP interfaces.
4. Clock system
50MHz clock, 100MHz clock, 200MHz clock, programmable clock
5. Memory Device
 - 4Gbit DDR3 SDRAM
 - 128Mbit Quad SPI FLASH Memory
6. SFP/SFP+ interface
 - 2 compact pluggable SFP+ connectors that receives SFP or SFP+ modules
 - External interface circuit to accommodate various optical modules
7. MIPI Interface
 - The interface includes 10 pairs of differential signals including 2 pairs for clock and 8 pairs for data, 34 single-ended signals, power supply, and GND.
 - Use connector with 80 contacts and 0.5mm pitch
8. FMC Interface
 - 58 pairs of differential signals: 34 pairs of LA (LA00-LA33); 24 pairs of HA (HA00-HA23)

- 4 pairs of GTP transceivers
- 2 pairs of GTP transceiver reference clocks
- 2 pairs of external input differential reference clocks
- 159 GNDs and 15 power connections
- Use 400pin HPC FMC connector with 1.27mm pitch
- Differential signals of 3 lanes are channeled to the 20pin double rows with 2.00mm pitch.

9. XADC Module

- The interface uses 2*4pin pin.
- The XADC differential input is designed with an anti-aliasing filter.

10. PCIe x4 Interface

- The overall dimension of the PCIe card conforms to the standard PCIe card electromechanical specification and can be used directly on a normal PCIe x4 slot.
- The transceiver signals of PCIe interface are directly connected to the GTP transceivers of FPGA.

11. Debug module

- 4 keys
- 4 LEDs

3 Development Board Circuit

3.1 FPGA Module

Overview

For the resources of GW5AST series of FPGA Products, refer to [*DS981, Arora V 138K & 75K FPGA Products Data Sheet*](#).

I/O BANK Introduction

For the I/O BANK, package, and pinout information, see [*UG1102, GW5AST series of FPGA Products Package & Pinout User Guide*](#) for more details.

3.2 Download Module

3.2.1 Introduction

The development board provides USB download interface, which is realized by GWU2X 2136A1A1N PAX486.00 chip (Version A), which is one of the ASSP chip of Gowin GoBridge Family. You can set the MODE value to download the programs to the on-chip SRAM or external Flash. When downloaded to SRAM, the bitstream file will be lost if the device is power down. When downloaded to Flash, the bitstream file will not be lost if power down.

The MODE value configuration is as follows:

1. In any mode, you can download the bitstream file to the on-chip SRAM and run it immediately.
2. Set MODE as "001" to download the bitstream file to the external Flash.

The connection diagram of download and configuration is as show in Figure 3-1.

Figure 3-1 Connection Diagram of FPGA Download and Configuration

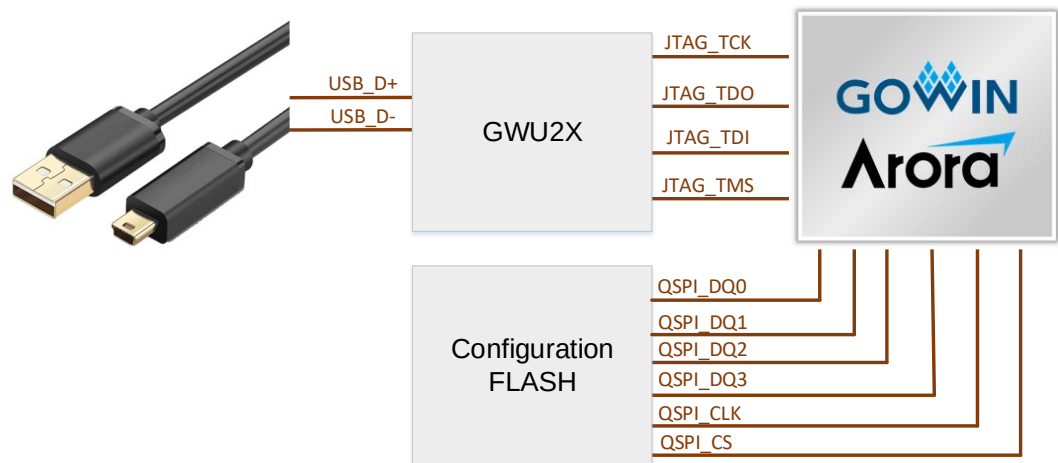


Figure 3-2 USB-to-JTAG Circuit Schematic Design

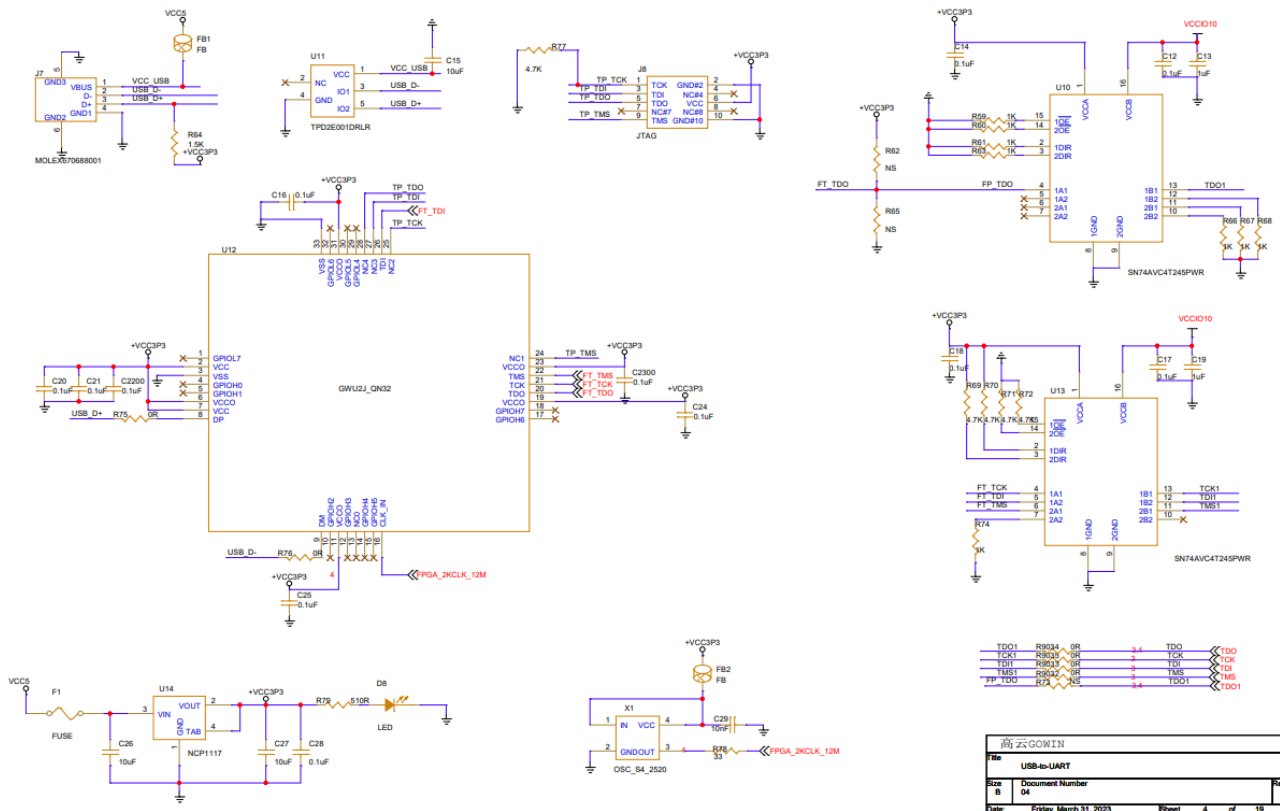
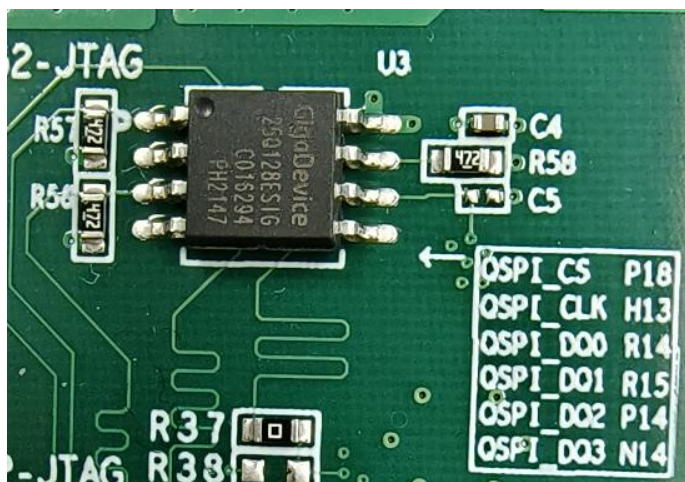


Figure 3-3 USB Download Circuit on Development Board



Figure 3-4 FLASH Circuit on Development Board



3.2.2 Pinout

Table 3-1 FPGA Download and Pinout

Signal Name	Schematic Page	FPGA(U1) Pin No.	BANK	I/O Level	Description
TCK	3	H12	10	3.3V	JTAG Signal
TDO	3	J10	10	3.3V	JTAG Signal
TDI	3	H10	10	3.3V	JTAG Signal
TMS	3	H11	10	3.3V	JTAG Signal
QSPI_DQ0	3	R14	3	3.3V	Configuration FLASH Signal
QSPI_DQ1	3	R15	3	3.3V	Configuration FLASH Signal
QSPI_DQ2	3	P14	3	3.3V	Configuration FLASH Signal
QSPI_DQ3	3	N14	3	3.3V	Configuration FLASH Signal
QSPI_CS	3	P18	3	3.3V	Configuration FLASH Signal
QSPI_CLK	3	H13	10	3.3V	Configuration FLASH Signal

3.3 Power Supply

3.3.1 Introduction

The development board is powered via a power adapter. The input parameter is 100-240V~50/60MHz 0.6A, and the output parameter is DC +12V 2A.

The input 12V power supply generates 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, 0.9V power supplies, 0.75V power supply required for DDR3, 3.3V power supply for SFP/SFP+ interface; and 12V, 3.3V power supplies for FMC interface through the power chip on the development board.

The board adopts three TPS54620 DC-DC power chips to generate 1.2V, 2.1V, and 3.6V power. The maximum output current is 6A.

Then the three DC-DC power chips output power supply to seventeen TPL930 LDO power chips, generating 0.9V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V power supplies. The maximum output current is 3A.

The power supply output from the TPL930 LDO power chips is used as the input to the DDR3 power supply chip, TPS51200, which outputs 0.75V to power the DDR3 chip.

SW7 & SW8 control the enable pins of the power chip. SW7 & SW8 should be set to the outermost position to enable the power chip.

Table 3-2 Arora V FPGA Voltage

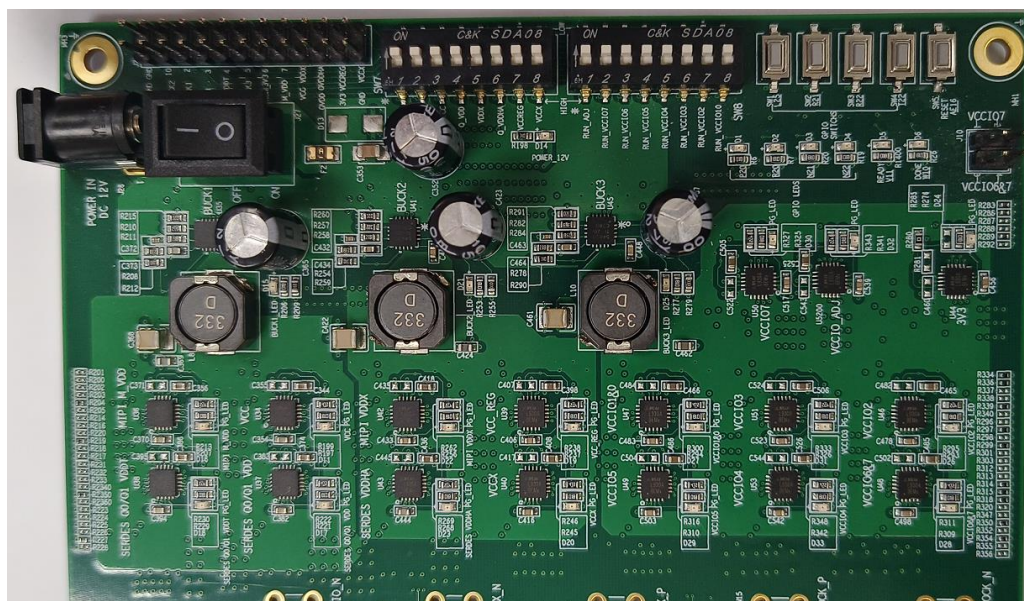
Group	Name	Description
FPGA	VCC	Core voltage
	VCCX	Auxiliary voltage
	VCCIO	I/O Bank voltage
	VCC_LDO	Regulator voltage
SERDES	VDD_Qn	SerDes analog core voltage
	VDDHA_Qn	SerDes analog high voltage
	VDDT_Qn	SerDes transmitter voltage
MIPI	VDD_M	MIPI analog core voltage
	VDDX	MIPI analog high voltage

Table 3-3 Recommended Operating Conditions of Arora V FPGA Voltage

Group	Name	Min.	Recommended	Max.
FPGA	VCC	0.87V	0.90V	1.00V
	VCCX	1.71V	1.80V	1.89V
	VCCIO	1.00V	1.80V	3.465V

Group	Name	Min.	Recommended	Max.
	VCC_LDO	1.14V	1.20V	1.26V
SERDES	VDD_Qn	0.87V	0.90V	1.00V
	VDDHA_Qn	1.71V	1.80V	1.89V
	VDDT_Qn	0.87V	0.90V	1.00V
MIPI	VDD_M	0.87V	0.90V	1.00V
	VDDX	1.71V	1.80V	1.89V

Figure 3-5 Power Supply Circuit on Development Board



3.4 Reset

3.4.1 Introduction

The reset circuit of the development board is controlled by keys. When switch SW5 is pressed, the FPGA (U1) Reconfig_n pin is connected to GND and the FPGA is reconfigured.

Figure 3-6 Reset Connection Diagram

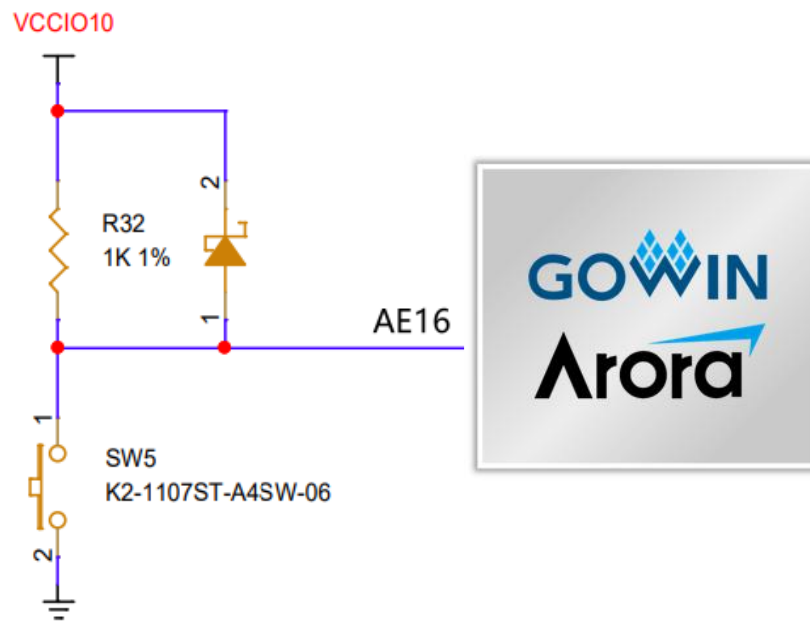
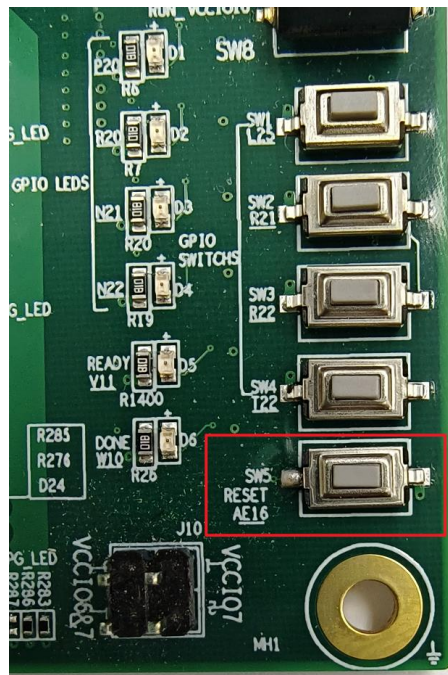


Figure 3-7 Reset Circuit on Development Board



3.4.2 Pinout

Table 3-4 Reset Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
Reconfig_n	AE16	10	3.3V	Reset Signal, active Low

3.5 Clock

3.5.1 Introduction

There are several clock sources available for the FPGA, as shown in Table 3-5.

Table 3-5 Clock Pinout

Signal Name	FPGA Pin No.	I/O Level	Clock Generator	Description
USER_CLOCK_P	M21	3.3V	Y3	SIT3521 3.3V I2C programmable differential clock
USER_CLOCK_N	M22	3.3V	Y3	SIT3521 3.3V I2C programmable differential clock
USER_SMA_CLOCK_P	J23	[1]	CN15	SMA input FPGA differential clock
USER_SMA_CLOCK_N	H23	[1]	CN18	SMA input FPGA differential clock
SYS_CLK_P	R3	1.5V	U33	SIT9102 3.3V 200Mhz differential clock
SYS_CLK_N	P3	1.5V	U33	SIT9102 3.3V 200Mhz differential clock
EMCCLK	P16	3.3V	Y2	The O5350000153350 generates a 3.3V single-ended 50Mhz clock
Q0_REFCLKP_0	F11	-	PCIe Clock Pin	PCIe clock pin inputs FPGA clock signal
Q0_REFCLKN_0	E11	-	PCIe Clock Pin	PCIe clock pin inputs FPGA clock signal
Q0_REFCLKP_1	F13	-	U32	SIT9102 3.3V 100Mhz differential clock
Q0_REFCLKN_1	E13	-	U32	SIT9102 3.3V 100Mhz differential clock
Q1_REFCLKP_0	AA11	-	U31	SIT9102 3.3V 100Mhz differential clock
Q1_REFCLKN_0	AB11	-	U31	SIT9102 3.3V 100Mhz differential clock
Q1_REFCLKP_1	AA13	-	U30	SIT9102 3.3V 100Mhz differential clock
Q1_REFCLKN_1	AB13	-	U30	SIT9102 3.3V 100Mhz differential clock

Note!

^[1] This user clock is input to FPGA bank 4, which is powered by VCCIO4. VCCIO4 is typically 2.5V, but can be reprogrammed to 1.8V or 3.3V. The USER_SMA_CLOCK_P/N signal should not exceed the VCCIO4 voltage (1.8V, 2.5V or 3.3V).

Figure 3-8 Clock Connection Diagram

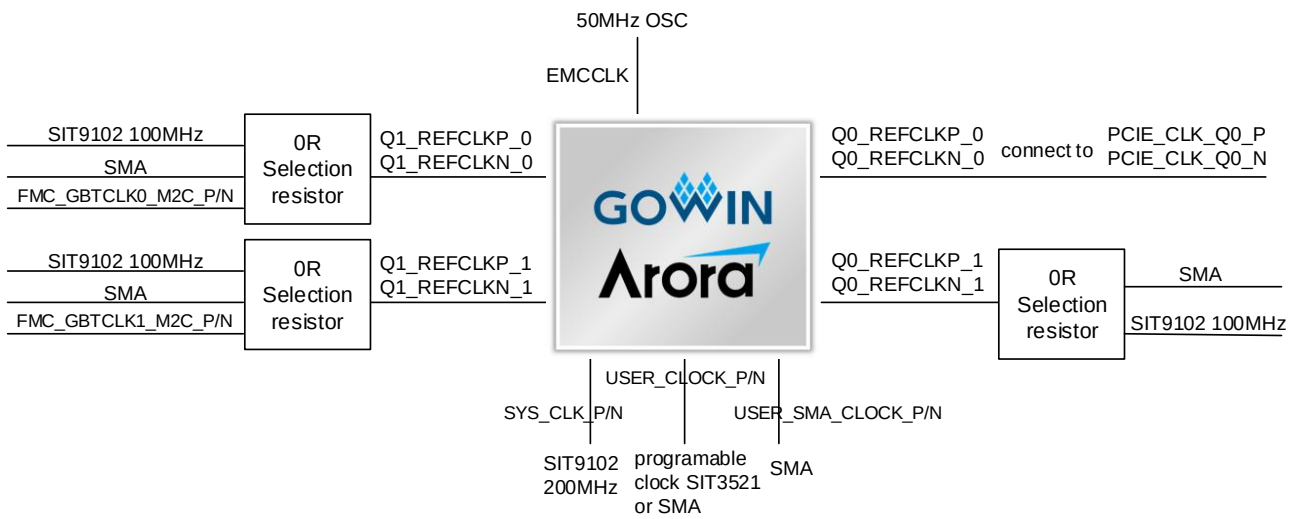
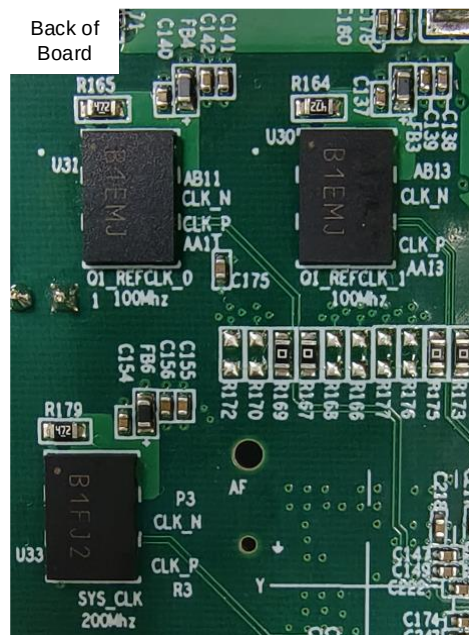
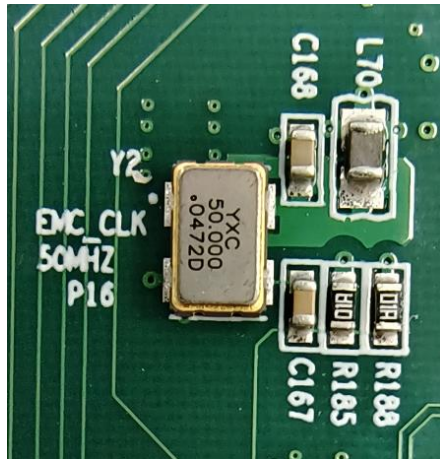


Figure 3-9 Clock Circuit on Development Board





3.6 DDR3

3.6.1 Introduction

The DK_START_GW5AST-LV138FPG676A_V1.0 development board includes two Micron MT41J128M16JT-125:K chips, which are 2Gbit (256MB) DDR3 chips (4Gbit in total). The bus width of DDR is 32 bits in total. The DDR3 storage system connects directly to the memory interfaces of the BANK 6 and BANK 7 on the FPGA. The specific configurations of DDR3 SDRAM are as shown in Table 3-6.

Table 3-6 DDR3 SDRAM Configuration

Designator	Model	Capacity	Manufacturer
U16, U17	MT41J128M16JT-125:K	128M x 16bit	Micron

DDR3 hardware design requires strict consideration of signal integrity. In the design of circuit and PCB, matching resistance/termination resistance, impedance control and equal length control of traces have been fully considered to ensure the high-speed and stability of DDR3.

The hardware connection diagram of DDR3 DRAM is as show in Figure 3-10.

Figure 3-10 Hardware Connection Diagram of DRAM

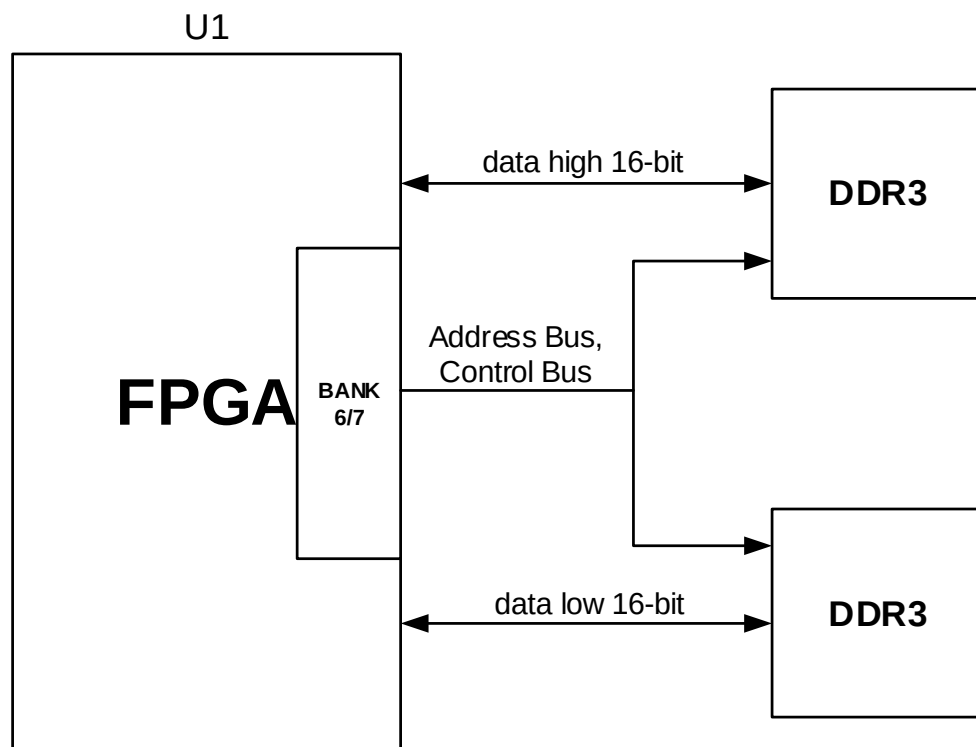


Figure 3-11 DDR3 SDRAM Circuit on Development Board



3.6.2 Pinout

Table 3-7 DDR3 Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
DDR3_A0	N1	7	1.5V	Address
DDR3_A1	R1	7	1.5V	Address
DDR3_A2	R2	7	1.5V	Address
DDR3_A3	N2	7	1.5V	Address
DDR3_A4	P1	7	1.5V	Address
DDR3_A5	T2	7	1.5V	Address
DDR3_A6	N4	7	1.5V	Address
DDR3_A7	U1	7	1.5V	Address
DDR3_A8	T4	7	1.5V	Address
DDR3_A9	T3	7	1.5V	Address
DDR3_A10	M1	7	1.5V	Address
DDR3_A11	P4	7	1.5V	Address
DDR3_A12	N3	7	1.5V	Address
DDR3_A13	U2	7	1.5V	Address
DDR3_BA0	M4	7	1.5V	Bank address
DDR3_BA1	L5	7	1.5V	Bank address
DDR3_BA2	K3	7	1.5V	Bank address
DDR3_CAS#	H1	7	1.5V	Column address strobe
DDR3_CKE	L3	7	1.5V	Clock Enable
DDR3_CLK0_N	L2	7	1.5V	Differential clock
DDR3_CLK0_P	M2	7	1.5V	Differential clock
DDR3_DQ0	G4	6	1.5V	Data
DDR3_DQ1	J6	6	1.5V	Data
DDR3_DQ2	L8	6	1.5V	Data
DDR3_DQ3	G5	6	1.5V	Data
DDR3_DQ4	K7	6	1.5V	Data
DDR3_DQ5	J5	6	1.5V	Data
DDR3_DQ6	K8	6	1.5V	Data
DDR3_DQ7	K6	6	1.5V	Data
DDR3_DQ8	E6	6	1.5V	Data
DDR3_DQ9	H8	6	1.5V	Data
DDR3_DQ10	H6	6	1.5V	Data

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
DDR3_DQ11	G8	6	1.5V	Data
DDR3_DQ12	D6	6	1.5V	Data
DDR3_DQ13	F8	6	1.5V	Data
DDR3_DQ14	G6	6	1.5V	Data
DDR3_DQ15	F7	6	1.5V	Data
DDR3_DQ0_1	C4	6	1.5V	Data
DDR3_DQ1_1	F3	6	1.5V	Data
DDR3_DQ2_1	B4	6	1.5V	Data
DDR3_DQ3_1	E5	6	1.5V	Data
DDR3_DQ4_1	D3	6	1.5V	Data
DDR3_DQ5_1	D5	6	1.5V	Data
DDR3_DQ6_1	A4	6	1.5V	Data
DDR3_DQ7_1	D4	6	1.5V	Data
DDR3_DQ8_1	E1	6	1.5V	Data
DDR3_DQ9_1	A2	6	1.5V	Data
DDR3_DQ10_1	G2	6	1.5V	Data
DDR3_DQ11_1	C2	6	1.5V	Data
DDR3_DQ12_1	F2	6	1.5V	Data
DDR3_DQ13_1	E2	6	1.5V	Data
DDR3_DQ14_1	G1	6	1.5V	Data
DDR3_DQ15_1	D1	6	1.5V	Data
DDR3_DM0	F4	6	1.5V	Data input mask
DDR3_DM1	H9	6	1.5V	Data input mask
DDR3_DM0_1	E3	6	1.5V	Data input mask
DDR3_DM1_1	A3	6	1.5V	Data input mask
DDR3_DQS0_P	J4	6	1.5V	Data Clock
DDR3_DQS0_N	H4	6	1.5V	Data Clock
DDR3_DQS1_P	H7	6	1.5V	Data Clock
DDR3_DQS1_N	G7	6	1.5V	Data Clock
DDR3_DQS0_P_1	B5	6	1.5V	Data Clock
DDR3_DQS0_N_1	A5	6	1.5V	Data Clock
DDR3_DQS1_P_1	C1	6	1.5V	Data Clock
DDR3_DQS1_N_1	B1	6	1.5V	Data Clock
DDR3_ODT	J1	7	1.5V	On-Die Termination Enable

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
DDR3_RAS#	H2	7	1.5V	Row address strobe
DDR3_RESET	N8	7	1.5V	Reset
DDR3_WE#	J3	7	1.5V	Write enable

3.7 QSPI Flash

3.7.1 Introduction

The DK_START_GW5AST-LV138FPG676A_V1.0 development board includes a FLASH memory chip. The chip model is GD25Q128 and the memory capacity of 128Mbit. Since FLASH has the feature of no loss of data when power down, while the data in our FPGA chip will be lost when power down, so FLASH can be used as the power-on configuration device. The power-on program can be hardened in FLASH, then FPGA chip reads the program stored in FLASH to run after power on, so that the program will not be lost when power down. The specific models and related parameters of SPI FLASH are as shown in Table 3-8.

Table 3-8 Specific Models and Related Parameters of SPI FLASH

Designator	Model	Capacity	Manufacturer
U3	GD25Q128ESIG	128M Bit	Gigadevice

The QSPI FLASH is connected to the dedicated pins of BANK10 and BANK3 on the FPGA chip, where the clock pin is connected to the CCLK of BANK10, other data and chip select signals are connected to the D00~D03 and MCSN pins of BANK3, respectively. Figure 3-12 is the hardware connection diagram of QSPI Flash.

Figure 3-12 Hardware Connection Diagram of QSPI Flash

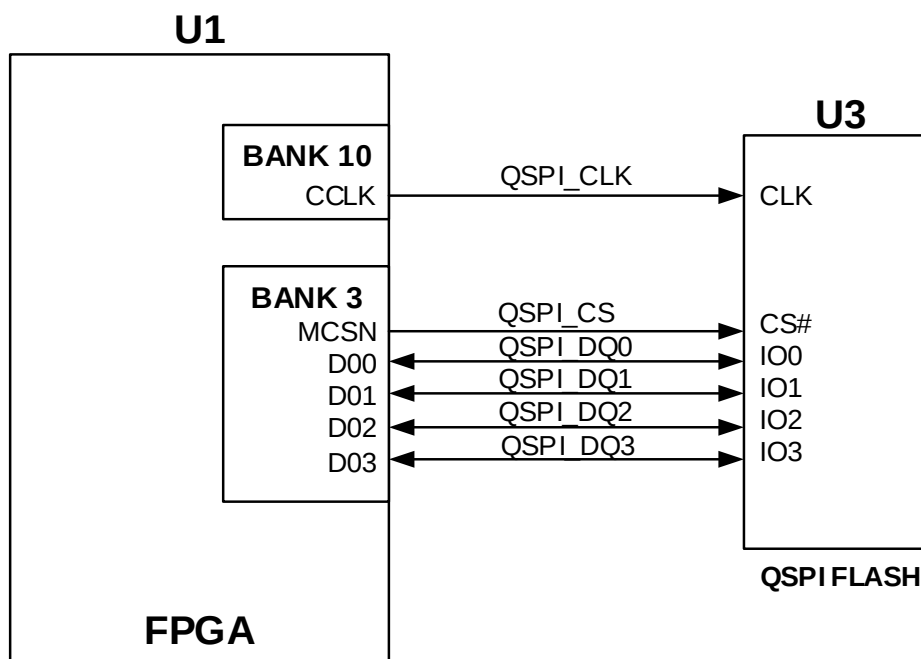
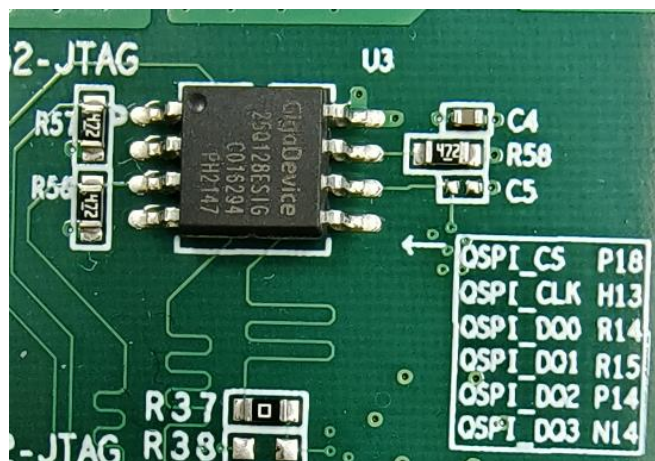


Figure 3-13 QSPI Flash Circuit on Development Board



3.7.2 Pinout

Table 3-9 FLASH Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level
QSPI_CLK	H13	10	3.3V
QSPI_CS	P18	3	3.3V
QSPI_DQ0	R14	3	3.3V
QSPI_DQ1	R15	3	3.3V
QSPI_DQ2	P14	3	3.3V
QSPI_DQ3	N14	3	3.3V

3.8 LED, Key

3.8.1 Introduction

There are 3 kinds of LEDs on the DK_START_GW5AST-LV138FPG676A_V1.0 development board, including power indicators, configuration LEDs, and user LEDs.

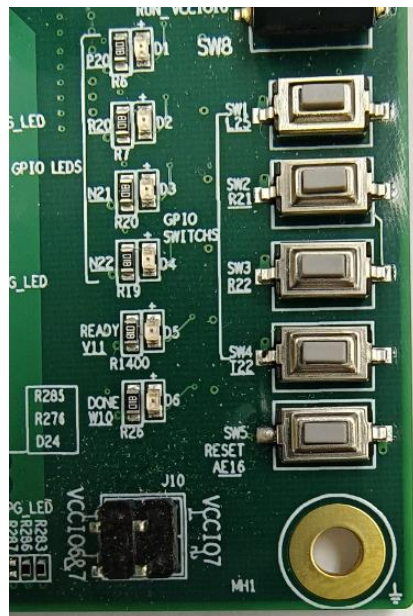
When 12V power supply, DC-DC power supply chip, LDO power supply chip are working properly, the power indicator will light up.

The configuration LED will light up after the FPGA is configured with programs.

The user LED is connected to the IO of BANK3 and can be switched on and off via the program. The user LED will be on when the IO voltage connected to the user LED is high. The user LED will be off when the IO voltage connected is low.

There are four user keys (SW1-SW4) on the development board. The four keys are connected to the normal IO of the FPGA. The IO input voltage of the FPGA is low when the key is pressed while high when the key is not pressed.

Figure 3-14 LED and Key Circuit on Development Board



3.8.2 Pinout

Table 3-10 LED Pinout

Signal Name	Designator	FPGA Pin No.	BANK	I/O Level	Description
LED1	D1	P20	3	3.3V	User LED
LED2	D2	R20	3	3.3V	User LED
LED3	D3	N21	3	3.3V	User LED
LED4	D4	N22	3	3.3V	User LED
Ready	D5	V11	10	3.3V	Configuration LED
Done	D6	W10	10	3.3V	Configuration LED
SW1	SW1	L25	3	3.3V	User Key
SW2	SW2	R21	3	3.3V	User Key
SW3	SW3	R22	3	3.3V	User Key
SW4	SW4	T22	3	3.3V	User Key
CPU_RESET	SW6	U4	7	1.5V	User Key

3.9 JTAG Interface

3.9.1 Introduction

The DK_START_GW5AST-LV138FPG676A_V1.0 development board has a JTAG test socket reserved to download and debug JTAG separately for FPGA.

J1 is used to download and debug the JTAG of FPGA U1; J8 is used to download and debug the JTAG of FPGA U12; J24 is used to download and debug the JTAG of FPGA U52.

Figure 3-15 Schematic of JTAG interface J1

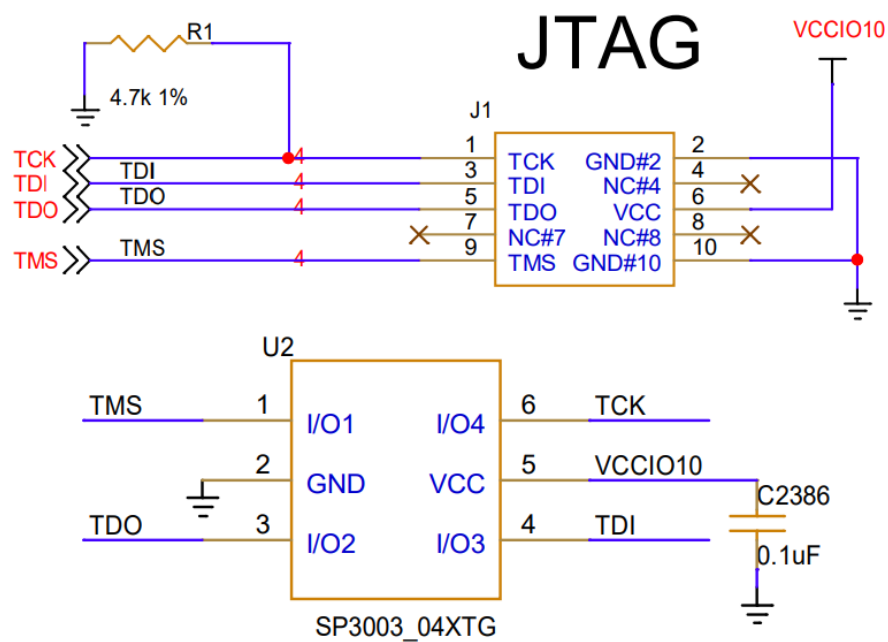
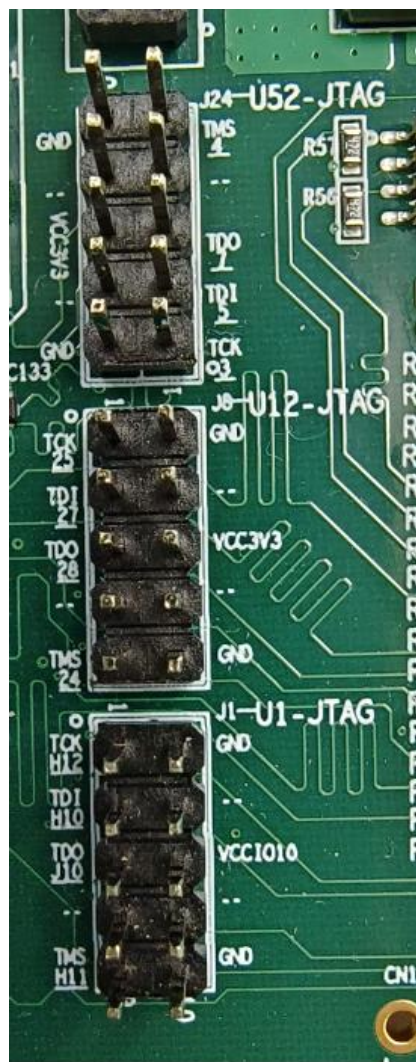


Figure 3-16 JTAG Circuit on Development Board



3.9.2 Pinout

Table 3-11 JTAG Pinout of FPGA U1

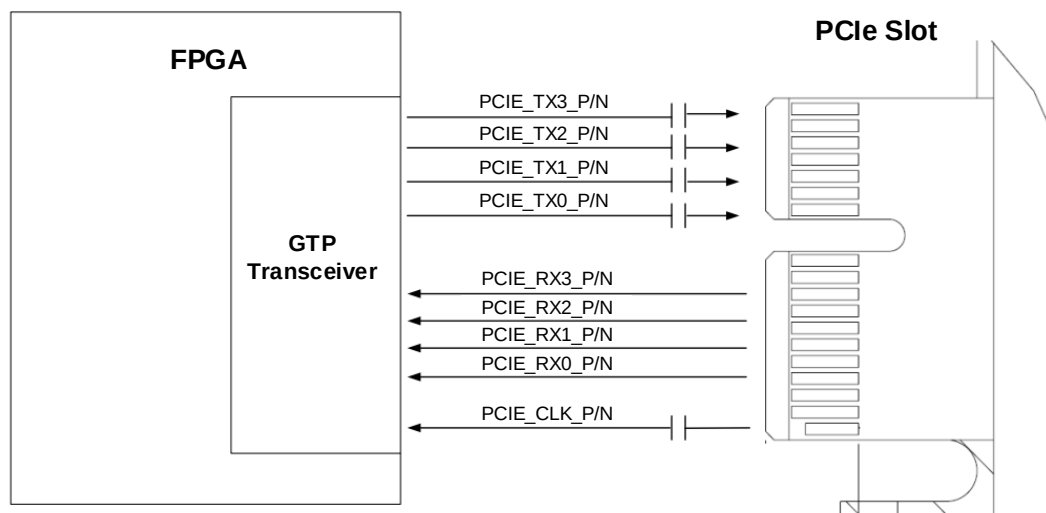
Signal Name	FPGA Pin No.	BANK	I/O Level	Schematic Page
TDI	H10	10	3.3V	3
TDO	J10	10	3.3V	3
TCK	H12	10	3.3V	3
TMS	H11	10	3.3V	3

3.10 PCIe x4 Interface

3.10.1 Introduction

The DK_START_GW5AST-LV138FPG676A_V1.0 development board provides an industrial-grade PCIe x4 interface for high-speed data transfer. The overall dimension of the PCIe card conforms to the standard PCIe card electromechanical specification and can be used directly on the PCIe x4 slot of PC. The transceiver signals of the PCIe interface are directly connected to the GTP transceiver of the FPGA, and the TX and RX signals of the four channels are connected to the FPGA as differential signals. The reference clock of PCIe is provided to the development board by the PCIe slot of the PC. The reference clock rate is 100Mhz. The ESD protection chip is added near the edge connector, and the PCIe interface of the development board is designed as shown in Figure 3-17, where the TX transmit signal and the reference clock CLK signal are connected with AC coupling mode.

Figure 3-17 PCIe x4 Design Diagram



Signal Name	FPGA Pin No.	Description
PCIE_TX3_N	A7	The negative pole of PCIe lane 3 data reception differential signal
PCIE_CLK_Q0_P	F11	Reference clock of PCIe Positive
PCIE_CLK_Q0_N	E11	Reference clock of PCIe Negative

3.11 SSPI, CPU, I2C, SERIAL

3.11.1 Introduction

The development board pulls the pins of various configuration modes of the GW5AST-LV138FPG676A chip to the pins and also connects the ESD protection chip for subsequent safe use.

The pin for SSPI configuration mode is pulled to pin J3; the pin for CPU configuration mode is pulled to pin J4, J222; the pin for I2C configuration mode is pulled to pin J5; the pin for SERIAL configuration mode is pulled to pin J60.

Figure 3-19 Configuration Pin Schematic Design

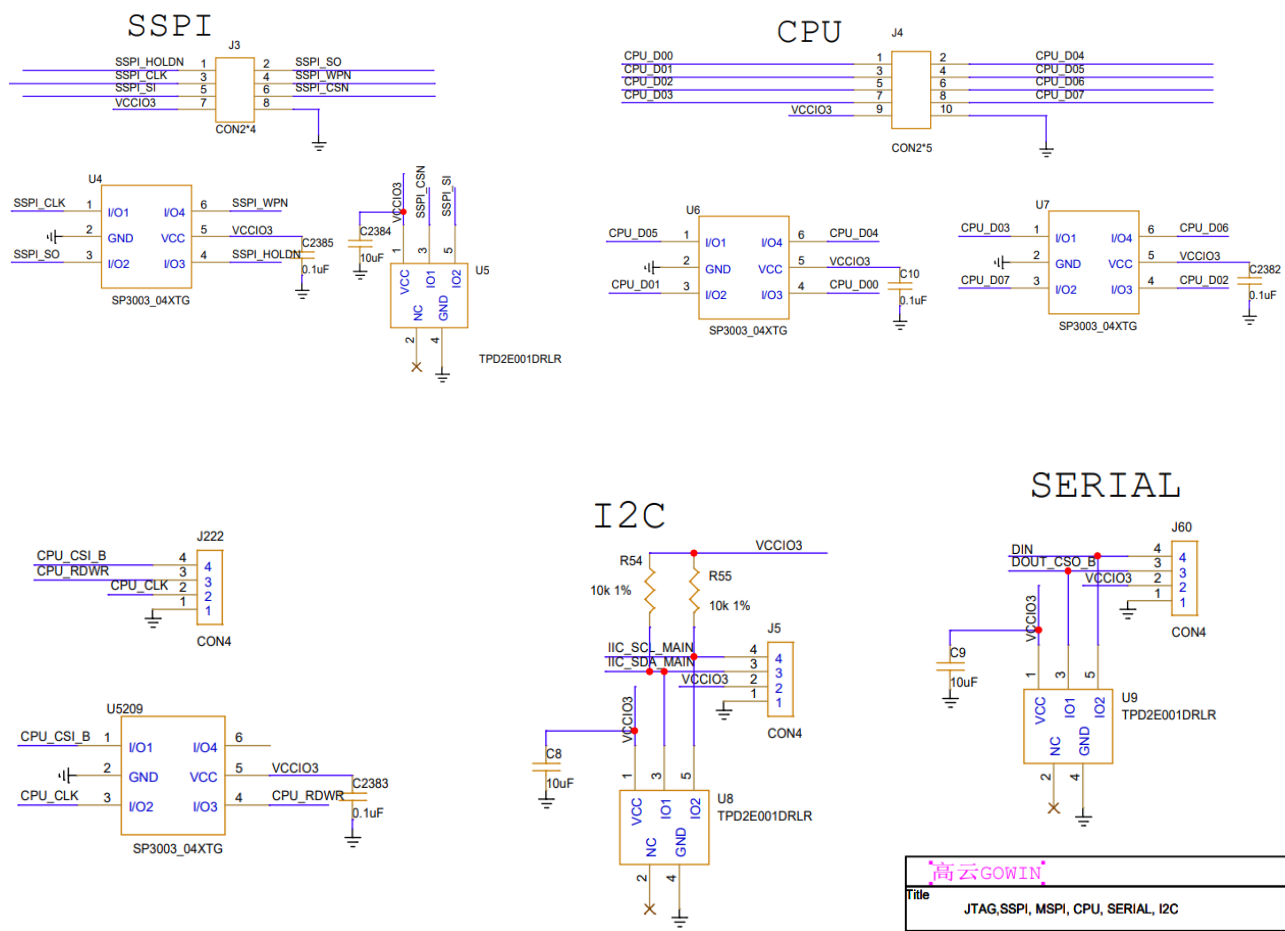
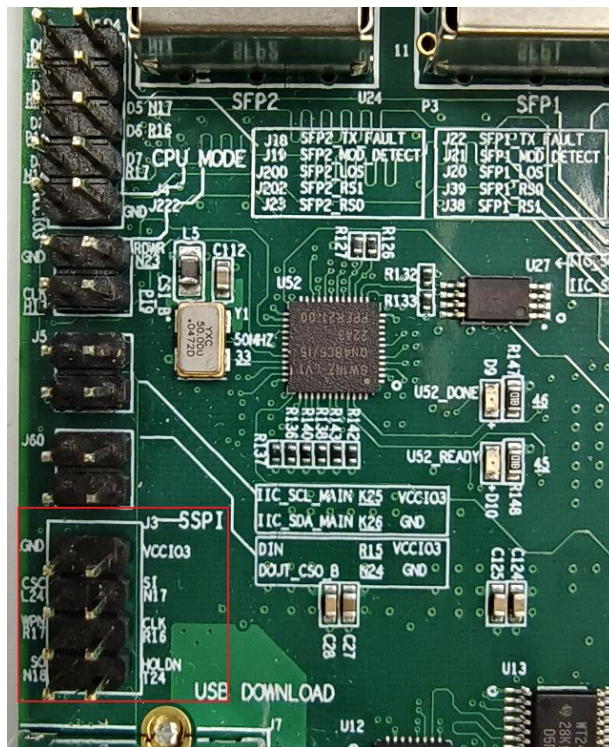


Figure 3-20 Configuration pin circuit on Development Board



3.11.2 Pinout

Table 3-13 Configuration Pinout

Signal Name	FPGA Pin No.	BANK	Designator	I/O Level
SSPI_HOLDN	T24	3	J3	3.3V
SSPI_CLK	R16	3	J3	3.3V
SSPI_SI	N17	3	J3	3.3V
SSPI_SO	N18	3	J3	3.3V
SSPI_WPN	R17	3	J3	3.3V
SSPI_CSN	L24	3	J3	3.3V
CPU_D00	R14	3	J4	3.3V
CPU_D01	R15	3	J4	3.3V
CPU_D02	P14	3	J4	3.3V
CPU_D03	N14	3	J4	3.3V
CPU_D04	N16	3	J4	3.3V
CPU_D05	N17	3	J4	3.3V
CPU_D06	R16	3	J4	3.3V
CPU_D07	R17	3	J4	3.3V
CPU_CSI_B	P19	3	J222	3.3V
CPU_RDWR	N23	3	J222	3.3V

Signal Name	FPGA Pin No.	BANK	Designator	I/O Level
CPU_CLK	H13	3	J222	3.3V
IIC_SCL_MAIN	K25	3	J5	3.3V
IIC_SDA_MAIN	K26	3	J5	3.3V
DIN	R15	3	J60	3.3V
DOUT_CSO_B	N24	3	J60	3.3V

3.12 XADC Interface

3.12.1 Introduction

The DK_START_GW5AST-LV138FPG676A_V1.0 development board is extended with a connector interface for XADC. The connector uses a 2x4 double-row pin with 2.54mm pitch. The analog-to-digital converter connected to the FPGA is as shown in Figure 3-21. Anti-aliasing filter designed for 2 differential XADC inputs.

Figure 3-21 Schematic Connection Diagram of XADC

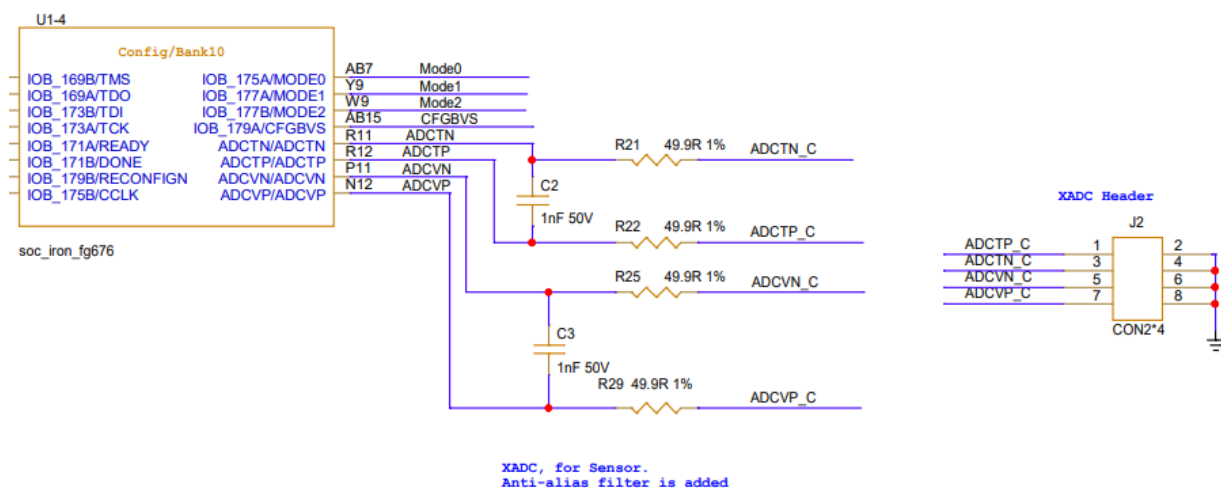
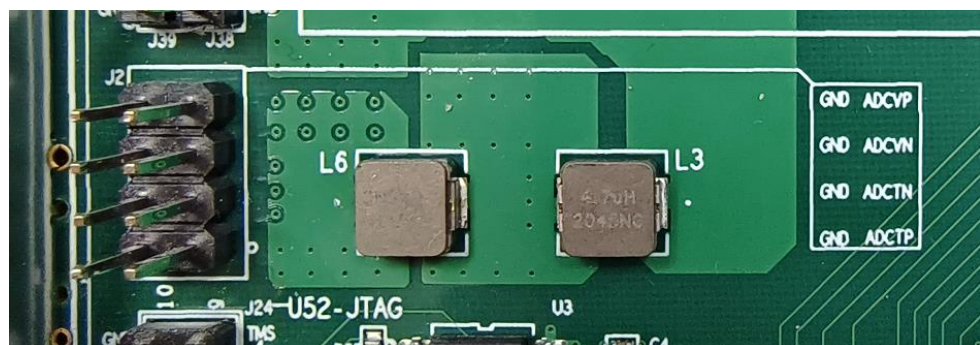


Figure 3-22 XADC Pin Circuit on Development Board



3.12.2 Pinout

Table 3-14 XADC Pinout

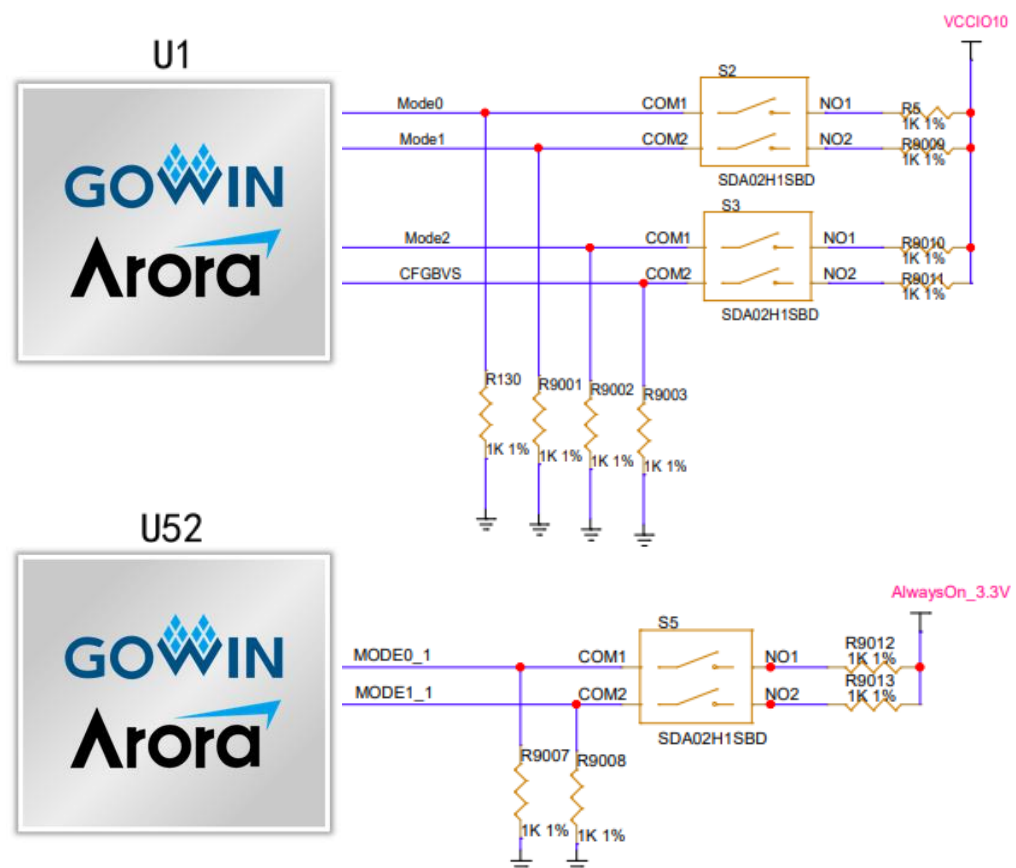
Signal Name	FPGA Pin No.	BANK	XADC Interface	IO Level
ADCTP	R12	10	J2.1	3.3V
ADCTN	R11	10	J2.3	3.3V
ADCVP	N12	10	J2.7	3.3V
ADCVN	P11	10	J2.5	3.3V

3.13 MODE, CFGBVS

3.13.1 Introduction

The development board has S2, S3, and S5 DIP switches for setting up CFGBVS and MODE. S2, S3 for GW5AST-LV138FPG676A (U1) and S5 for GW1NZ-LV1QN48 (U52). The schematic diagram is as shown in Figure 3-23.

Figure 3-23 Schematic Connection Diagram of CFGBVS and MODE



Configuration Banks Voltage Select (CFGBVS) is the voltage

selection signal for the configuration BANK, which refers to BANK3, BANK4, and BANK10. When CFGBVS is High, the BANK voltage defaults to 3.3V, 2.5V.

When the FPGA powers on or a low pulse triggers the RECONFIG_N, the device enters the corresponding GowinCONFIG state according to the MODE value. Note that when the MODE value changes, power-on again or providing one low pulse for triggering RECONFIG_N is required for it to take effect. The configuration modes corresponding to different mode values are as shown in Figure Table 3-15.

Table 3-15 Configuration Mode Selection

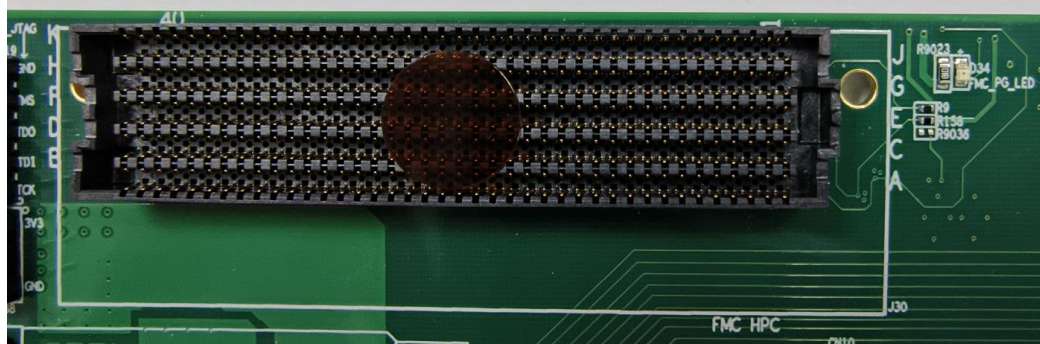
Configuration Mode	MODE[2:0] ^[1]	Bus Width	Description
JTAG	XXX/101 ^[3]	-	Arora V FPGA products are configured by external Host via JTAG interface
MSPI ^[2]	001	x1, x2, x4	As a Master, FPGA reads data from external Flash (or other devices) via the SPI interface for configuration
SSPI ^[2]	010	x1, x4	Arora V FPGA products are configured by external Host via SPI interface
Master SERIAL	000	x1	Before FPGA used as a Slave, FPGA reads data from external devices via the DIN interface for configuration
Slave SERIAL	111	x1	Arora V FPGA products are configured by external Host via DIN interface
Master CPU	100	x8, x16, x32	Before FPGA used as a Slave, FPGA reads data from external devices via the DBUS interface for configuration
Slave CPU	110	x8, x16, x32	Arora V FPGA products are configured by external Host via DBUS interface

Note!

- ^[1] Please refer to the related Pinout manuals for the status of the unbound MODE pins.
- ^[2] The SPI interfaces of the SSPI and MSPI modes are independent of each other.
- ^[3] The JTAG configuration mode is independent of the MODE [2:0] values; If the MODE [2:0] value is 101, only the JTAG mode is available.

- 2 GTP transceiver reference clocks
- 2 external input differential reference clocks
- 159 GNDs and 15 power connections

Figure 3-25 FMC HPC Circuit on Development Board



3.14.2 Pinout

Table 3-17 WIFI Pinout

Signal Name	FPGA (U1) Pin No.	FMC HPC Connector (J30) Pin No.	I/O Level
FMC1_HPC_DP1_M2C_P	D9	A2	-
FMC1_HPC_DP1_M2C_N	A10	A3	-
FMC1_HPC_DP1_C2M_P	B8	A22	-
FMC1_HPC_DP1_C2M_N	C8	A23	-
FMC1_HPC_GBTCLK1_M2C_P	AA13	B20	-
FMC1_HPC_GBTCLK1_M2C_N	AB13	B21	-
FMC1_HPC_DP0_C2M_P	C2	C2	-
FMC1_HPC_DP0_C2M_N	C3	C3	-
FMC1_HPC_DP0_M2C_P	AC14	C6	-
FMC1_HPC_DP0_M2C_N	AD14	C7	-
FMC1_HPC_LA06_P	F18	C10	2.5V
FMC1_HPC_LA06_N	F19	C11	2.5V
FMC1_HPC_LA10_P	E20	C14	2.5V
FMC1_HPC_LA10_N	D20	C15	2.5V
FMC1_HPC_LA14_P	C17	C18	2.5V
FMC1_HPC_LA14_N	B17	C19	2.5V
FMC1_HPC_LA18_CC_P	G20	C22	2.5V
FMC1_HPC_LA18_CC_N	G21	C23	2.5V
FMC1_HPC_LA27_P	G25	C26	2.5V
FMC1_HPC_LA27_N	F25	C27	2.5V

Signal Name	FPGA (U1) Pin No.	FMC HPC Connector (J30) Pin No.	I/O Level
FMC1_IIC_SCL	U52.15	C30	-
FMC1_IIC_SDA	U52.16	C31	-
GA0 = 0 = GND	-	C34	-
VCC12_P	-	C35	-
VCC12_P	-	C37	-
VCC3V3	-	C39	-
PG_C2M	J14	D1	2.5V
FMC1_HPC_GBTCLK0_M2C_P	AA11	D4	-
FMC1_HPC_GBTCLK0_M2C_N	AB11	D5	-
FMC1_HPC_LA01_CC_P	E17	D8	2.5V
FMC1_HPC_LA01_CC_N	E18	D9	2.5V
FMC1_HPC_LA05_P	G19	D11	2.5V
FMC1_HPC_LA05_N	F20	D12	2.5V
FMC1_HPC_LA09_P	C21	D14	2.5V
FMC1_HPC_LA09_N	B21	D15	2.5V
FMC1_HPC_LA13_P	B19	D17	2.5V
FMC1_HPC_LA13_N	A19	D18	2.5V
FMC1_HPC_LA17_CC_P	K21	D20	2.5V
FMC1_HPC_LA17_CC_N	J21	D21	2.5V
FMC1_HPC_LA23_P	K22	D23	2.5V
FMC1_HPC_LA23_N	K23	D24	2.5V
FMC1_HPC_LA26_P	L17	D26	2.5V
FMC1_HPC_LA26_N	L18	D27	2.5V
FMC1_TCK	U19.1	D29	-
FMC1_TDI	U19.2	D30	-
FMC1_TDO	U19.3	D31	-
AlwaysOn_3.3V	-	D32	-
FMC1_TMS	U19.4	D33	-
AlwaysOn_3.3V	-	D36	-
AlwaysOn_3.3V	-	D38	-
AlwaysOn_3.3V	-	D40	-
FMC1_HPC_HA01_CC_P	W21	E2	2.5V
FMC1_HPC_HA01_CC_N	Y21	E3	2.5V
FMC1_HPC_HA05_P	V23	E6	2.5V

Signal Name	FPGA (U1) Pin No.	FMC HPC Connector (J30) Pin No.	I/O Level
FMC1_HPC_HA05_N	W23	E7	2.5V
FMC1_HPC_HA09_P	V19	E9	2.5V
FMC1_HPC_HA09_N	W19	E10	2.5V
FMC1_HPC_HA13_P	AA22	E12	2.5V
FMC1_HPC_HA13_N	AA23	E13	2.5V
FMC1_HPC_HA16_P	Y25	E15	2.5V
FMC1_HPC_HA16_N	AA25	E16	2.5V
FMC1_HPC_HA20_P	V26	E18	2.5V
FMC1_HPC_HA20_N	W26	E19	2.5V
VCCIO_ADJ	-	E39	-
FMC1_HPC_PG_M2C	P15	F1	2.5V
FMC1_HPC_HA00_CC_P	U21	F4	2.5V
FMC1_HPC_HA00_CC_N	V21	F5	2.5V
FMC1_HPC_HA04_P	V16	F7	2.5V
FMC1_HPC_HA04_N	V17	F8	2.5V
FMC1_HPC_HA08_P	W20	F10	2.5V
FMC1_HPC_HA08_N	Y20	F11	2.5V
FMC1_HPC_HA12_P	AB24	F13	2.5V
FMC1_HPC_HA12_N	AC24	F14	2.5V
FMC1_HPC_HA15_P	AB26	F16	2.5V
FMC1_HPC_HA15_N	AC26	F17	2.5V
FMC1_HPC_HA19_P	U25	F19	2.5V
FMC1_HPC_HA19_N	U26	F20	2.5V
VCCIO_ADJ	-	F40	-
FMC1_HPC_CLK1_M2C_P	H21	G2	2.5V
FMC1_HPC_CLK1_M2C_N	H22	G3	2.5V
FMC1_HPC_LA00_CC_P	D18	G6	2.5V
FMC1_HPC_LA00_CC_N	C18	G7	2.5V
FMC1_HPC_LA03_P	E21	G9	2.5V
FMC1_HPC_LA03_N	D21	G10	2.5V
FMC1_HPC_LA08_P	A17	G12	2.5V
FMC1_HPC_LA08_N	A18	G13	2.5V
FMC1_HPC_LA12_P	E16	G15	2.5V
FMC1_HPC_LA12_N	D16	G16	2.5V

Signal Name	FPGA (U1) Pin No.	FMC HPC Connector (J30) Pin No.	I/O Level
FMC1_HPC_LA16_P	G15	G18	2.5V
FMC1_HPC_LA16_N	F15	G19	2.5V
FMC1_HPC_LA20_P	M16	G21	2.5V
FMC1_HPC_LA20_N	M17	G22	2.5V
FMC1_HPC_LA22_P	J24	G24	2.5V
FMC1_HPC_LA22_N	H24	G25	2.5V
FMC1_HPC_LA25_P	G24	G27	2.5V
FMC1_HPC_LA25_N	F24	G28	2.5V
FMC1_HPC_LA29_P	E25	G30	2.5V
FMC1_HPC_LA29_N	D25	G31	2.5V
FMC1_HPC_LA31_P	G22	G33	2.5V
FMC1_HPC_LA31_N	F22	G34	2.5V
FMC1_HPC_LA33_P	J19	G36	2.5V
FMC1_HPC_LA33_N	H19	G37	2.5V
VCCIO_ADJ	-	G39	-
FMC1_HPC_PRSNT_M2C_B	N16	H2	3.3V
FMC1_HPC_CLK0_M2C_P	D19	H4	2.5V
FMC1_HPC_CLK0_M2C_N	C19	H5	2.5V
FMC1_HPC_LA02_P	B22	H7	2.5V
FMC1_HPC_LA02_N	A22	H8	2.5V
FMC1_HPC_LA04_P	B20	H10	2.5V
FMC1_HPC_LA04_N	A20	H11	2.5V
FMC1_HPC_LA07_P	H14	H13	2.5V
FMC1_HPC_LA07_N	H15	H14	2.5V
FMC1_HPC_LA11_P	G17	H16	2.5V
FMC1_HPC_LA11_N	F17	H17	2.5V
FMC1_HPC_LA15_P	H16	H19	2.5V
FMC1_HPC_LA15_N	G16	H20	2.5V
FMC1_HPC_LA19_P	M14	H22	2.5V
FMC1_HPC_LA19_N	L14	H23	2.5V
FMC1_HPC_LA21_P	H26	H25	2.5V
FMC1_HPC_LA21_N	G26	H26	2.5V
FMC1_HPC_LA24_P	E26	H28	2.5V
FMC1_HPC_LA24_N	D26	H29	2.5V

Signal Name	FPGA (U1) Pin No.	FMC HPC Connector (J30) Pin No.	I/O Level
FMC1_HPC_LA28_P	F23	H31	2.5V
FMC1_HPC_LA28_N	E23	H32	2.5V
FMC1_HPC_LA30_P	K20	H34	2.5V
FMC1_HPC_LA30_N	J20	H35	2.5V
FMC1_HPC_LA32_P	J18	H37	2.5V
FMC1_HPC_LA32_N	H18	H38	2.5V
VCCIO_ADJ	-	H40	-
FMC1_HPC_HA03_P	U14	J6	2.5V
FMC1_HPC_HA03_N	V14	J7	2.5V
FMC1_HPC_HA07_P	V18	J9	2.5V
FMC1_HPC_HA07_N	W18	J10	2.5V
FMC1_HPC_HA11_P	U22	J12	2.5V
FMC1_HPC_HA11_N	V22	J13	2.5V
FMC1_HPC_HA14_P	AA24	J15	2.5V
FMC1_HPC_HA14_N	AB25	J16	2.5V
FMC1_HPC_HA18_P	W25	J18	2.5V
FMC1_HPC_HA18_N	Y26	J19	2.5V
FMC1_HPC_HA22_P	V24	J21	2.5V
FMC1_HPC_HA22_N	W24	J22	2.5V
FMC1_HPC_HA02_P	T14	K7	2.5V
FMC1_HPC_HA02_N	T15	K8	2.5V
FMC1_HPC_HA06_P	U15	K10	2.5V
FMC1_HPC_HA06_N	U16	K11	2.5V
FMC1_HPC_HA10_P	T20	K13	2.5V
FMC1_HPC_HA10_N	U20	K14	2.5V
FMC1_HPC_HA17_CC_P	Y22	K16	2.5V
FMC1_HPC_HA17_CC_N	Y23	K17	2.5V
FMC1_HPC_HA21_P	T17	K19	2.5V
FMC1_HPC_HA21_N	T18	K20	2.5V
FMC1_HPC_HA23_P	T19	K22	2.5V
FMC1_HPC_HA23_N	U19	K23	2.5V

3.15 SFP/SFP+ Connector

3.15.1 Introduction

The development board includes two compact pluggable (SFP+) connectors and rack mount kits (P3) that can be inserted into SFP or SFP+ modules. Figure 3-26 shows the SFP+ module connector circuits.

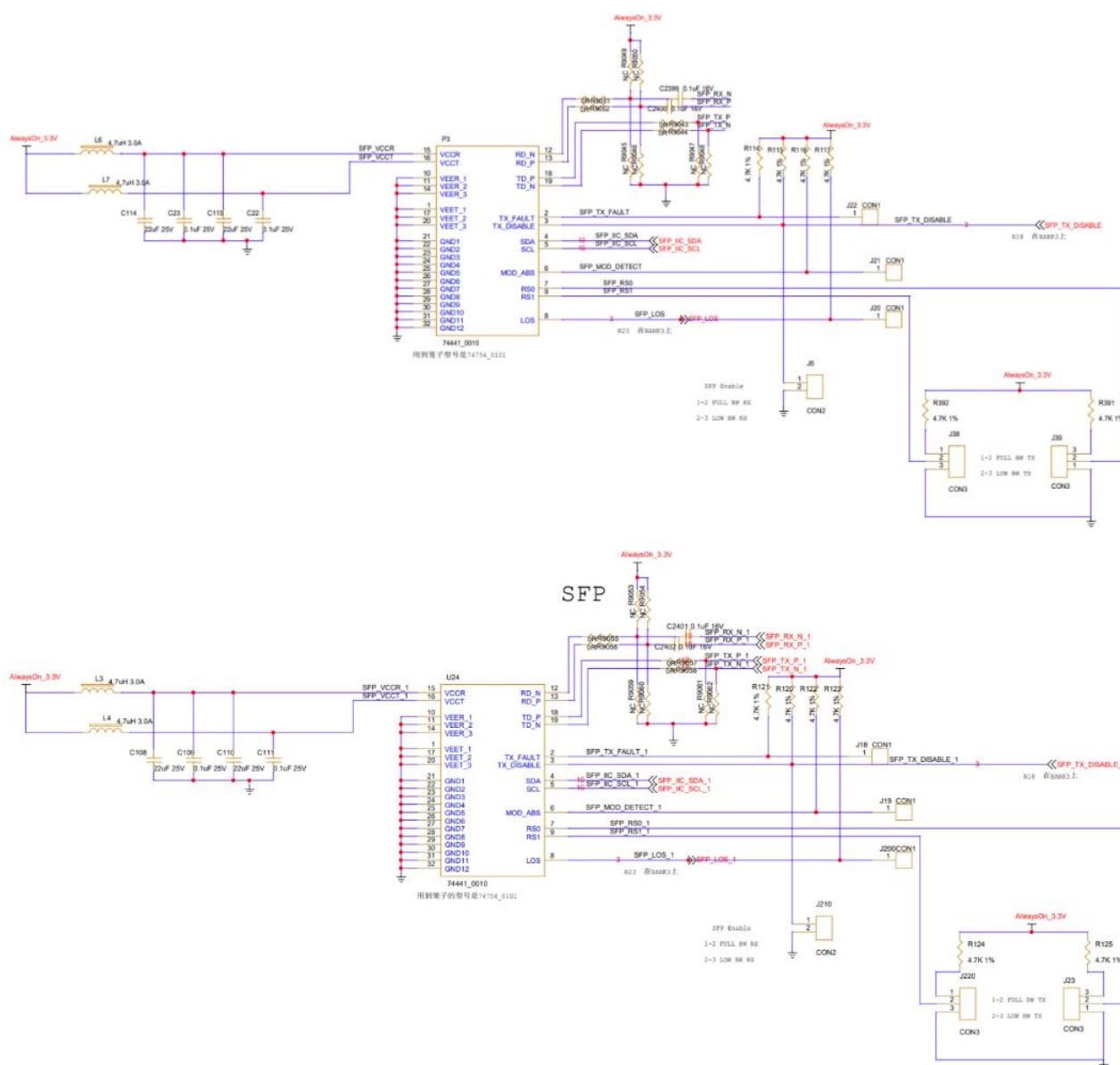
In order to adapt to more models of optical modules, an interface circuit has been added to the RX and TX differential signal circuits of the SFP+ module connector. The details are as follows:

The alternate interface circuit for the TX signal of the P3 connector consists of R9043, R9044, R9047, and R9048, and the alternate interface circuit is placed near the P3 connector in the circuit board;

P3 connector RX signal alternate interface circuit consists of R9049, R9050, R9045, R9046, R9051, R9052, C2399, C2400, alternate interface circuit in the circuit board is placed near the U1 FPGA; users adjust the interface circuit according to the specific electrical standards in the actual use of different optical modules.

The alternate interface circuit for the TX signal of the U24 connector consists of R9057, R9058, R9061, R9062, and the alternate interface circuit is placed near the U24 connector in the circuit board;

U24 connector RX signal alternate interface circuit consists of R9055, R9056, R9053, R9054, R9059, R9060, C2401, C2402, alternate interface circuit in the circuit board is placed near the U1 FPGA; users adjust the interface circuit according to the specific electrical standards in the actual use of different optical modules.



The SFP+ module control and status pins are shown in Table 3-17.

Table 3-17 SFP + Module Control and Status Pin

SFP Control Status Signal Network Name	Signal Description	Development Board Connection
SFP_TX_FAULT	P3 transmitting error	Connect to J22 test point High: Error Transmit; Low: Normal Transmit
SFP_TX_FAULT_1	U24 transmitting error	Connect to J18 test point High: Error Transmit; Low: Normal Transmit
SFP_TX_DISABLE	P3 transmitting enable	Connect to J6 pin, connect pin when transmitting High or Floating: Transmitting Disallowed; Low: Transmitting Allowed
SFP_TX_DISABLE_1	U24 transmitting enable	Connect to J210 pin, connect pin when transmitting High or Floating: Transmitting Disallowed; Low: Transmitting Allowed
SFP_MOD_DETECT	P3 detects if an SFP+ module is plugged in	Connect to J21 High: No SFP+ module in P3 slot; Low: SFP+ module in P3 slot
SFP_MOD_DETECT_1	U24 detects if an SFP+ module is plugged in	Connect to J19 High: No SFP+ module in U24 slot; Low: SFP+ module in U24 slot
SFP_RS0	P3 speed is selected as 0	Connect to J39 1-2 = full receiver bandwidth; 2-3 = reduced receiver bandwidth
SFP_RS1	P3 speed is selected as 1	Connect to J38 1-2 = full transmitter bandwidth; 2-3 = reduced transmitter bandwidth
SFP_RS0_1	U24 speed is selected as 0	Connect to J23 1-2 = full receiver bandwidth; 2-3 = reduced receiver bandwidth
SFP_RS1_1	U24 speed is selected as 1	Connect to J220 1-2 = full transmitter bandwidth; 2-3 = reduced transmitter bandwidth
SFP_LOS	P3 Signal Loss Indicator	Connect to J20 High: Receiver Signal Loss; LOW: Normal Operation
SFP_LOS_1	U24 Signal Loss Indicator	Connect to J200 High: Receiver Signal Loss; LOW: Normal Operation

3.15.2 Pinout

Table 3-18 FPGA U1 to SFP+ Module Connection

Network Name	FPGA Pin No.	SFP + Pin No.
SFP_RX_N	U1.AD12	P3.12
SFP_RX_P	U1.AC12	P3.13
SFP_TX_N	U1.AD10	P3.19
SFP_TX_P	U1.AC10	P3.18
SFP_LOS	U1.R23	P3.8
SFP_TX_DISABLE	U1.R18	P3.3
SFP_IIC_SDA	U52.20	P3.4
SFP_IIC_SCL	U52.19	P3.5
SFP_RX_N_1	U1.M25	U24.12
SFP_RX_P_1	U1.M24	U24.13
SFP_TX_N_1	U1.L23	U24.19
SFP_TX_P_1	U1.L22	U24.18
SFP_LOS_1	U1.R25	U24.8
SFP_TX_DISABLE_1	U1.M20	U24.3
SFP_IIC_SDA_1	U52.21	U24.4
SFP_IIC_SCL_1	U52.22	U24.5

3.16 MIPI

3.16.1 Introduction

The MIPI interface on the development board uses 80pin AXK580137YG connectors with 0.5mm pitch. The FPGA leads to 10 pairs of differential signals, including 2 pairs of clock signals and 8 pairs of data signals, 34 single-ended signals, power supply and GND. The schematic circuit is as shown in Figure 3-28.

Figure 3-28 Schematic Circuit of MIPI Interface

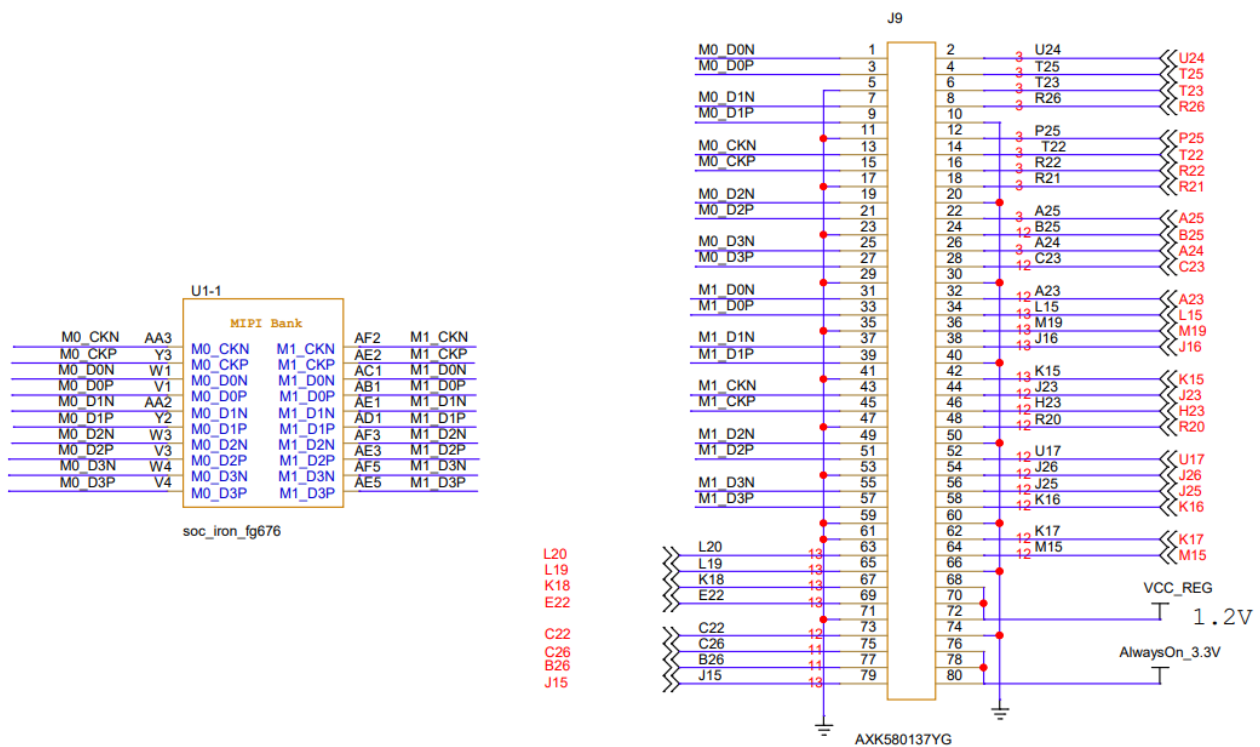


Figure 3-29 MIPI Circuit on Development Board



3.16.2 Pinout

Table 3-19 MIPI Interface Pinout

Signal Name	FPGA Pin No.	MIPI Socket Pin No.	I/O Level
M0_D0N	W1	J9.1	-
M0_D0P	V1	J9.3	-
M0_D1N	AA2	J9.7	-
M0_D1P	Y2	J9.9	-
M0_D2N	W3	J9.13	-
M0_D2P	V3	J9.15	-
M0_D3N	W4	J9.19	-
M0_D3P	V4	J9.21	-
M0_CKN	AA3	J9.25	-
M0_CKP	Y3	J9.27	-
M1_D0N	AC1	J9.31	-
M1_D0P	AB1	J9.33	-
M1_D1N	AE1	J9.37	-
M1_D1P	AD1	J9.39	-
M1_D2N	AF3	J9.43	-
M1_D2P	AE3	J9.45	-
M1_D3N	AF5	J9.49	-
M1_D3P	AE5	J9.51	-
M1_CKN	AF2	J9.55	-
M1_CKP	AE2	J9.57	-
L20	L20	J9.63	-
L19	L19	J9.65	-
K18	K18	J9.67	-
E22	E22	J9.69	-
C22	C22	J9.73	-
C26	C26	J9.75	-
B26	B26	J9.77	-
J15	J15	J9.79	-
U24	U24	J9.2	-
T25	T25	J9.4	-
T23	T23	J9.6	-
R26	R26	J9.8	-

Signal Name	FPGA Pin No.	MIPI Socket Pin No.	I/O Level
P25	P25	J9.12	-
T22	T22	J9.14	-
R22	R22	J9.16	-
R21	R21	J9.18	-
A25	A25	J9.22	-
B25	B25	J9.24	-
A24	A24	J9.26	-
C23	C23	J9.28	-
A23	A23	J9.32	-
L15	L15	J9.34	-
M19	M19	J9.36	-
J16	J16	J9.38	-
K15	K15	J9.42	-
J23	J23	J9.44	-
H23	H23	J9.46	-
R20	R20	J9.48	-
U17	U17	J9.52	-
J26	J26	J9.54	-
J25	J25	J9.56	-
K16	K16	J9.58	-
K17	K17	J9.62	-
M15	M15	J9.64	-

4 Appendix

