



Gowin RoraLink 8B10B IP User Guide

IPUG1190-1.2E, 03/07/2025

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Revision History

Date	Version	Description
07/05/2024	1.0E	Initial version published.
10/25/2024	1.1E	Descriptions of "Reference Clock Source" configuration option updated.
03/07/2025	1.2E	"Channel Bonding" and "RX Clock Correction" configuration options added.

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1 About This Guide

1.1 Purpose

Gowin RoraLink 8B10B IP User Guide is designed to help you learn the features and usage of Gowin RoraLink 8B10B IP by providing descriptions of functions, GUI, and reference design, etc. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.11.01. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com.

- [SUG100, Gowin Software User Guide](#)
- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
CB	Channel Bonding
ICC	Clock Tolerance Compensation
CRC	Cyclic Redundancy Code
ECP	End of Channel PDU
FPGA	Field Programmable Gate Array
IP	Intellectual Property
NFC	Native Flow Control Interface
PCS	Physical Coding Sublayer
PDU	Protocol Data Unit

Terminology and Abbreviations	Meaning
PMA	Physical Medium Attachment Sublayer
SCP	Start of Channel PDU
UFC	User Flow Control RX Interface

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Function Overview

2.1 Overview

Gowin RoraLink 8B10B IP provides users with an extensible and lightweight transmission solution. It utilizes the 8B/10B encoding and decoding, offering user-friendly data interfaces and flow control interfaces.

Table 2-1 Gowin RoraLink 8B10B IP Overview

Gowin RoraLink 8B10B IP	
Logic Resource	See Table 2-2
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.10 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features

- Supports 1~8 lanes
- Supports simplex or full-duplex operations
- Supports 8B/10B encoding and decoding
- Supports RX Channel Bonding (CB) alignment and clock adjustment
- Supports serial data scrambling and descrambling
- Supports big-endian or little-endian
- Supports CRC32 and CRC16
- Provides user-friendly data interfaces and flow control interfaces

2.3 Resource Utilization

Gowin RoraLink 8B10B IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW5AT series of FPGA as an instance, the resource utilization of Gowin RoraLink 8B10B IP is as shown in Table 2-2.

Table 2-2 Gowin RoraLink 8B10B IP Resource Utilization

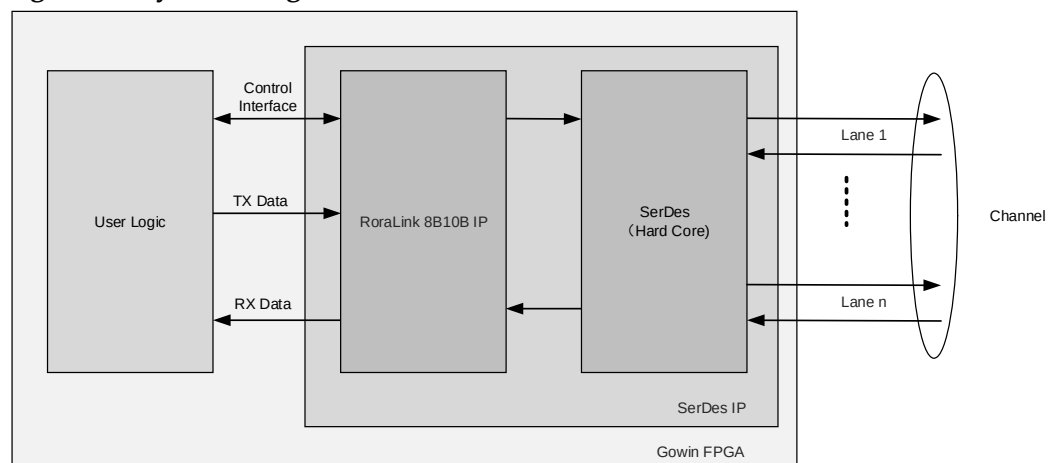
Lane Width	Dataflow Mode	Data Width Per Lane	Interface	Resource Utilization		
				REG	LUT	BSRAM
1	Duplex	2	Framing	1033	527	2
			Streaming	923	478	2
		4	Framing	1472	849	2
			Streaming	1134	645	2
	RX-only Simplex	2	Framing	705	354	2
			Streaming	662	341	2
		4	Framing	1089	652	2
			Streaming	856	491	2
	TX-only Simplex	2	Framing	356	132	0
			Streaming	289	100	0
		4	Framing	408	150	0
			Streaming	301	113	0
2	Duplex	2	Framing	1805	1010	4
			Streaming	1471	809	4
		4	Framing	2667	1792	4
			Streaming	1956	1166	4
	RX-only Simplex	2	Framing	1346	763	4
			Streaming	1115	604	4
		4	Framing	1979	1479	4
			Streaming	1530	924	4
	TX-only Simplex	2	Framing	457	183	0
			Streaming	354	145	0
		4	Framing	681	240	0
			Streaming	415	175	0

3 Functional Description

3.1 System Block Diagram

The system diagram of Gowin RoraLink 8B10B IP is shown in Figure 3-1. The IP includes both the hard core SerDes and the soft IP core. The SerDes hard core implements functions such as 8B10B encoding/decoding and RX channel bonding alignment, and the soft IP core implement functions such as scrambling/descrambling, link initialization, and data transmission. The SerDes module transmits data encoded with 8B/10B, and users can connect with the counterpart device using 1~8 lanes, utilizing multiple lanes to transmit data for one channel.

Figure 3-1 System Diagram



3.2 Operating Frequency

The operating frequency of the Gowin RoraLink 8B10B IP is related to the SerDes line rate and the Data Width Per Lane option on the GUI.

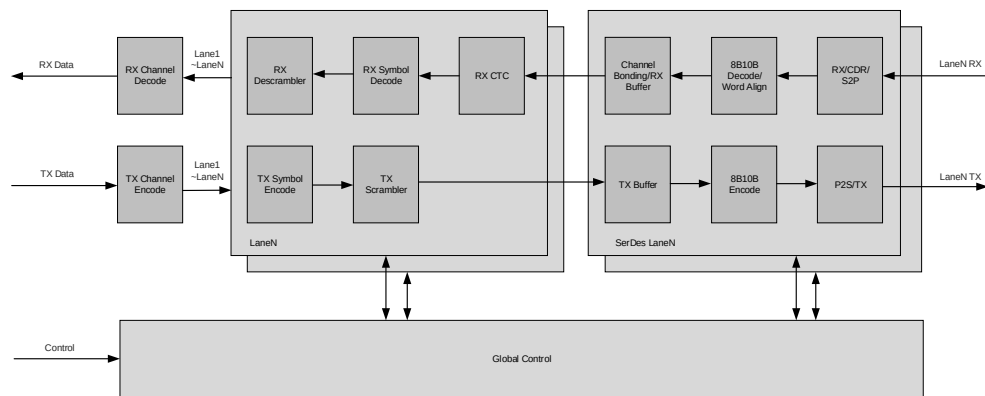
- When "2" Bytes is selected for Data Width Per Lane on the GUI, and the operating clock frequency is calculated as the formula $\text{clock} = \text{line rate} / 20 \text{ bits}$. For example, if the line rate for a single Lane is 3.125 Gbps, then the operating clock frequency is calculated as follows:
 $\text{clock} = 3.125 \text{ Gbps} / 20 \text{ bits} = 156.25 \text{ MHz}$.
- When "4" Bytes is selected for Data Width Per Lane on the GUI, and the operating clock frequency is calculated as the formula $\text{clock} = \text{line}$

rate/40 bits. For example, if the line rate for a single Lane is 3.125 Gbps, then the operating clock frequency is calculated as follows:
 $\text{clock} = 3.125 \text{ Gbps} / 40 \text{ bits} = 78.125 \text{ MHz}.$

3.3 Operating Principles

The structure diagram of Gowin RoraLink 8B10B IP is as shown in Figure 3-2. The functions of each module are described as follows:

- Global Control: The global control module manages IP SerDes lanes, IP initialization, link monitoring, and reset, etc.
- TX Data: The user inputs data, and the IP processes the data and controls the flow, scrambles the data, encodes it with SerDes 8B10B, and then transmits the data.
 - TX Channel Encode: Processes TX user data, flow control data, including interface conversion, flow control, endianness conversion, adding CRC fields, etc. The CRC calculation formula depends on the option Data Width Per Lane on the GUI. When the option Data Width Per Lane is set to "2" Bytes on the GUI, CRC16 uses the formula: $G(X) = X^{16} + X^{12} + X^5 + 1$. When the option Data Width Per Lane is set to "4" Bytes on the GUI, CRC32 uses the formula: $G(X) = X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$.
 - TX Symbol Encode: TX Channel Encode output data will be input into multiple lanes, and control symbols will be added to this data.
 - TX Scrambler: The TX scrambler module scrambles the data using the formula: $G(X) = X^{16} + X^5 + X^4 + X^3 + 1$. Only the data is scrambled.
- RX Data: The IP receives SerDes data, and sends it to users after operations of gearbox, block synchronization, descrambling, clock compensation, channel bonding alignment, and data decoding.
 - RX Descrambler: The RX descrambler module, and it is only descrambles the data.
 - RX CTC: RX clock adjustment module.
 - RX Symbol Decode: Receives and processes control symbols.
 - RX Channel Decode: Processes the received data and sends it to the user. Data processing includes removing CRC fields, endianness conversion, and interface conversion.

Figure 3-2 Structure Diagram

3.4 User Interface

The user interfaces provided by Gowin RoraLink 8B10B IP are described below:

- **Clock Interface:** The user inputs the operating clock of IP Core.
- **Reset Interface:** Allows the user to perform a reset operation on the IP Core, and simultaneously the IP outputs a reset signal to the user-side module.
- **Transmit Data Interface:** User interface for transmitting data.
- **Receive Data Interface:** User interface for receiving data.
- **Native Flow Control (NFC) TX Interface:** User TX interface for NFC, used to control data transfer rate at the RX end.
- **NFC RX Interface:** User RX interface for NFC.
- **User Flow Control (UFC) TX Interface:** User TX interface for UFC, used for transmitting high-priority control messages.
- **UFC RX Interface:** User RX interface for UFC.
- **Status Interface:** Includes internal error status of the IP, lane linking status, channel linking status, and CRC verification status.
- **SerDes-related Interfaces:** SerDes reset and SerDes status interfaces.

3.5 Port List

The I/O port of Gowin RoraLink 8B10B IP is shown in Figure 3-3.

Figure 3-3 Gowin RoraLink 8B10B IP Port Diagram

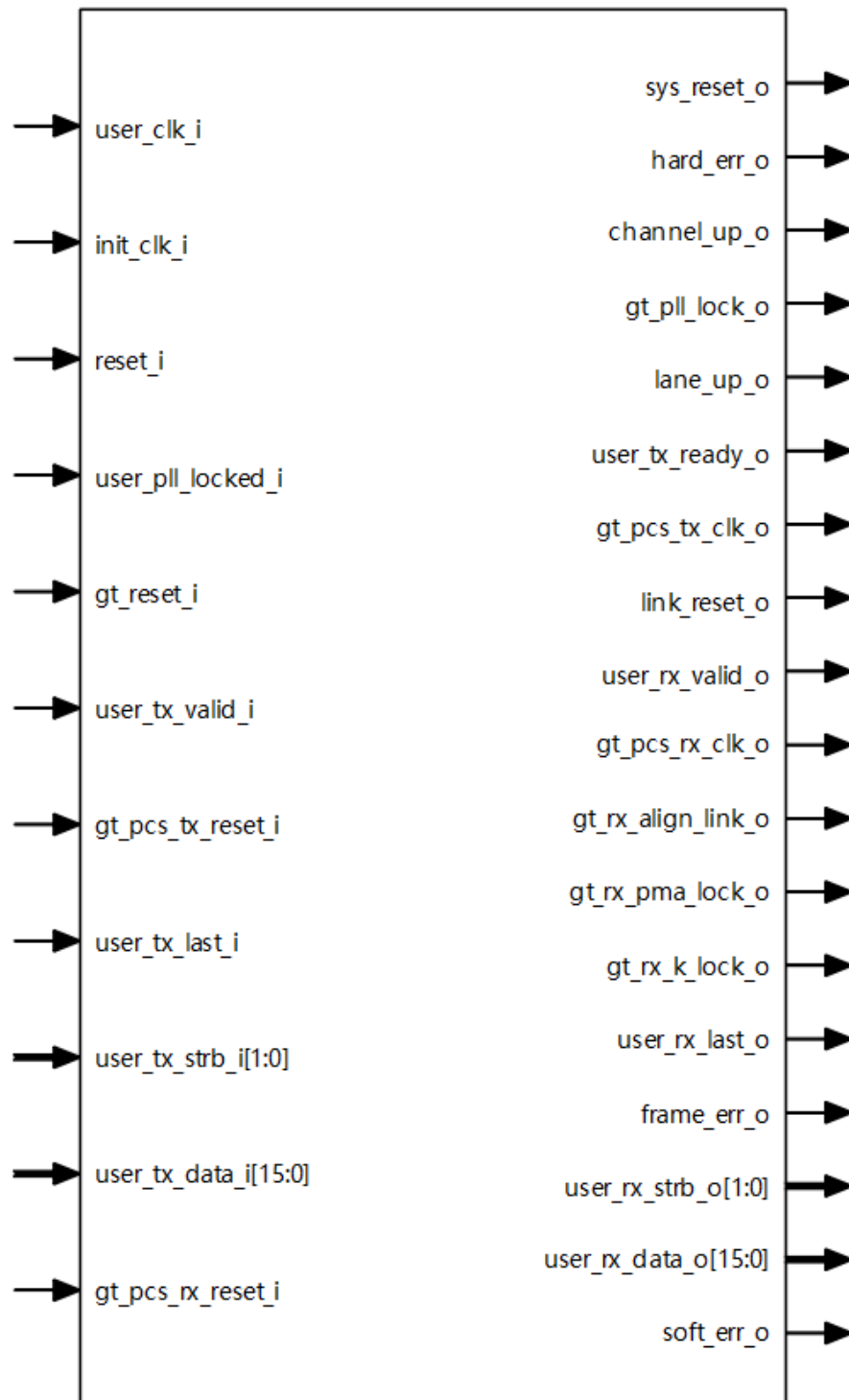


Table 3-1 I/O List of Gowin RoraLink 8B10B IP

Port Name	I/O	Data Width	Description
Clock and reset			
reset_i	input	1	Reset signal, active-high
user_clk_i	input	1	Operating clock, and you can refer to the clock frequency details described in Section 3.2 Operating Frequency .
init_clk_i	input	1	Input the local crystal oscillator 50MHz clock
user_pll_locked_i	input	1	Operating clock corresponding to PLL lock status, active-high.
link_reset_o ^[3]	output	1	RX link reset signal, active-high.
sys_reset_o	output	1	System reset signal, active-high.
User Data Transmission Interface			
user_tx_data_i ^[2]	input	[(8n ^[1] -1):0] or [0:(8n ^[1] -1)]	Transmit user data
user_tx_valid_i ^[2]	input	1	Valid indicator for transmitting user data, active-high.
user_tx_ready_o ^[2]	output	1	Handshake signal for transmitting user data, and data on the bus is valid when both user_tx_ready_o and user_tx_valid_i are high.
user_tx_strb_i ^[2]	input	[(n ^[1] -1):0] or [0:(n ^[1] -1)]	Enable transmitting user data frame-tail byte valid. For example, if user_tx_strb_i is 8'h1f, it indicates that the user_tx_data_i [39:0] is valid, and user_tx_data_i [63:40] is invalid. This signal is only valid when user_tx_valid_i, user_tx_ready_o, and user_tx_last_i are high. Note! This port is only available when the Interface option on the GUI is set to "Framing".
user_tx_last_i ^[2]	input	1	Indicator for transmitting user data frame tail valid; when user_rx_valid_o and user_rx_last_o are high, it indicates the data on the bus is the last data of each frame. Note! This port is only available when the Interface option on the GUI is set to "Framing".
User Data Reception Interface			
user_rx_data_o ^[3]	output	[(8n ^[1] -1):0] or [0:(8n ^[1] -1)]	Receive user data
user_rx_valid_o ^[3]	output	1	Valid indicator for receiving user data; when it is high, the data on the bus is valid.
user_rx_strb_o ^[3]	output	[(n ^[1] -1):0] or [0:(n ^[1] -1)]	Enable receiving user data frame-tail byte valid. For example, if user_rx_strb_o is 8'h1f, it indicates that the user_rx_data_o [39:0] is valid, and user_rx_data_o [63:40] is invalid. This signal is only valid when both user_rx_valid_o and user_rx_last_o are high. Note! This port is only available when the Interface option on the GUI is set to "Framing".
user_rx_last_o ^[3]	output	1	Indicator for receiving user data frame tail valid; when both user_rx_valid_o and user_rx_last_o are high, it indicates the data on the bus is the

Port Name	I/O	Data Width	Description
			last data of each frame. Note! This port is only available when the Interface option on the GUI is set to "Framing".
Native Flow Control TX Interface			
user_tx_nfc_req_i ^{[2][4]}	input	1	NFC TX request signal, active-high.
user_tx_nfc_nb_i ^{[2][4]}	input	[3:0] or [0:3]	NFC TX data, indicating the number of pause idles the partner must send when it receives the NFC message.
user_tx_nfc_ack_o ^{[2][4]}	output	1	NFC TX handshake signal; when user_tx_nfc_ack_o and user_tx_nfc_req_i are high, the data on the bus is valid.
Native Flow Control RX Interface			
user_rx_nfc_fc_nb_o ^{[3][4]}	output	[3:0] or [0:3]	NFC RX data, indicating receiving the pause value sent by the partner.
user_rx_nfc_snf_o ^{[3][4]}	output	1	Valid indicator for NFC RX data, active-high.
User Flow Control TX Interface			
user_ufc_tx_req_i ^{[2][5]}	input	1	UFC TX data request signal, active-high.
user_ufc_tx_ms_i ^{[2][5]}	input	[2:0] or [0:2]	UFC TX data, used to specify the size of UFC messages.
user_ufc_tx_ack_o ^{[2][5]}	output	1	UFC TX data handshake signal; when user_ufc_tx_ack_o and user_ufc_tx_req_i are high, it indicates the data on the bus is valid.
User Flow Control RX Interface			
user_ufc_rx_data_o ^{[3][5]}	output	[(8n ^[1] -1):0]or [0:(8n ^[1] -1)]	UFC RX data, up to 128-bit data width.
user_ufc_rx_strb_o ^{[3][5]}	output	[(n ^[1] -1):0]or [0:(n ^[1] -1)]	Enable receiving UFC frame-tail byte valid. For example, if user_ufc_rx_strb_o is 8'h1f, it indicates that the user_ufc_rx_data_o [39:0] is valid, and ser_ufc_rx_data_o [63:40] is invalid. This signal is only valid when both user_ufc_rx_valid_o and user_ufc_rx_last_o are high.
user_ufc_rx_last_o ^{[3][5]}	output	1	Indicator for receiving user data frame tail valid; when both user_ufc_rx_valid_o and user_ufc_rx_last_o are high, it indicates the data on the bus is the last data of each frame.
user_ufc_rx_valid_o ^{[3][5]}	output	1	Valid indicator for receiving UFC data, active-high.
CRC Status Interface			
crc_pass_fail_n_o ^[6]	output	1	CRC check status; when crc_valid_o is high and crc_pass_fail_n_o is low, it indicates a current CRC error; when crc_valid_o is high and crc_pass_fail_n_o is high, it indicates a current successful CRC.
crc_valid_o ^[6]	output	1	CRC check status indicator, active-high.
Status Interface			
hard_err_o	output	1	Hard error indicator; high indicates that a hard error has occurred in the link, and it sets to 1'b0

Port Name	I/O	Data Width	Description
			until the IP is reset.
soft_err_o ^[3]	output	1	Soft error indicator; high indicates that the current RX link has a soft error.
frame_err_o ^[3]	output	1	Frame error indicator; High, indicates a current frame structure error. Note! This port is only available when the Interface option on the GUI is set to "Framing".
channel_up_o	output	1	Channel linking status indicator, active-high; high indicates successful linking of the channel.
lane_up_o	output	$[(m^{[7]}-1):0]$	Lane linking status indicator, active-high; high indicates successful linking of the corresponding lane.
Sidebands Interface			
rx_aligned_o ^{[3][9]}	output	1	Indicates completion of lane initialization for the RX channel
rx_bonded_o ^{[3][9]}	output	1	Indicates completion of channel bonding alignment for the RX channel
rx_verify_o ^{[3][9]}	output	1	Indicates completion of validation for the RX channel
rx_reset_o ^{[3][9]}	output	1	Indicates the RX channel requires resetting from the transmitting end for reinitialization
tx_aligned_i ^{[2][9]}	input	1	Typically directly connects to the rx_aligned_o of the partner
tx_bonded_i ^{[2][9]}	input	1	Typically directly connects to the rx_bonded_o of the partner
tx_verify_i ^{[2][9]}	input	1	Typically directly connects to the rx_verify_o of the partner
tx_reset_i ^{[2][9]}	input	1	Typically directly connects to the rx_reset_o of the partner
User-side SerDes-related Control Interface			
gt_reset_i	input	1	SerDes channel reset signal, active-high; reset all lanes for the IP at the same time.
gt_pll_ok_o	output	1	SerDes PLL lock status; High indicates clock lock.
gt_pcs_tx_clk_o ^[2]	output	$[(m^{[7]}-1):0]$	PCS layer clock in the TX, with each lane corresponding to a 1-bit clock.
gt_pcs_tx_reset_i ^[2]	input	1	SerDes PCS layer TX reset, active-high; reset all lanes for the IP at the same time.
gt_pcs_rx_reset_i ^[3]	input	1	SerDes PCS layer RX reset, active-high; reset all lanes for the IP at the same time.
gt_rx_align_link_o ^[3]	output	$[(m^{[7]}-1):0]$	Alignment status of the SerDes channel; high indicates normal link alignment, with each lane corresponding to 1 bit of valid data.
gt_rx_pma_lock_o ^[3]	output	$[(m^{[7]}-1):0]$	PMA layer lock status of the SerDes channel; high indicates normal link, with each lane corresponding to 1 bit of valid data.
gt_pcs_rx_clk_o ^[3]	output	$[(m^{[7]}-1):0]$	PCS layer clock in the RX, with each lane corresponding to a 1-bit clock.

Port Name	I/O	Data Width	Description
gt_rx_k_lock_o ^[3]	output	$[(m^{[7]}-1):0]$	SerDes RX K character synchronization indicator; high indicates normal RX K character synchronization, with each lane corresponding to 1 bit of valid data.
Dynamic Configuration Interface			
user_drp_clk_o ^[10]	output	1	DRP interface clock
user_drp_addr_i ^[10]	input	24	DRP operation address, synchronized to user_drp_clk_o.
user_drp_wren_i ^[10]	input	1	DRP write operation enable, synchronized to user_drp_clk_o, active-high; high indicates a DRP write operation.
user_drp_wrdata_i ^[10]	input	32	DRP write data, synchronized to user_drp_clk_o.
user_drp_strb_i ^[10]	input	8	DRP write byte enable signal, synchronized to user_drp_clk_o, active-high. It should be set to 8'hff during write operation.
user_drp_rden_i ^[10]	input	1	DRP read operation enable, synchronized to user_drp_clk_o, active-high; high indicates a DRP read operation.
user_drp_ready_o ^[10]	output	1	DRP write operation completion indication, synchronized to user_drp_clk_o, active-high; high indicates that the write operation is complete.
user_drp_rdvld_o ^[10]	output	1	DRP read return data valid indication, synchronized to user_drp_clk_o, active-high; high indicates read data is valid.
user_drp_rddata_o ^[10]	output	32	DRP read data, synchronized to user_drp_clk_o.
user_drp_resp_o ^[10]	output	1	Reserved
SerDes Hard-core Interface			
SerDes_*	—	—	The signal with the beginning of SerDes_ is the connection signal of RoraLink 8B10B IP with SerDes hardcore; users may not need to pay attention; EDA tools will automatically complete the connections.

Note!

- ^[1]In the table, n represents the number of lanes multiplied by the number of bytes in the option Data Width Per Lane on the GUI. For example, if the number of lanes is 2 and the option Data Width Per Lane is set to "4" bytes, then $n = 2 * 4 = 8$.
- ^[2]When "Dataflow Mode" is set to "RX-only Simplex" on the GUI, the IP does not have this port.
- ^[3]When "Dataflow Mode" is set to "TX-only Simplex" on the GUI, the IP does not have this port.
- ^[4]When "Flow Control" is set to "None" or "UFC" on the GUI, the IP does not have this port.
- ^[5]When "Flow Control" is set to "None", "Immediate NFC" or "Completion NFC" on the GUI, the IP does not have this port.
- ^[6]When "CRC" is not checked on the GUI, the IP does not have this port.
- ^[7]m in the table means the number of lanes.
- ^[8]Bus data supports both big-endian and little-endian modes. If the GUI option "Little Endian Support" is checked, the signal is defined in little-endian mode as [N:0]. If the GUI option is unchecked, it is defined in big-endian mode as [0:N].

- ^[9]When "Bank Channel" is set to "Sidebands" on the GUI, the IP has this port.
- ^[10]When "DRP Ports" is not checked on the GUI, the IP does not have this port.

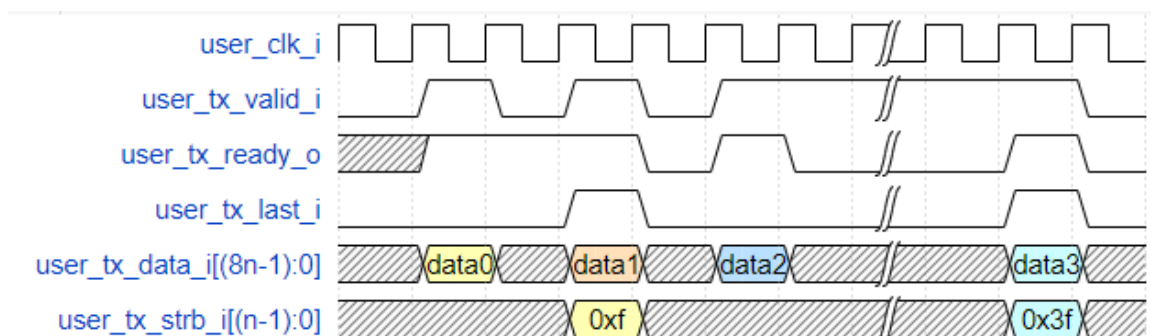
3.6 User Interface Timing

3.6.1 User Data TX Interface Timing Diagram

Gowin RoraLink 8B10B IP provides a user data transmission interface for transmitting frame data or stream data.

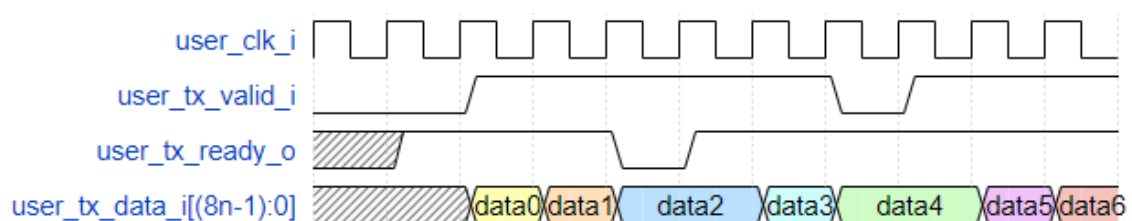
Frame data uses a 2-byte SCP (/K28.2/K27.7/) as the start of frame and a 2-byte ECP (/K29.7/K30.7/) as the end of frame. When there is no data transmission, the IP will automatically insert inter-frame sequences. If the length of the transmitted data frame is not an even number of bytes, the IP will insert padding characters at the end of the frame. Frame data TX interface timing is illustrated in Figure 3-4; `user_tx_data_i` is used to transmit data blocks. The data is valid when both `user_tx_valid_i` and `user_tx_ready_o` are high. The `user_tx_last_i` signal indicates the end of frame data, and `user_tx_strb_i` is only valid when `user_tx_last_i`, `user_tx_valid_i`, and `user_tx_ready_o` are all high. `user_tx_strb_i` represents the byte enable for the frame tail. The frame start, frame end and inter-frame gap are inserted to the frame data within the IP. If the CRC option is selected on the GUI, IP internally adds the CRC field to the end of the frame.

Figure 3-4 Frame Data TX Interface Timing Diagram



In the case of stream data transmission, there are no frame delimiters, making the transmission simple and resource-efficient. The timing diagram for the data TX interface is illustrated in Figure 3-5. `user_tx_data_i` is used to transmit data blocks. Data is valid when both `user_tx_valid_i` and `user_tx_ready_o` are high.

Figure 3-5 Stream Data TX Interface Timing Diagram

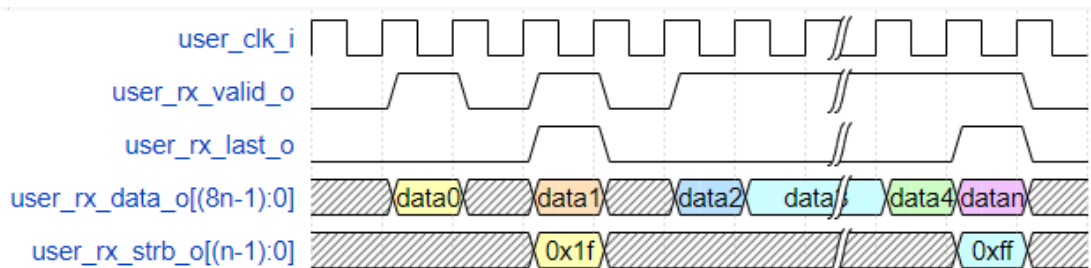


3.6.2 User Data RX Interface Timing Diagram

Gowin RoraLink 8B10B IP provides a user data RX interface for transmitting frame data or stream data. After receiving data, the IP processes control characters in the data and transmits the remaining data to the user through the RX interface. If flow control is required when receiving data in the application, it can be managed through the UFC or NFC interfaces.

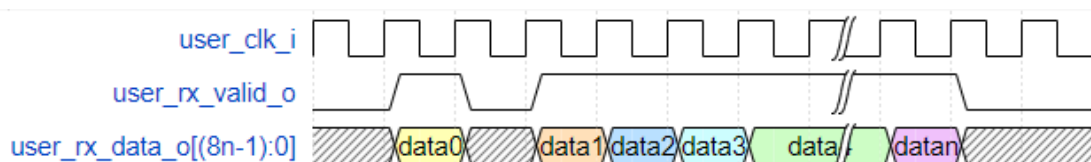
The timing diagram for the frame data RX interface is shown in Figure 3-6. `user_rx_data_o` is used to transmit data blocks. Data is valid when `user_rx_valid_o` is high. `user_rx_last_o` indicates the end of the frame data. `user_rx_strb_o` is valid only when both `user_rx_last_o` and `user_rx_valid_o` are high, and it represents the byte enable for the frame tail.

Figure 3-6 Frame Data RX Interface Timing Diagram



The timing diagram for the stream data RX interface is as shown in Figure 3-7. `user_rx_data_o` is used to transmit data blocks. Data is valid when `user_rx_valid_o` is high.

Figure 3-7 Stream Data RX Interface Timing Diagram



3.6.3 NFC Interface Timing Diagram

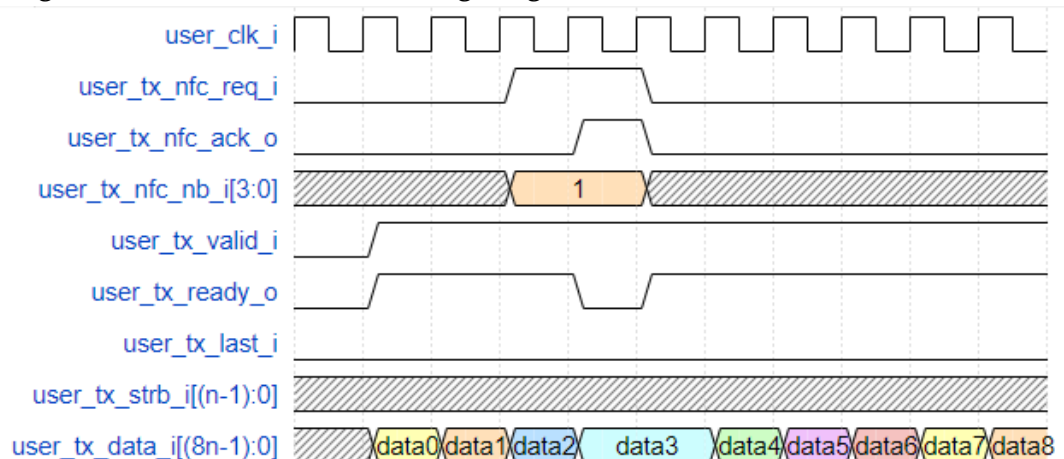
Gowin RoraLink 8B10B IP provides an NFC interface, which allows the receiver to send NFC request messages to the transmitter. This is used to control the data rate at the receiver end to prevent FIFO overflow.

The NFC data description is as shown in Table 3-2. The value of `user_tx_nfc_nb_i` corresponds to the number of requested pause intervals sent by the partner. Here, "XON" indicates normal data transmission on the link, while "XOFF" indicates continuous transmission of interval codes without sending data.

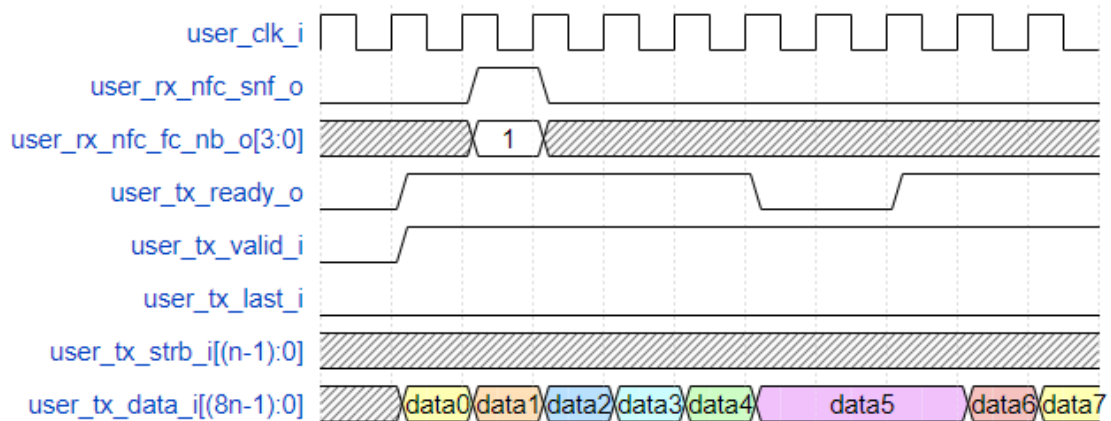
Table 3-2 NFC Data Description

user_tx_nfc_nb_i	Pause Interval
4'b0000	0 (XON)
4'b0001	2
4'b0010	4
4'b0011	8
4'b0100	16
4'b0101	32
4'b0110	64
4'b0111	128
4'b1000	256
4'b1001~4'b1110	Reserved
4'b1111	XOFF

The timing diagram for NFC TX interface is as shown in Figure 3-8. The user_tx_nfc_nb_i data is valid when both user_tx_nfc_req_i and user_tx_nfc_ack_o are high. Simultaneously, user_tx_ready_o is pulled low for one clock cycle to transfer NFC data.

Figure 3-8 NFC TX Interface Timing Diagram

The timing diagram for NFC RX interface is as shown in Figure 3-9. Upon receiving NFC messages from the partner, the IP will pull down user_tx_ready_o for the corresponding clock cycles to transmit pause intervals.

Figure 3-9 NFC RX Interface Timing Diagram

3.6.4 UFC Interface Timing Diagram

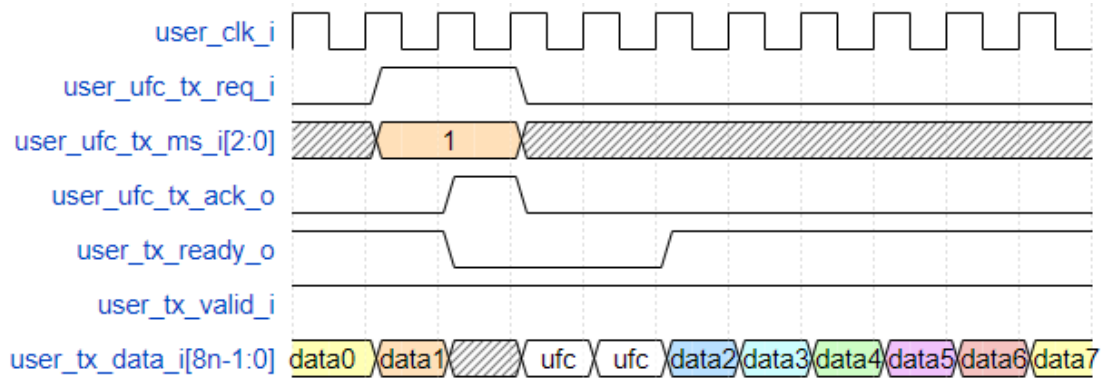
Gowin RoraLink 8B10B IP provides a UFC mode flow control interface, which includes TX and RX.

The UFC data description is as shown in Table 3-3. The value of **user_ufc_tx_ms_i** corresponds to the size of the UFC message.

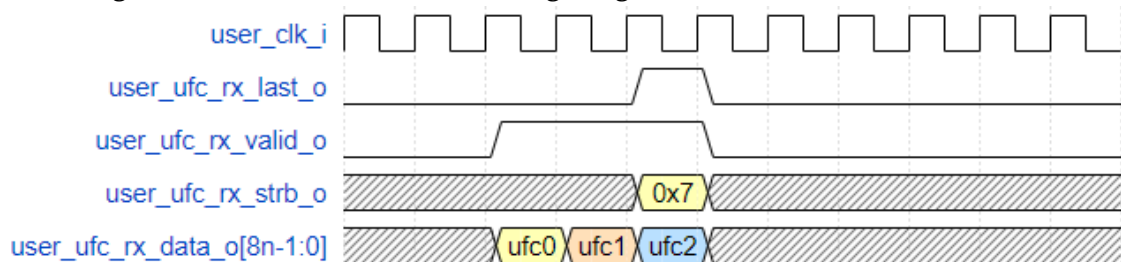
Table 3-3 UFC Data Description

user_ufc_tx_ms_i	UFC Message Size (Bytes)
3'b000	2
3'b001	4
3'b010	6
3'b011	8
3'b100	10
3'b101	12
3'b110	14
3'b0111	16

The timing diagram for the UFC TX interface is shown in Figure 3-10. The **user_ufc_tx_req_i** signal is set to high to initiate a UFC TX request. The **user_ufc_tx_ms_i** signal indicates the size of the UFC message and is valid when both **user_ufc_tx_req_i** and **user_ufc_tx_ack_o** are high. The **user_tx_data_i** signal begins transmitting UFC data in the clock cycle following the one when **user_ufc_tx_ack_o** goes high. UFC data must be transmitted continuously without interruption, and the length of the UFC data corresponds to the UFC message size indicated by **user_ufc_tx_ms_i**.

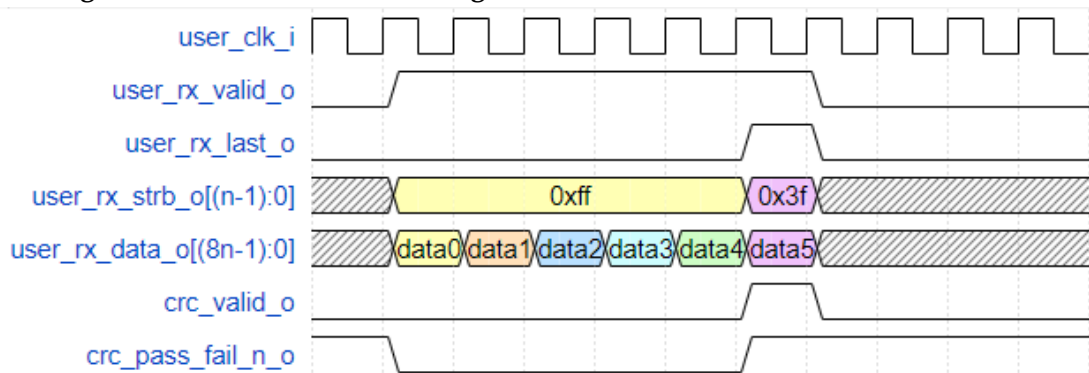
Figure 3-10 UFC TX Interface Timing Diagram

The timing diagram for the UFC RX interface is shown in Figure 3-11. When `user_ufc_rx_valid_o` is high, the `user_ufc_rx_data_o` is valid. `user_ufc_rx_strb_o` corresponds to the byte enable of the data in `user_ufc_rx_data_o`, and `user_ufc_rx_last_o` being high indicates the end of the UFC data frame.

Figure 3-11 UFC RX Interface Timing Diagram

3.6.5 CRC Interface Timing Diagram

Gowin RoraLink 8B10B IP provides a CRC interface that indicates CRC check. As shown in Figure 3-12, in the CRC check timing diagram, `crc_valid_o` is asserted high for one clock cycle at the end of the data frame. When `crc_valid_o` is high, the `crc_pass_fail_n_o` signal is valid. A high level on `crc_pass_fail_n_o` indicates a successful CRC check, while a low level indicates a CRC check error.

Figure 3-12 CRC Interface Timing

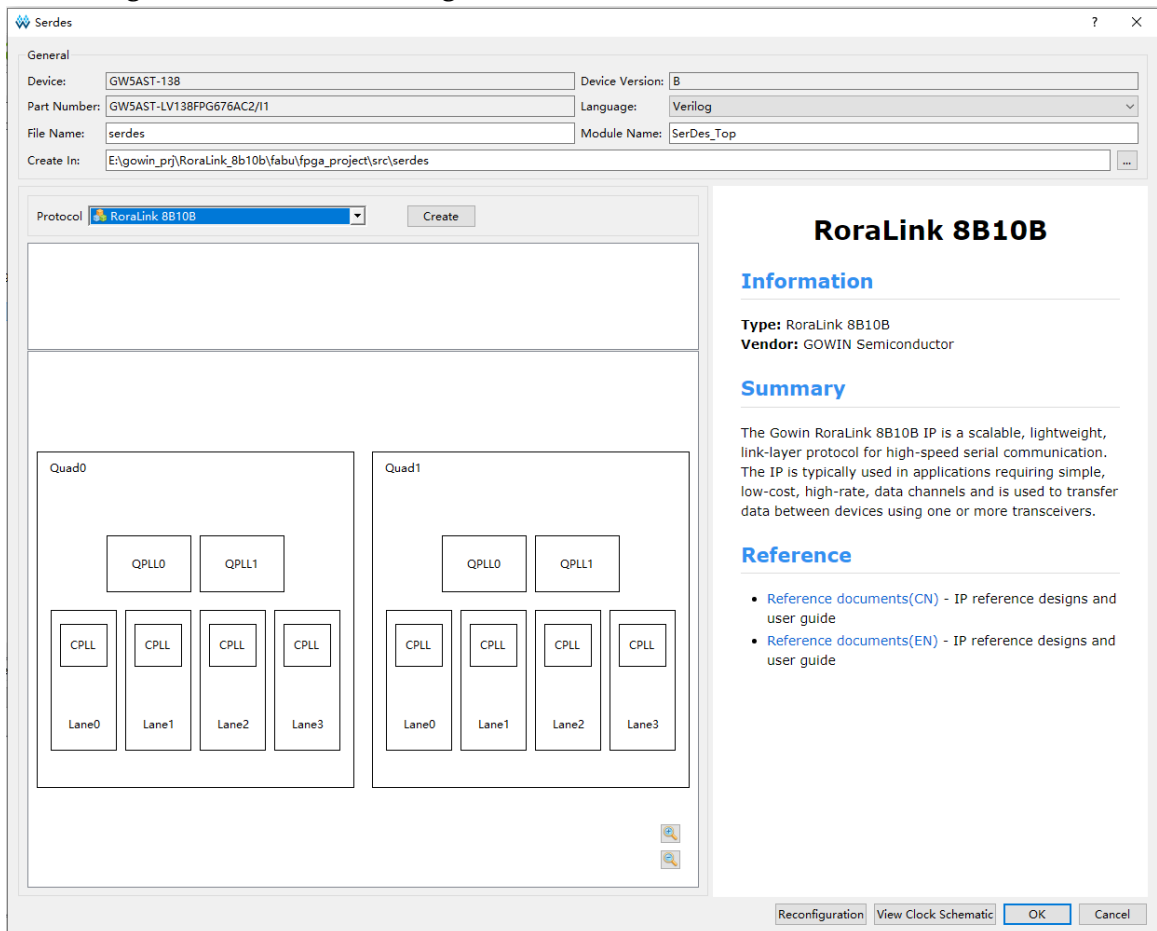
4 Interface Configuration

You can call and configure Gowin RoraLink 8B10B IP using the IP core generator tool in the IDE.

1. Open SerDes IP

After creating the project, click the "Tools" tab in the upper left interface, click "IP Core Generator" from the drop-down list to open Gowin IP Core Generator. Then find SerDes under the Soft IP Core directory, and double-click to open SerDes IP.

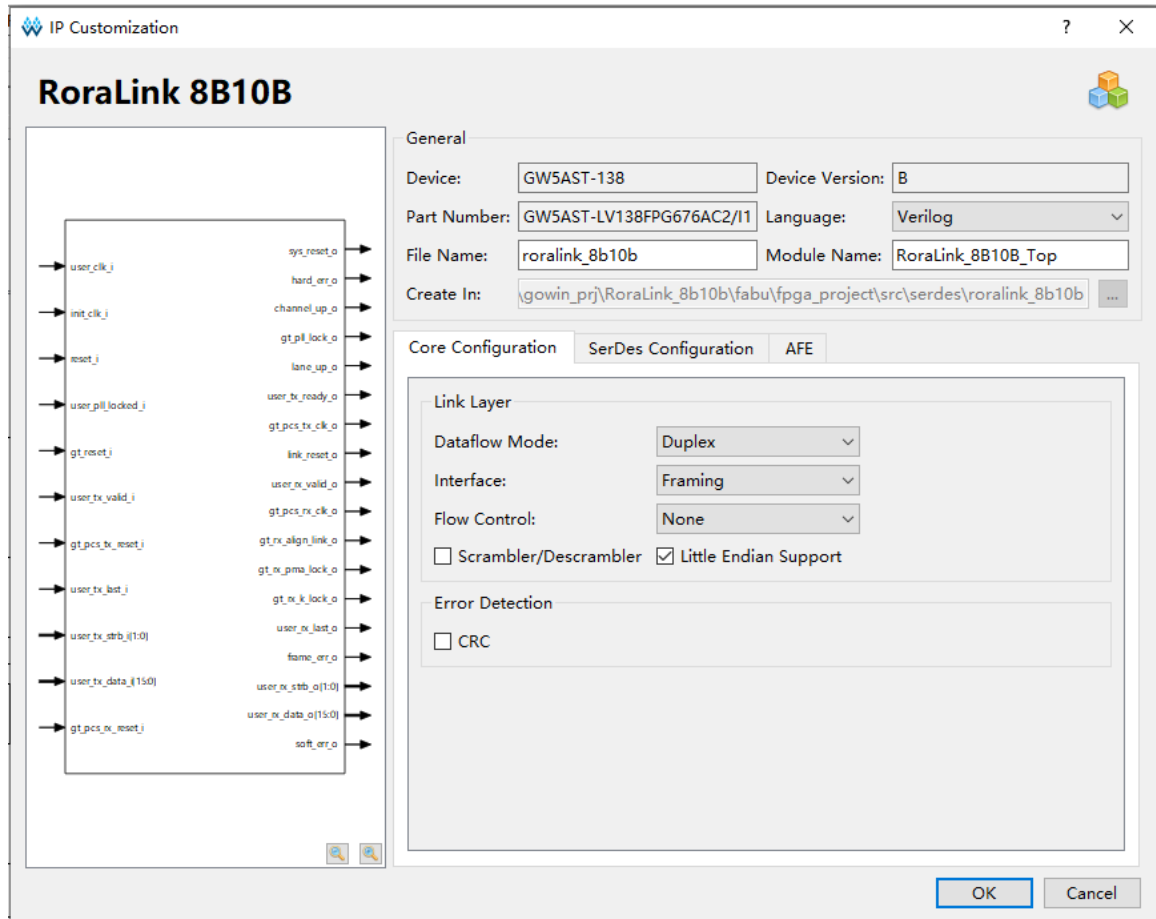
Figure 4-1 SerDes IP Configuration Interface



2. Open RoraLink 8B10B IP core.

After opening SerDes IP, find RoraLink 8B10B in the "Protocol" drop-down list and click "Create" to open the RoraLink 8B10B IP protocol configuration interface.

Figure 4-2 Gowin RoraLink 8B10B IP Configuration Interface



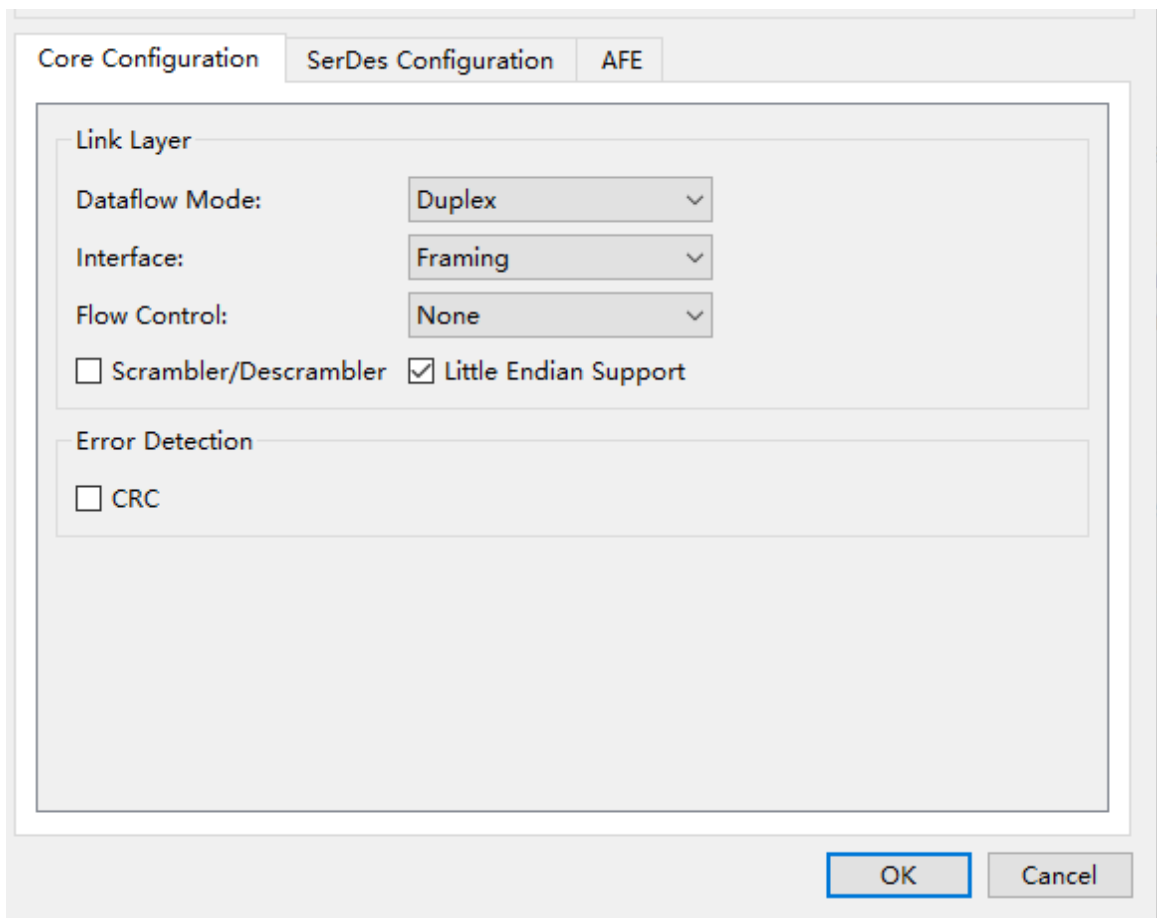
3. Configure RoraLink 8B10B IP protocol.

Gowin RoraLink 8B10B IP configuration interface includes "Core Configuration", "SerDes Configuration", and "AFE", as shown in Figure 4-3, Figure 4-4, and Figure 4-5. In the "Core Configuration" tab, the user can select the link layer-related parameters. In the "SerDes Configuration" tab, the user can select the SerDes-related parameters. In the "AFE" tab, the user can select the SerDes analog parameters. The descriptions of parameters are shown in Table 4-1. After configuring the RoraLink 8B10B IP parameters, click the "OK" button to generate the configuration for the RoraLink 8B10B IP protocol.

4. Complete SerDes IP configuration

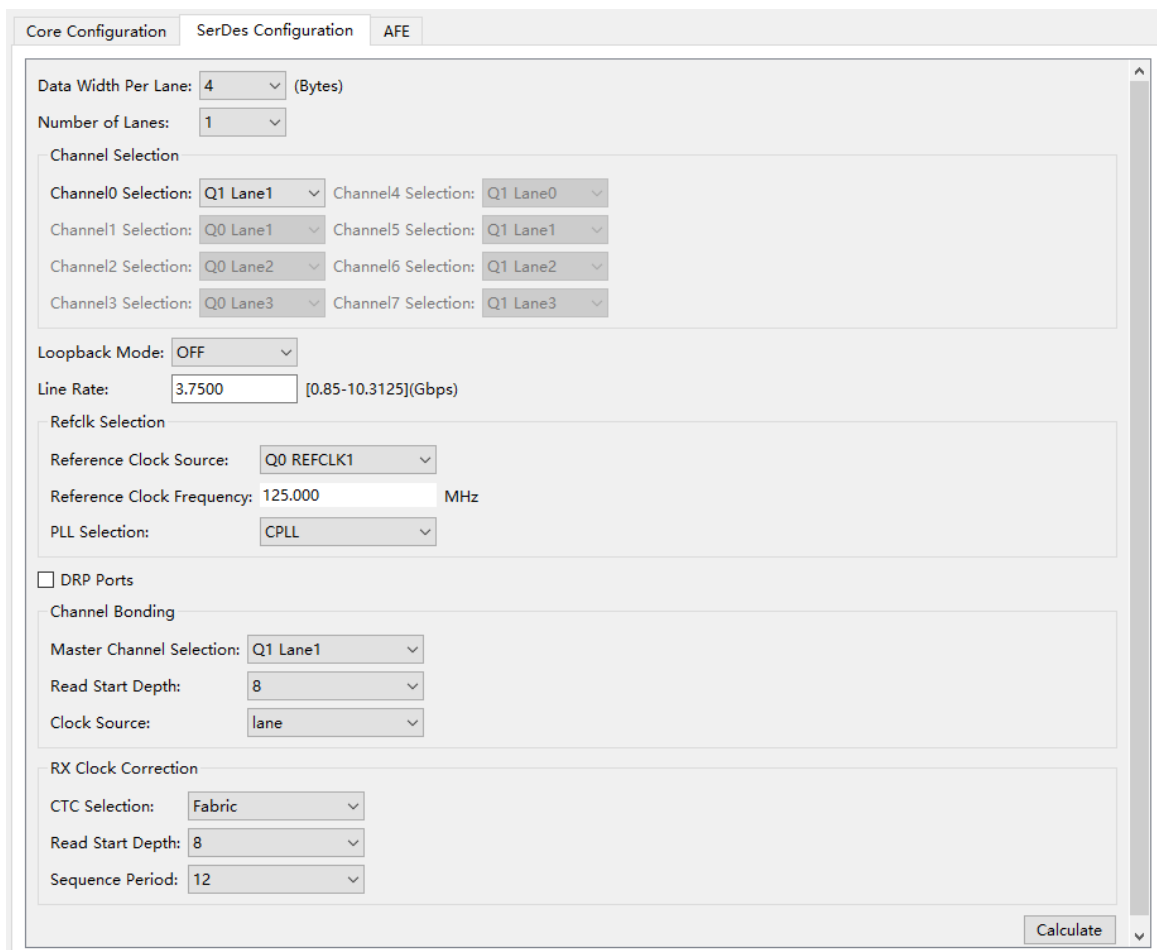
On the SerDes IP interface, the user completes the configuration of all protocols and then clicks the "OK" button to generate the SerDes IP. In the top-level SerDes IP file, signals with the prefix RoraLink_8B10B_Top_ are the signals related to the RoraLink 8B10B IP.

Figure 4-3 IP Configuration Interface



The image shows a software configuration window titled "IP Configuration Interface". It has three tabs at the top: "Core Configuration" (which is selected), "SerDes Configuration", and "AFE". The main content area is divided into two sections. The first section, "Link Layer", contains four settings: "Dataflow Mode" set to "Duplex", "Interface" set to "Framing", "Flow Control" set to "None", and two checkboxes: "Scrambler/Descrambler" (unchecked) and "Little Endian Support" (checked). The second section, "Error Detection", contains a single checkbox for "CRC" which is unchecked. At the bottom right of the window are "OK" and "Cancel" buttons.

Tab	Section	Parameter	Value
Core Configuration	Link Layer	Dataflow Mode	Duplex
		Interface	Framing
		Flow Control	None
		Scrambler/Descrambler	☐
	Error Detection	Little Endian Support	☒
CRC		☐	
SerDes Configuration			
AFE			

Figure 4-4 SerDes Configuration Interface

The image shows a software configuration window for SerDes. It has three tabs: 'Core Configuration', 'SerDes Configuration' (which is active), and 'AFE'. The 'SerDes Configuration' tab contains several sections of settings:

- Data Width Per Lane:** A dropdown menu set to '4' with '(Bytes)' next to it.
- Number of Lanes:** A dropdown menu set to '1'.
- Channel Selection:** A section with eight dropdown menus for Channel0 through Channel7. Channel0 and Channel4 are set to 'Q1 Lane1'. Channel1, Channel5, Channel2, Channel6, Channel3, and Channel7 are all set to 'Q0 Lane1'.
- Loopback Mode:** A dropdown menu set to 'OFF'.
- Line Rate:** A text input field containing '3.7500' and a range '[0.85-10.3125](Gbps)' to its right.
- Refclk Selection:**
 - Reference Clock Source:** A dropdown menu set to 'Q0 REFCLK1'.
 - Reference Clock Frequency:** A text input field containing '125.000' followed by 'MHz'.
 - PLL Selection:** A dropdown menu set to 'CPLL'.
- DRP Ports:** A checkbox that is currently unchecked.
- Channel Bonding:**
 - Master Channel Selection:** A dropdown menu set to 'Q1 Lane1'.
 - Read Start Depth:** A dropdown menu set to '8'.
 - Clock Source:** A dropdown menu set to 'lane'.
- RX Clock Correction:**
 - CTC Selection:** A dropdown menu set to 'Fabric'.
 - Read Start Depth:** A dropdown menu set to '8'.
 - Sequence Period:** A dropdown menu set to '12'.

A 'Calculate' button is located at the bottom right of the configuration area.

Figure 4-5 AFE Configuration Interface

The screenshot shows the 'AFE' configuration tab in a software interface. It is divided into two main sections: TX (Transmit) and RX (Receive).

TX Section:

- Differential Swing: 900mV (dropdown)
- FFE Mode:
 - FFE Mode: Auto (dropdown)
 - Cm: 0 (range 0~19)
 - C0: 40 (range 21~40)
 - C1: 0 (range 0~19)

RX Section:

- SD Threshold: 100mV (dropdown)
- Equalization:
 - Equalization Mode: Auto (dropdown)
 - ATT: 7 (range 0~10)
 - BOOST: 9 (range 0~15)
 - BIAS: 7 (range 0~15)

At the bottom right, there are 'OK' and 'Cancel' buttons.

Table 4-1 Gowin RoraLink 8B10B IP Parameters

Name	Range	Default	Description
Core Configuration			
Dataflow Mode	Duplex, RX-only Simplex, TX-only Simplex	Duplex	Select duplex mode or simplex mode
Interface	Framing, Streaming	Framing	Select frame data or stream data.
Flow Control	None, UFC, Immediate NFC, Completion NFC, UFC+Immediate NFC, UFC+Completion NFC	None	Select the flow control mode
Back Channel	Sidebands, Timer	Sidebands	Valid only when "Dataflow Mode" is set to "RX-only Simplex" or "TX-only Simplex" on the GUI. It is used to initialize the relevant signals in simplex

Name	Range	Default	Description
			mode, using either dedicated sideband signals or an internal timer. If Sidebands is selected, dedicated sideband signals are used for initialization. If Sidebands is selected, dedicated sideband signals are used for initialization.
Scrambler/Descrambler	Check/Uncheck	Unchecked	Choose whether to scramble the data. If checked, data scrambling and descrambling will be performed; if unchecked, data will not be scrambled or descrambled.
Little Endian Support	Check/Uncheck	Check	The interface is in little-endian mode or big-endian mode. If checked, it is in little-endian mode; if unchecked, it is in big-endian mode.
CRC	Check/Uncheck	Unchecked	Whether the IP performs CRC processing. CRC is added in the user data transmission direction and removed with CRC check in the user data reception direction. If checked, CRC is enabled; if unchecked, CRC is disabled.
SerDes Configuration			
Data Width Per Lane	2, 4	2	Select the data width per Lane of the IP as either 16 bits or 32 bits.
Number of Lanes	1,2,3,4,5,6,7,8	1	Select the number of lanes for the IP
Channel0 Selection	Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2, Q1 Lane3,	Q0 Lane0	Selection of the SerDes channel for the first Lane of the IP. Q0 and Q1 correspond to two Quads of SerDes Lane0, Lane1, Lane2, and Lane3 indicate the 4 Lane numbers for each Quad of SerDes. Note! The number of lanes available on the GUI is associated with the option "Lane Width".
Channel1 Selection	Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2, Q1 Lane3,	Q0 Lane1	Selection of the SerDes channel for the second Lane of the IP. Q0 and Q1 correspond to two Quads of SerDes Lane0, Lane1, Lane2, and Lane3 indicate the 4 Lane numbers for each Quad of SerDes.
Channel2 Selection	Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2, Q1 Lane3,	Q0 Lane2	Selection of the SerDes channel for the third Lane of the IP. Q0 and Q1 correspond to two Quads of SerDes Lane0, Lane1, Lane2, and Lane3 indicate the 4 Lane numbers for each Quad of SerDes.
Channel3 Selection	Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1,	Q0 Lane3	Selection of the SerDes channel for the fourth Lane of the IP. Q0 and Q1 correspond to two Quads of SerDes

Name	Range	Default	Description
	Q1 Lane2, Q1 Lane3,		Lane0, Lane1, Lane2, and Lane3 indicate the 4 Lane numbers for each Quad of SerDes.
Channel4 Selection	Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2, Q1 Lane3,	Q1 Lane0	Selection of the SerDes channel for the fifth Lane of the IP. Q0 and Q1 correspond to two Quads of SerDes Lane0, Lane1, Lane2, and Lane3 indicate the 4 Lane numbers for each Quad of SerDes.
Channel5 Selection	Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2, Q1 Lane3,	Q1 Lane1	Selection of the SerDes channel for the sixth Lane of the IP. Q0 and Q1 correspond to two Quads of SerDes Lane0, Lane1, Lane2, and Lane3 indicate the 4 Lane numbers for each Quad of SerDes.
Channel6 Selection	Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2, Q1 Lane3,	Q1 Lane2	Selection of the SerDes channel for the seventh Lane of the IP. Q0 and Q1 correspond to two Quads of SerDes Lane0, Lane1, Lane2, and Lane3 indicate the 4 Lane numbers for each Quad of SerDes.
Channel7 Selection	Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2, Q1 Lane3,	Q1 Lane3	Selection of the SerDes channel for the eighth Lane of the IP. Q0 and Q1 correspond to two Quads of SerDes Lane0, Lane1, Lane2, and Lane3 indicate the 4 Lane numbers for each Quad of SerDes.
Loopback Mode	OFF, LB_NES, LB_FES, LB_ENC	OFF	Serdes Loopback Selection: ● OFF indicates Normal mode; SerDes data is transmitted and received normally. ● LB_NES (Loopback Near-End SerDes), SerDes internal loopback; data is looped back to from the near-end PMA to the near-end PMA. ● LB_ENC (Loopback Near-End PCS), SerDes internal loopback; data is looped back to the near-end PCS to the near-end PCS. ● LB_FES, SerDes external loopback; data is looped back to TX from RX of SerDes.
Line Rate	User input	3.1250Gbps	User inputs the required SerDes line rate. When PLL is selected as QPLL0 or CPLL, the theoretical operating line rate range of SerDes is 0.85G~12.5G. When PLL is selected as QPLL1, the theoretical operating line rate range of SerDes is 0.95G~12.5G. However, the final achievable performance depends on the project timing. If CRC is selected, or if a larger number of lanes

Name	Range	Default	Description
			are chosen (larger data width), the maximum achievable speed may be reduced due to timing violation issues.
Reference Clock Source	- For devices GW5AST-138/GW5AT-138/GW5AT-75 Q0 REFCLK0, Q0 REFCLK1, Q1 REFCLK 0, Q1 REFCLK 1 - For devices GW5AT-60 Q0 REFCLK0, Q0 REFCLK1, Q0 REFCLK2, Q0 REFCLK3, SERDES Q0CLKIN0, SERDES Q0CLKIN1, SERDES Q0CLKIN2, SERDES Q0CLKIN3	Q0 REFCLK0	- For devices GW5AST-138/GW5AT-138/GW5AT-75: The reference clock selection for high-speed transceivers is as follows: Q0/Q1 corresponds to the two Quads of SerDes. REFCLK0 and REFCLK1 correspond to the two input reference clocks for each SerDes Quad. Users can select the input reference clock according to their application needs. - For devices GW5AT-60: The reference clock selection for high-speed transceivers is as follows: Q0REFCLK0, Q0REFCLK1, Q0REFCLK2, and Q0REFCLK3 correspond to the four input reference clocks for Quad0. SERDES Q0CLKIN0, SERDES Q0CLKIN1, SERDES Q0CLKIN2, and SERDES Q0CLKIN3 correspond to the input reference clocks for dedicated GPIO pins. The selectable input reference clocks vary depending on the chip package.
Reference Clock Frequency	User input	125M	The reference clock frequency for high-speed transceivers. The GUI interface will automatically calculate a set of recommended reference clock frequencies based on the input Line Rate in the dropdown list. Users can either customize the frequency or choose one of the frequencies generated by the GUI. Clicking the "Calculate" button allows users to confirm the correctness of the frequency.
PLL Selection	QPLL0, QPLL1, CPLL	CPLL	PLL selection
DRP Ports	Check/Uncheck	Unchecked	If checked, DRP enabled. If unchecked, DRP disabled.
Channel Bonding			
Master Channel Selection	Selected Lane	First selected Lane	Select the master channel for receiving Channel Bonding
Read Start Depth	3~28	8	Configure the read start depth of this module after data bonding
Clock Source	Quad, lane	quad	Select the clock source for channel bonding
RX Clock Correction			
CTC Selection	SerDes, Fabric	SerDes	Select Clock Correction module SerDes: Uses the SerDes hard

Name	Range	Default	Description
			core for clock correction ● Fabric: Uses the soft core on the Fabric side for clock correction
Read Start Depth	3~28	8	Configure the read start depth of this module after data adjustment
Sequence Period	4~31	11	Set the interval for transmitting Clock Correction codes in the protocol
AFE (Analog Front End)			
Differential Swing	100mV~900mV	900mV	Configure the swing of the differential signal V_{diffpp} , where $V_{diffpp} = 2 \times V_{diff}$
FFE Mode	Auto, Manual	Auto	Configure TX FFE mode Auto: Auto mode Manual: Manual mode
Cm	0~19	0	Transmit FFE pre-cursor
C0	21~40	40	Transmit FFE main-cursor
C1	0~19	0	Transmit FFE post-cursor
SD Threshold	25mV~200mV	100mV	SD threshold for RX differential signal
Equalization Mode	Auto, Manual	Auto	Auto: Auto mode Manual: Manual mode
ATT	0~10	7	Adjust the RX intermediate-frequency attenuation; a smaller value indicates greater attenuation.
BOOST	0~15	9	Adjust the RX high-frequency amplification; a larger value indicates greater gain.
BIAS	0~15	7	Configure SerDes amplification parameters for RX signals; The higher the configuration, the stronger the signal amplification.

5 Reference Design

See the RoraLink 8B10B [reference design](#) for details at Gowinsemi website.

5.1 Typical Applications

The data transmission of RoraLink 8B10B IP can be composed of a single Lane or multiple Lanes, with each Lane corresponding to a SerDes channel. Data transmission can be either duplex or simplex. As shown in Figure 5-1, it illustrates simplex data transmission with a single Lane. As shown in Figure 5-2, it illustrates simplex data transmission with multiple Lanes. As shown in Figure 5-3, it illustrates simplex data transmission with a single Lane. As shown in Figure 5-4, it illustrates simplex data transmission with multiple Lanes.

Figure 5-1 Simplex Data Transmission with a Single Lane

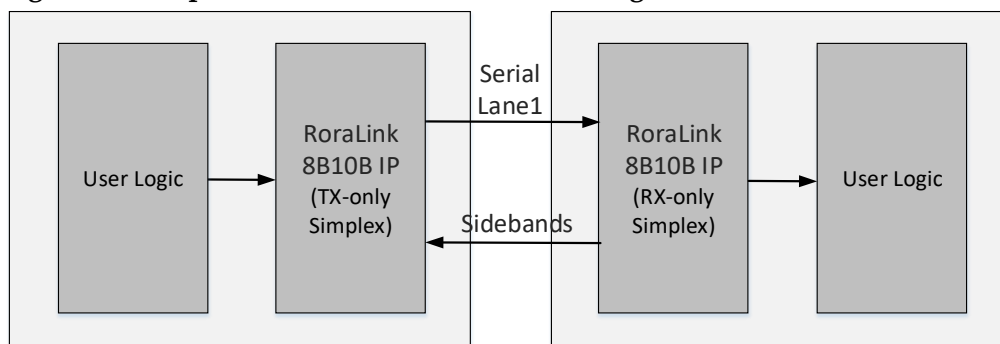


Figure 5-2 Simplex Data Transmission with Multiple Lanes

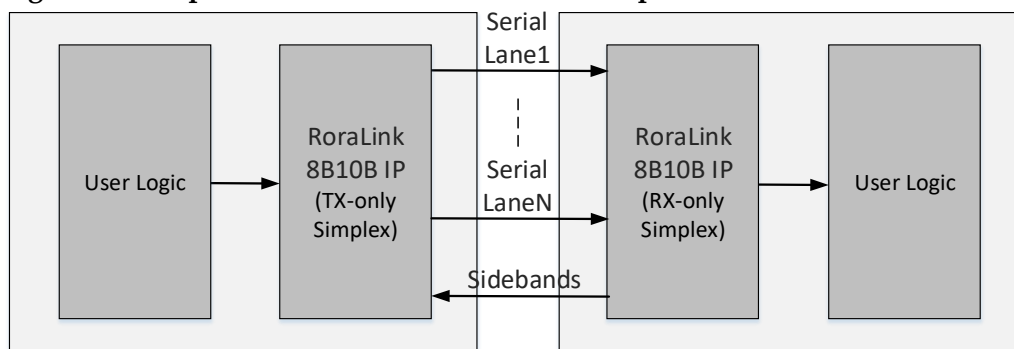
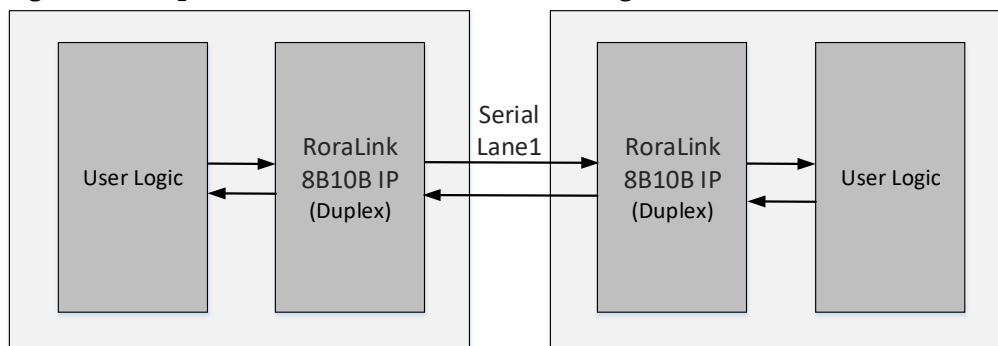
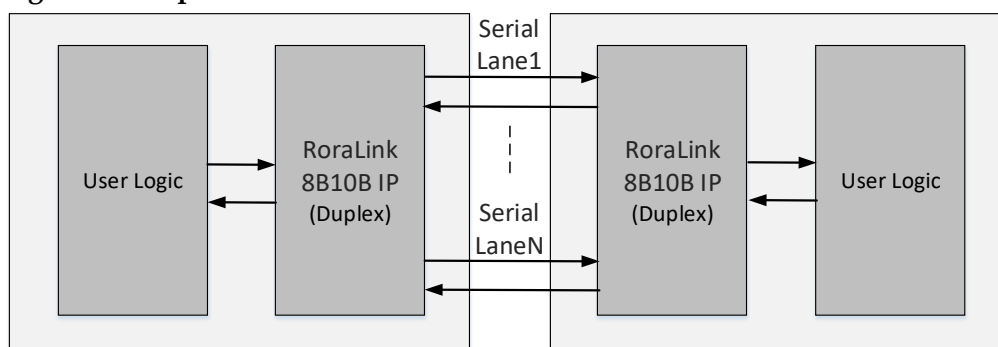


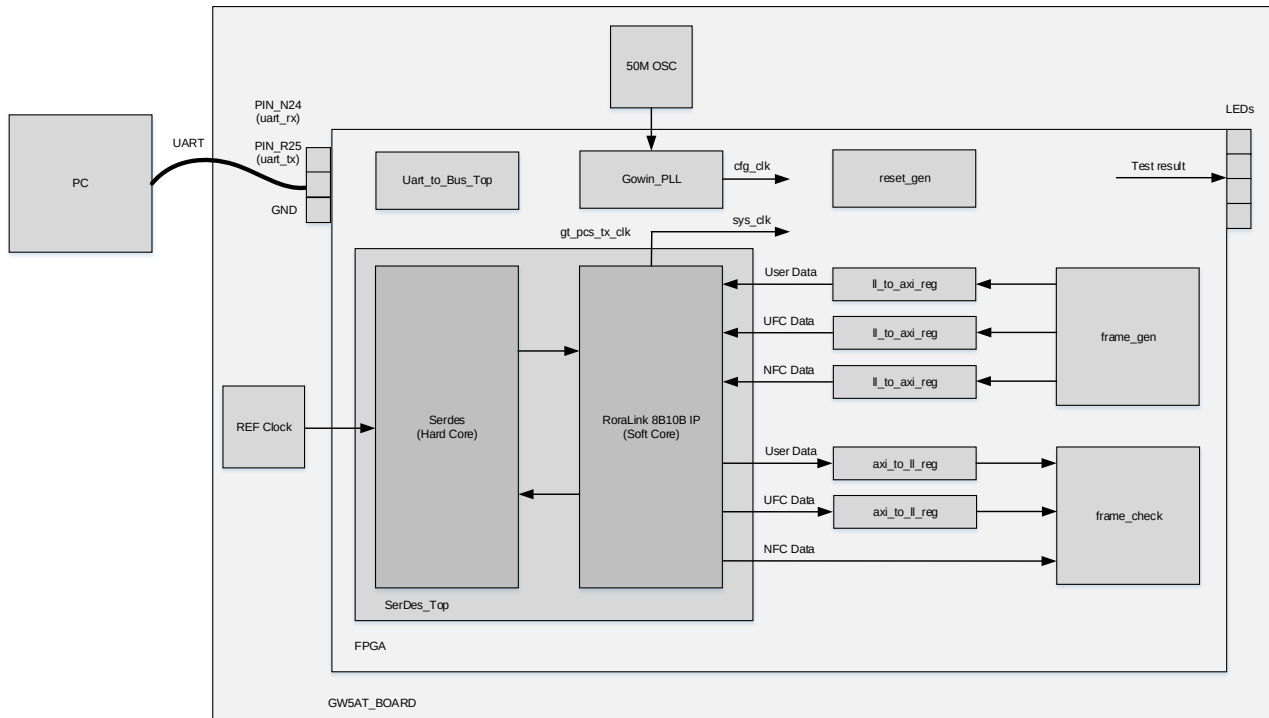
Figure 5-3 Duplex Data Transmission with a Single Lane**Figure 5-4 Duplex Data Transmission with Multi Lanes**

5.2 Gowin RoraLink 8B10B IP Reference Design Project

Gowin RoraLink 8B10B IP reference design contains the SerDes IP module (with the RoraLink 8B10B IP softcore), clock and reset, interface conversion module, frame generation module, frame detection module and debug module.

- `uart_to_bus_top`: Converts UART serial port to internal configuration bus interface in FPGA, easy to read/write registers, and easy to debug single board.
- `gowin_pll`: The on-board internal 50MHz crystal oscillator locks out the operating clock for the configuration module.
- `reset_gen`: Generates the system reset signal.
- `frame_gen`: Frame generation module.
- `frame_check`: Frame detection module.
- `ll_to_axi_reg`: AXI interface conversion module.
- `axi_to_ll_reg`: AXI interface conversion module.
- `Serdes_Top`: Contains SerDes hard core and RoraLink 8B10B IP soft core; Gowin EDA tool will automatically complete the connection between SerDes hard core and RoraLink 8B10B IP; user only needs to pay attention to the interface of SerDes top layer after package.

Figure 5-5 Reference Design Instance Structure Diagram



5.3 Reference Design Board Test

Gowin currently offers a reference design for SerDes internal loopback testing of single RoraLink 8B10B IP, allowing users to quickly become familiar with the interface, timing, and function of RoraLink 8B10B IP without relying on a daughter card.

The steps for reference project board test are as follows:

- Download the project from the website and compile to generate bit file.
- The structure is as shown in Figure 5-5.
- Download fs to single board
- To confirm the test results, there are two methods:

Method 1: Observe the LEDs

- LED0 (PIN_P20): Constantly ON indicates that Gowin_PLL is in a locked state.
- LED1 (PIN_R20): Constantly ON indicates that the internal PLL of SerDes is in a locked state.
- LED2 (PIN_N21): Constantly ON indicates that the IP Channel linking is established successfully.
- LED3 (PIN_N22): Constantly ON indicates that the data received by the IP has passed the verification.

Method 2: Read the register through the serial tool

PC can access the register addresses of the reference design through a serial port tool. When the environment is built, input "R 0" in the serial port tool and the register value is displayed as shown in Figure 5-6. If you

input "W 0 value", the register value corresponding to this value will be written to the register, and if you input "R 0" to reread the register, and the read register value should match the previously written value.

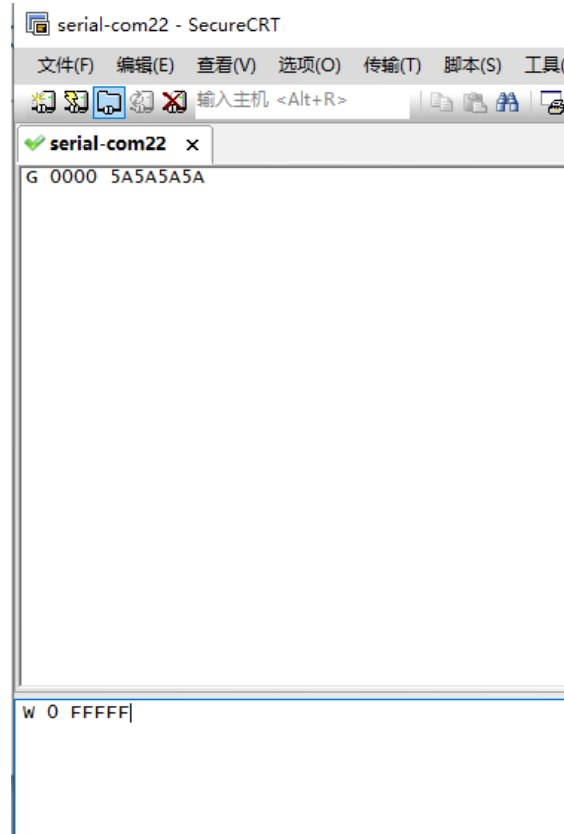
Table 5-1 Reference Design Register List

Address (Word)	Type	Data Width	Signal Name	Description
0x0	RW	[31:0]	test_reg	Test registers, and it can be written and read back, confirming the register read and write function.
0x1	RW	[31:4]	--	Reserved bits
	RW	[3]	reg_rst	IP system reset, active-high
	RW	[2]	gt_pcs_rx_rst	SerDes PCS reset in the RX, active-high
	RW	[1]	gt_pcs_tx_rst	SerDes PCS reset in the TX, active-high
	RW	[0]	gt_reset	SerDes PMA reset, active-high
0x2~0xf	RW	[31:0]	--	Reserved bits
0x10	RO	[24]	gt_rx_k_lock	SerDes K character lock status in the RX; high level indicates normal operation.
	RO	[16]	gt_rx_align_link	SerDes alignment status in the RX; high level indicates normal operation.
	RO	[8]	gt_rx_pma_lock	SerDes PMA lock status in the RX; high level indicates normal operation.
	RO	[1]	cfg_pll_lock	Configure PLL lock status
	RO	[0]	gt_pll_ok	SerDes PLL lock status
0x11	RO	[31:9]	--	Reserved bits
	RO	[8]	lane_up	IP Lane linking status; high indicates successful link establishment
	RO	[3]	channel_up	IP Channel linking status; high indicates successful link establishment
	RO	[2]	frame_err	IP frame error status; high indicates errors
	RO	[1]	soft_err	IP Soft Error status; high indicates errors
	RO	[0]	hard_err	IP Hard Error status; high indicates errors
0x12	RO	[31:24]	frame_count	Receive frame statistics
	RO	[23:16]	--	Reserved bits
	RO	[15:8]	crc_err_count	RX data CRC check error statistics
	RO	[7:0]	err_count	RX data check error statistics
0x13	RO	[31:24]	re_channel_up_count	IP link re-establishment statistics
	RO	[23:16]	hard_err_cnt	IP hard error statistics
	RO	[15:8]	frame_err_count	IP frame error statistics
	RO	[7:0]	soft_err_count	IP soft error statistics

Note!

Register read/write definition:

- RO indicates read-only
- RW indicates read-write

Figure 5-6 Serial Port Tool

6 File Delivery

The delivery file for Gowin RoraLink 8B10B IP includes documentation, design source code, and reference design.

6.1 Documentation

The folder contains the user guide in PDF version.

Table 6-1 Document List

Name	Description
IPUG1190, Gowin RoraLink 8B10B IP User Guide	Gowin RoraLink 8B10B IP User Guide, namely this one

6.2 Design Source Code (Encryption)

The encrypted code file contains Gowin RoraLink 8B10B IP RTL encrypted code which is used for GUI in order to cooperate with Gowin software to generate the IP core required by users.

Table 6-2 Design Source Code List of Gowin RoraLink 8B10B IP

Name	Description
roralink_8b10b.v	The top-level file of the IP core, which provides users with interface information, encrypted.

6.3 Reference Design

The Ref. Design folder contains the netlist file, the user reference design, the constraints file, the top file, and the project folder, etc.

Table 6-3 Gowin RoraLink 8B10B IP RefDesign Folder Content List

Name	Description
top.v	The top module of reference design
top.cst	Project physical constraints file
top.sdc	Project timing constraints file
top.gsc	Project synthesis constraints file
top.gao	Project debugging file
reset_gen.v	Reset generation module
local2reg.v	Bus to register module

Name	Description
apb2local.v	Configure the bus to Register module
ll_to_axi_reg.v	AXI bus conversion module
axi_to_ll_reg.v	AXI bus conversion module
axi_register_slice.v	AXI bus conversion module
frame_gen.v	Data generation module
frame_check.v	Data check module
SerDes	SerDes IP folder, including SerDes related files and roralink_8b10b folder generated by EDA tool
uart_to_bus	Generated UART to Bus IP files, used to convert UART to internal configuration bus
gowin_pll	PLL IP folder, using an external input 50MHz clock as the reference clock, locking out the internal configuration clock

