



Gowin USB 2.0 Mass Storage Controller IP

User Guide

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1 About This Guide

1.1 Purpose

The purpose of Gowin USB 2.0 Mass Storage Controller IP User Guide is to help you to quickly understand the features and usage of Gowin USB 2.0 Mass Storage Controller IP by providing descriptions of the functions, features, ports, timing, configuration, and reference design, etc. The software screenshots and the supported products listed in this manual are based on Gowin Software V1.9.9 Beta-5. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use

1.2 Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at www.gowinsemi.com:

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS821, GW1NS series of FPGA Products Data Sheet](#)
- [DS861, GW1NSR series of FPGA Products Data Sheet](#)
- [DS841, GW1NZ series of FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS971, GW2AN-18X & 9X Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)

- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1118, GW5ART series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
IP	Intellectual Property
USB	Universal Serial Bus
UMS	USB 2.0 Mass Storage
BOT	Bulk-Only Transport
SCSI	Small Computer System Interface
UFI	USB Floppy Interface
CBW	Command Block Wrapper
CSW	Command Status Wrapper

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

USB Mass Storage (UMS) is a type of device that exchanges data with storage media by sending SCSI commands.

Gowin USB 2.0 Mass Storage Controller IP is based on the USB 2.0 protocol and achieves Bulk-Only Transfer (BOT) data transmission. This IP can use either the default user-defined Flash or W25Q128FV Flash as the storage device. One end of the IP features a parallel data interface that can be connected to the USB Device Controller, and the other end also has a parallel data interface that can be connected to the user-designed Flash.

Table 2-1 Gowin USB 2.0 Mass Storage Controller IP

Gowin USB 2.0 Mass Storage Controller IP	
Logic Resource	See Table 2-2.
Delivered Doc.	
Design Files	Verilog
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9.Beta-5 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.1 Feature

Support default user-defined Flash mode and W25Q128FV Flash mode.

2.2 Resource Utilization

Gowin USB 2.0 Mass Storage Controller IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW2AR-18 series of FPGA as an instance, the resource utilization is as shown in Table 2-2. For the resource utilization of other devices, please refer to later release information.

Table 2-2 Resource Utilization

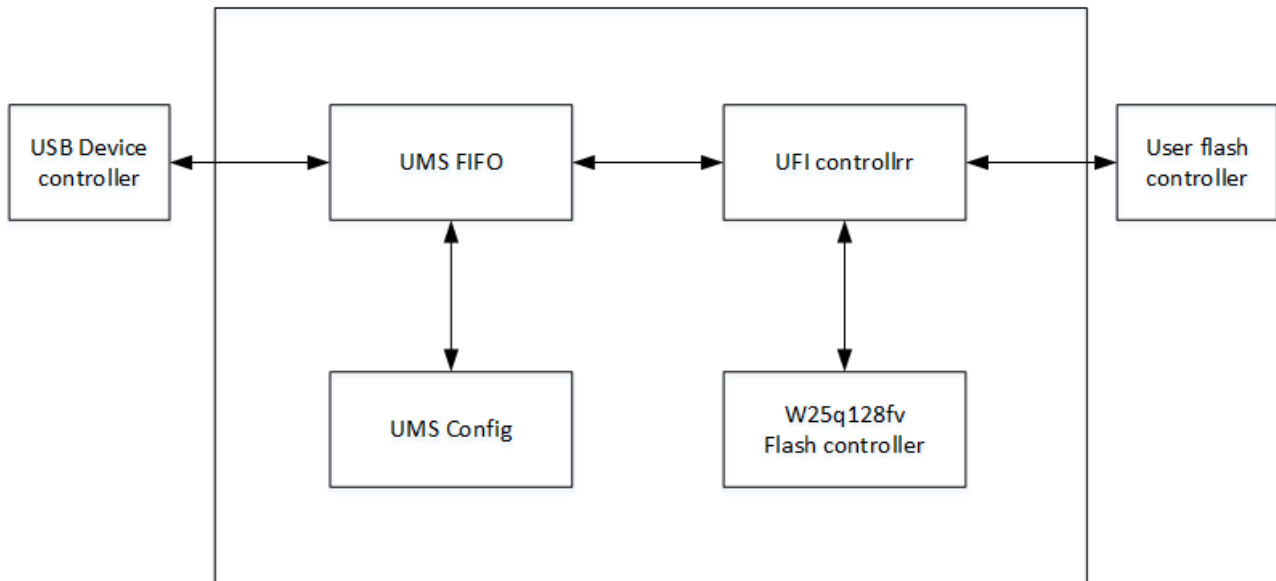
Device	Speed Grade	Resource Name	Resource Utilization
GW2AR-18	-6	LUT	1731
		REG	1132
		ALU	208
		BSRAM	18

3 Functional Description

3.1 USB 2.0 Mass Storage Controller

The USB 2.0 Mass Storage Controller is located between the User Design and the USB Device Controller. It acts as an intermediary between the user design and the USB Device Controller, receiving commands from the USB side to facilitate data transmission between the user side and the USB side. The functional block diagram of USB 2.0 Mass Storage Controller is as shown in Figure 3-1.

Figure 3-1 USB 2.0 Mass Storage Controller Block Diagram



3.2 USB Mass Storage Controller User Flash RX Interface

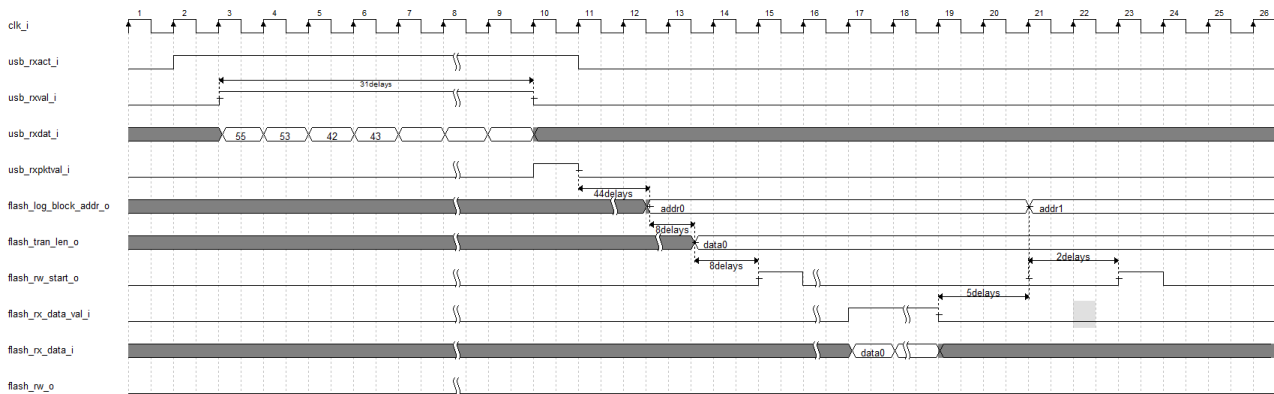
Table 3-1 USB Mass Storage Controller User Flash RX Interface

Name	I/O	Bit Width	Description
flash_rx_data_val_i	Input	1	Receive data valid signal; High indicates that rx_data is valid.
flash_rx_data_i	Input	8	Receive data; the IP receives FLASH read data through this interface.
flash_tran_len_o	Output	16	The number of consecutive logical blocks specified for this data transfer.
flash_log_block_addr_o	Output	32	The start logical block address for this data transfer.
flash_rw_o	Output	1	Read/Write flag High indicates a write operation to FLASH. Low indicates a Read operation to FLASH.
flash_rw_start_o	Output	1	The flag indicating the start of the current logical block read/write operation.

When the Device receives a USB Floppy Interface (UFI) command issued by the Host, it analyzes the Command Block Wrapper (CBW) command packet within that UFI command and performs the output. If the UFI command is a WRITE10 or READ10 command, the Device will output flash_rw_o to indicate the read/write status of the device, and it will also output flash_tran_len_o and flash_log_block_addr_o to indicate the length of output logical blocks and the start logical block address for the read/write operation. The user should check if the Flash data is ready and wait to receive the flash_rw_start_o flag indicating the start of the read/write operation.

When the Device is operating in READ10, the Device receives the flash_rw_start_o start flag and waits for the user to send flash_rx_data_val_i and flash_rx_data_i, the the received data is transferred to the subsequent USB device controller data interface. This transmission continues until the number of logical blocks transferred meets the requirements of the UFI command. At this point, the Device stops receiving flash_rx_data and returns Command Status Wrapper (CSW) to the USB Device Controller regarding the UFI command.

The following diagram shows the timing for device data reception.

Figure 3-2 Data Reception Timing for USB Mass Storage Controller User Flash RX Interface

3.3 USB Mass Storage Controller User Flash TX Interface

Table 3-2 USB Mass Storage Controller User Flash TX Interface

Name	I/O	Bit Width	Description
flash_tx_data_val_o	Output	1	Transmit data valid signal; High indicates that tx_data is valid.
flash_tx_data_o	Output	8	Transmit data; the IP transmits FLASH write data through this port.
flash_write_busy_i	Input	1	Transmit data busy signal; High indicates stop writing data to Flash.
flash_tran_len_o	Output	16	The number of consecutive logical blocks specified for this data transfer.
flash_log_block_addr_o	Output	32	The start logical block address for this data transfer.
flash_rw_o	Output	1	Read/Write flag High indicates a write operation to Flash; low indicates a read operation to Flash.
flash_rw_start_o	Output	1	The flag indicating the start of the current logical block read/write operation.
flash_write_finish_i	Input	1	The flag indicating the completion of the WRITE10 write operation.

When the Device receives a UFI command issued by the Host, it analyzes the CBW command packet within that UFI command and performs the output. If the UFI command is a WRITE10 or READ10 command, the Device will output flash_rw_o to indicate the read/write status of the device, and it will also output flash_tran_len_o and flash_log_block_addr_o to indicate the length of output logical blocks and the start logical block address for the read/write operation. The user should check if the Flash data is ready and wait to receive the flash_rw_start_o flag indicating the start of the read/write operation.

When the Device is operating in WRITE10, it receives the flash_rw_start_o start flag and waits for the USB device controller to send

flash_tx_data, and it then outputs the received data through flash_tx_data_val_o and flash_tx_data_o. During this transmission, if flash_write_busy_i is pulled high, it indicates that the Flash is busy, and the write operation for the logical block will be aborted; until flash_write_busy_i is pulled low, the write operation for the current and subsequent blocks will be re-performed. Once the number of logical blocks to be transferred meets the requirements of the UFI command and the flash_write_finish_i signal is pulled high, the device will stop the write operation and return CSW to the USB Device Controller regarding the UFI command. The following diagram shows the timing diagram for device data transmitting.

Figure 3-3 WRITE10 Command Timing for USB Mass Storage Controller User Flash TX Interface

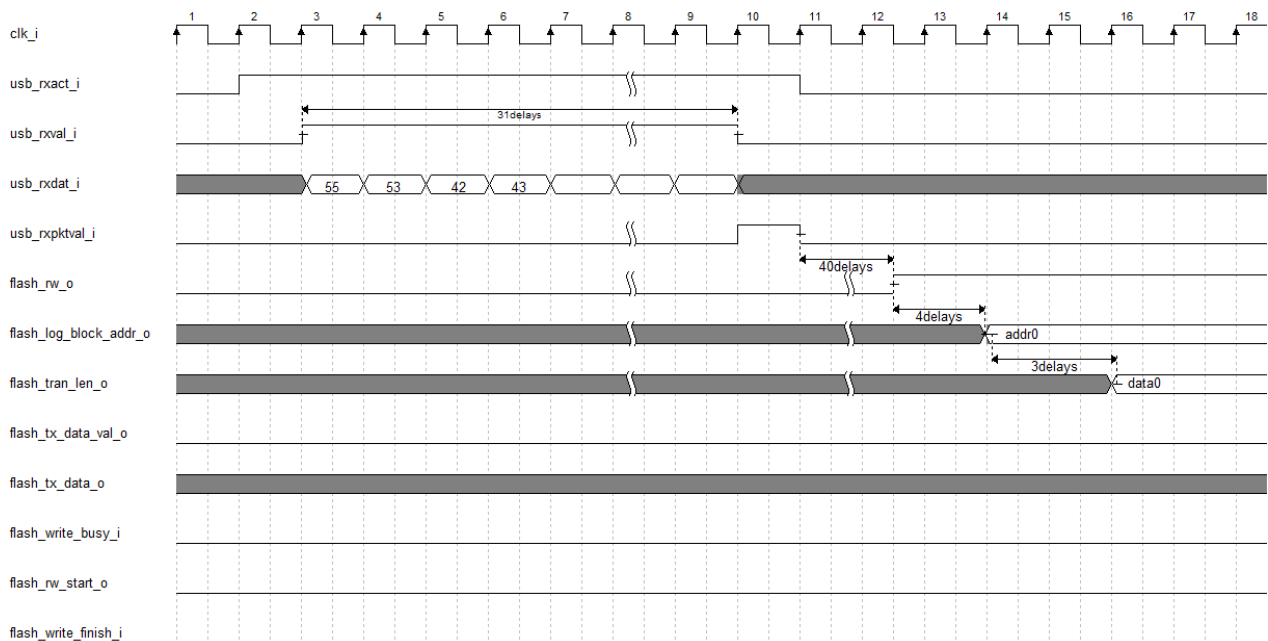
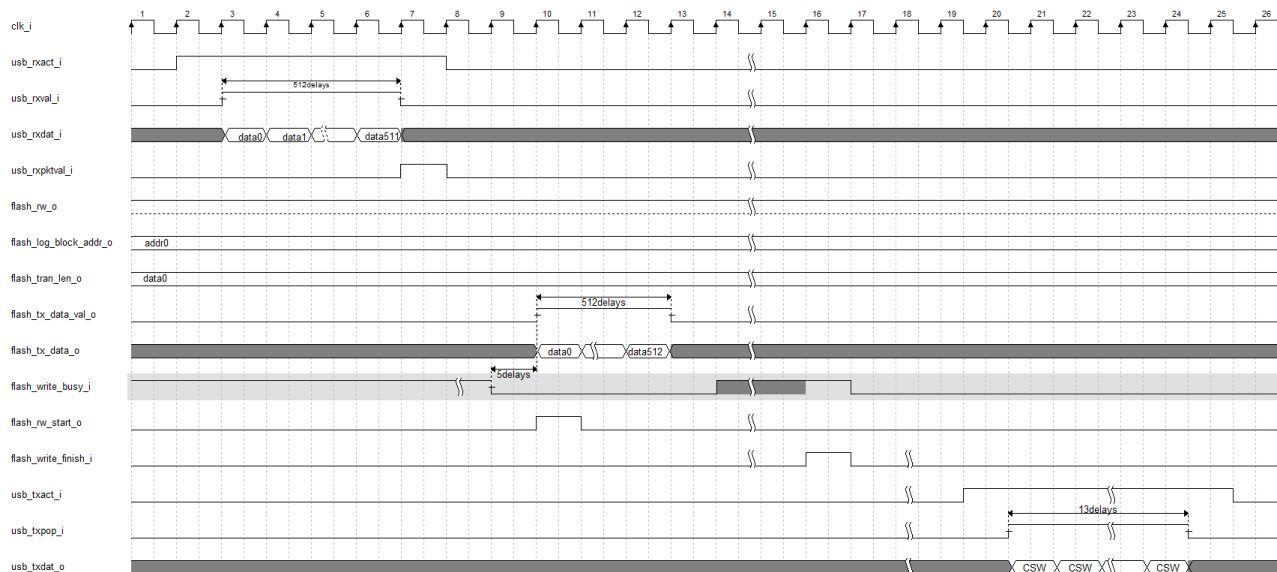


Figure 3-4 Data Transmitting Timing for USB Mass Storage Controller User Flash TX Interface



3.4 USB Mass Storage Controller Control Interface

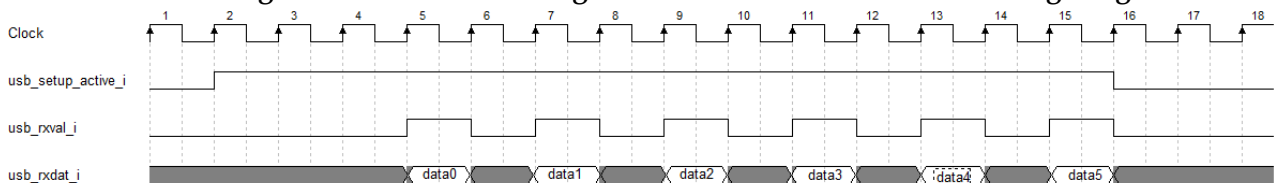
3.4.1 Control Data Interface

Table 3-3 Control Interface

Name	I/O	Bit Width	Description
usb_setup_active_i	Input	1	Data active indicator signal; high indicates that the UMS configuration data is active.
usb_rxval_i	Input	1	Data valid indicator signal; high indicates that the UMS configuration data is valid.
usb_rxdат_i	Input	8	Receive data; IP inputs the data received from the USB interface through this port.

During the USB Mass Storage enumeration, after the completion of standard requests issued by the host, the host will send two special USB class requests, namely Bulk-Only Mass Storage Reset and Get Max LUN. The USB Mass Storage Controller control interface receives configuration requests through usb_setup_active_i, usb_rxval_i, and usb_rxdат_i, and proceeds with subsequent data processing. The following diagram shows the timing diagram for device configuration data reception.

Figure 3-5 USB Mass Storage Controller Control Data RX Timing Diagram



3.4.2 Configuration Data TX Interface

Table 3-4 Configuration Data TX Interface

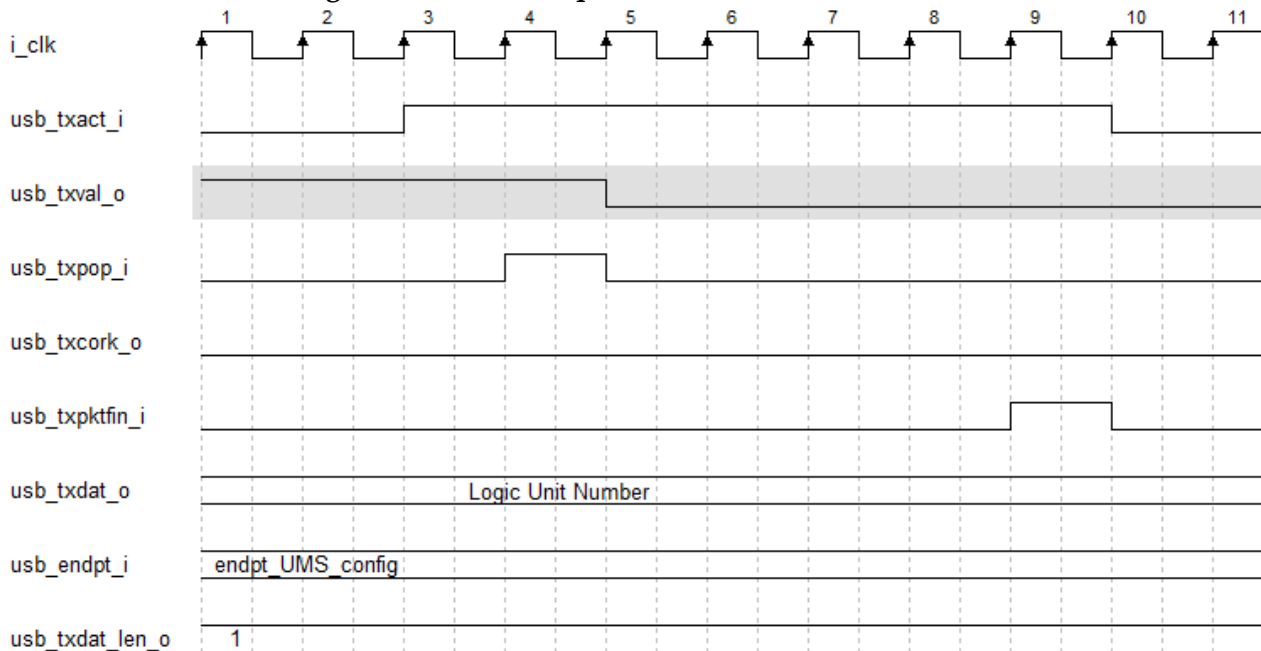
Name	I/O	Bit Width	Description
usb_txact_i	Input	1	Transmit operating signal; high indicates that the device enters data transmitting status.
usb_txval_o	Output	1	Transmit data valid indicator signal; high indicates the user input data is valid.
usb_txpop_i	Input	1	Transmit read signal; high indicates the read of next data.
usb_txdat_o	Output	8	Transmit data; IP transmits this data to the USB interface.
usb_txdat_len_o	Output	12	Transmit data byte count; used to control the number of TX data bytes.
usb_txcork_o	Output	1	Transmit data valid signal; low indicates that TXDAT is insufficient.
usb_endpt_i	Input	4	Endpoint selection indicator signal; it

Name	I/O	Bit Width	Description
			indicates the current communication endpoint of USB.
usb_txpktfin_i	Input	1	Transmit data completion signal; it indicates the completion of this data transmission.

During the USB Mass Storage enumeration, the host issues two specific class requests, that is, Bulk-Only Mass Storage Reset, which involves no data exchange, and Get Max LUN, which reads configuration data from the device. Therefore, only the configuration data TX interface is reserved.

After receiving the Get Max LUN specific class request from the host, in the subsequent Host IN command, the device sends the corresponding configuration data through the TX interface.

Figure 3-6 Data TX Timing for USB Mass Storage Controller Control Endpoint Sending Get Max LUN Request



4 Signal Definition

4.1 Signal Definition

The signal definitions of Gowin USB 2.0 Mass Storage Controller IP are as shown in Table 4-1.

Table 4-1 Signal Definition

No.	Signal Name	I/O	Data Width	Description	Note
1	clk_i	I	1	Receive clock signal from PHY, and it must be 60M.	
2	reset_i	I	1	Asynchronous reset signal	
3	usb_busreset_i	I	1	USB reset indicator signal; high indicates the detection of USB bus reset.	
4	usb_txact_i	I	1	Transmit operating signal; high indicates that the device enters data transmitting status.	
5	usb_txval_o	O	1	Transmit data valid indicator signal; high indicates the user input data is valid (only valid during control endpoint data transmission, otherwise inactive).	
6	usb_txpop_i	I	1	Transmit read signal; high indicates the read of next data.	
7	usb_txdat_o	O	8	Transmit data; IP transmits this data to device controller.	
8	usb_txdat_len_o	O	12	Transmit data byte count; used to control the number of TX data bytes.	
9	usb_txck_o	O	1	Transmit data valid signal; low indicates that TXDAT is insufficient.	
10	usb_txpktfm_i	I	1	Transmit data completion signal; high indicates that the TX data is complete.	
11	usb_setup_active_i	I	1	Configuration data active indicator signal; high indicates that the USB configuration data is active.	

No.	Signal Name	I/O	Data Width	Description	Note
12	usb_rxact_i	I	1	Receiving operating signal; high indicates that the device enters data receiving status.	
13	usb_rxval_i	I	1	Receive data valid signal; High indicates RXDAT is valid.	
14	usb_rxdn_i	I	8	Receive data; IP will receive data from the device controller for subsequent configuration and SCSI command.	
15	usb_rxdy_o	O	1	Receive ready signal; high indicates that it can receive RXDAT.	
16	usb_rxpktval_i	I	1	Data packet valid signal; high indicates that the RX data packets are valid.	
17	usb_endpt_i	I	4	Endpoint selection indicator signal; It indicates the currently selected communication endpoint of USB.	
18	w25_di_i	I	1	W25Q128FV Flash data input	w25q128fv flash mode
19	w25_do_o	O	1	W25Q128FV Flash data output	
20	w25_cs_o	O	1	W25Q128FV Flash chip selected signal	
21	w25_sclk_o	O	1	W25Q128FV Flash clock	
22	flash_rx_data_val_i	I	1	Receive data valid signal; High indicates RXDAT is valid.	User-defined mode
23	flash_rx_data_i	I	8	Receive data; the IP reads the data and transfers it to the host.	
24	flash_tx_data_val_o	O	1	Transmit data valid signal; high indicates TXDAT is valid.	
25	flash_tx_data_o	O	8	Transmit data; the IP transmits the host write data through this port.	
26	flash_write_busy_i	I	1	Transmit busy signal; high indicates that the device is busy. The IP will re-transmit the current logical block data after the busy signal is pulled low.	
27	flash_tran_len_o	O	16	Number of logical blocks in this read/write operation.	
28	flash_log_block_addr_o	O	32	The logical block address in this read/write operation.	
29	flash_rw_o	O	1	Read/write operation indicator: 1: Write 0: Read	
30	flash_rw_start_o	O	1	Read/write operation start flag	
31	flash_write_finish_i	I	1	Write operation completion flag	

4.2 Parameter Configuration Option

The parameter configuration of Gowin USB 2.0 Mass Storage IP is shown in Table 4-2.

Table 4-2 Configuration Options

Options	Description
Flash mode	Flash mode selection, including user-defined mode and w25q128fv flash mode.

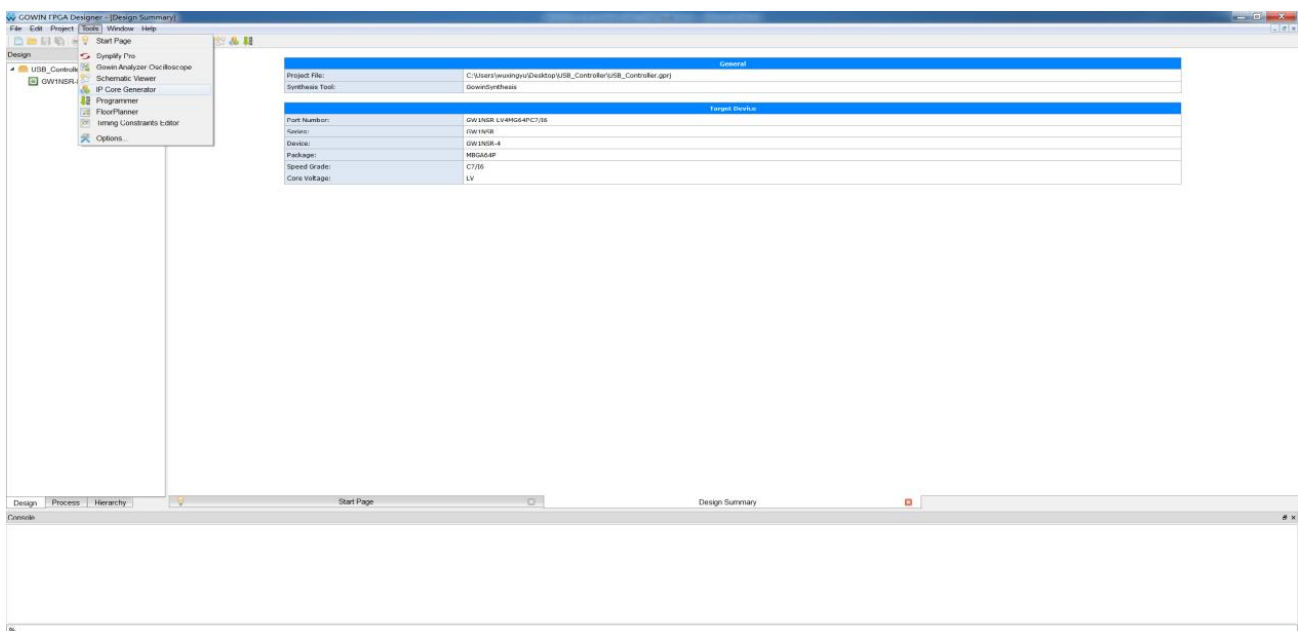
5 Interface Configuration

You can select “Tools” in Gowin Software to start the IP Core Generator to call and configure USB 2.0 Mass Storage IP.

1. Open IP Core Generator.

After creating the project, you can click the “Tools” tab in the upper-left corner, then click the “IP Core Generator” via the drop-down list, as shown in Figure 5-1.

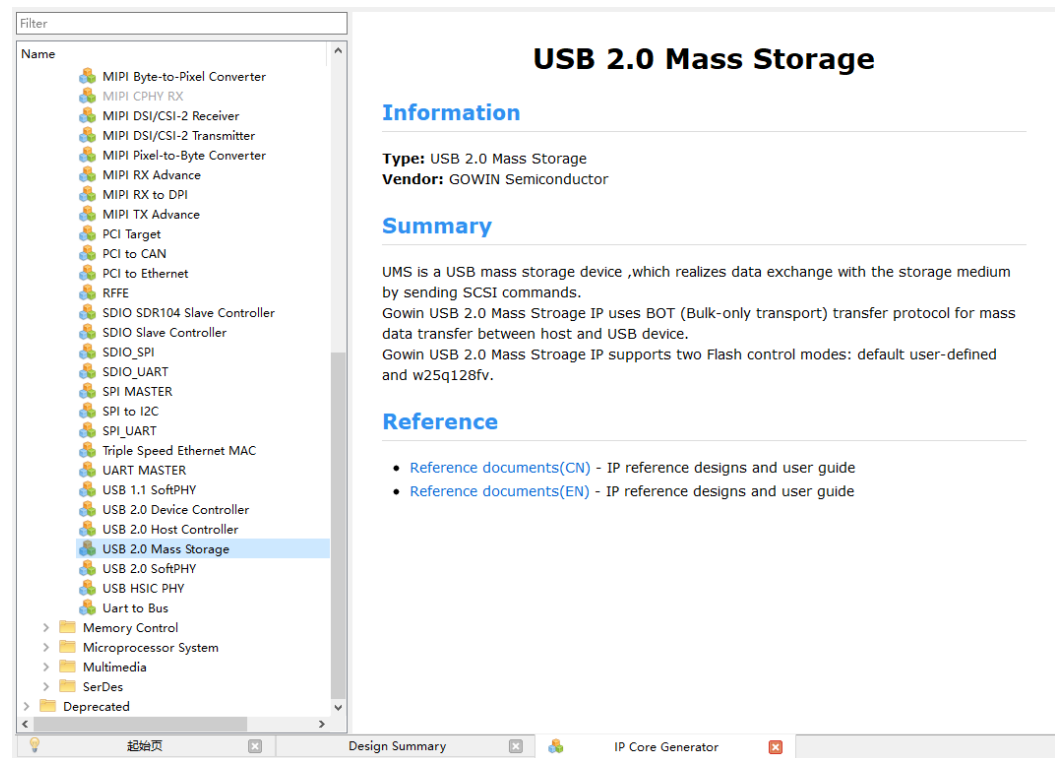
Figure 5-1 IP Core Generator



2. Open USB 2.0 Mass Storage IP Core

Select “Soft IP Core > Interface and Interconnect > USB 2.0 Mass Storage IP”, as shown in Figure 5-2. Double-click to open the configuration interface.

Figure 5-2 USB 2.0 Mass Storage IP Core

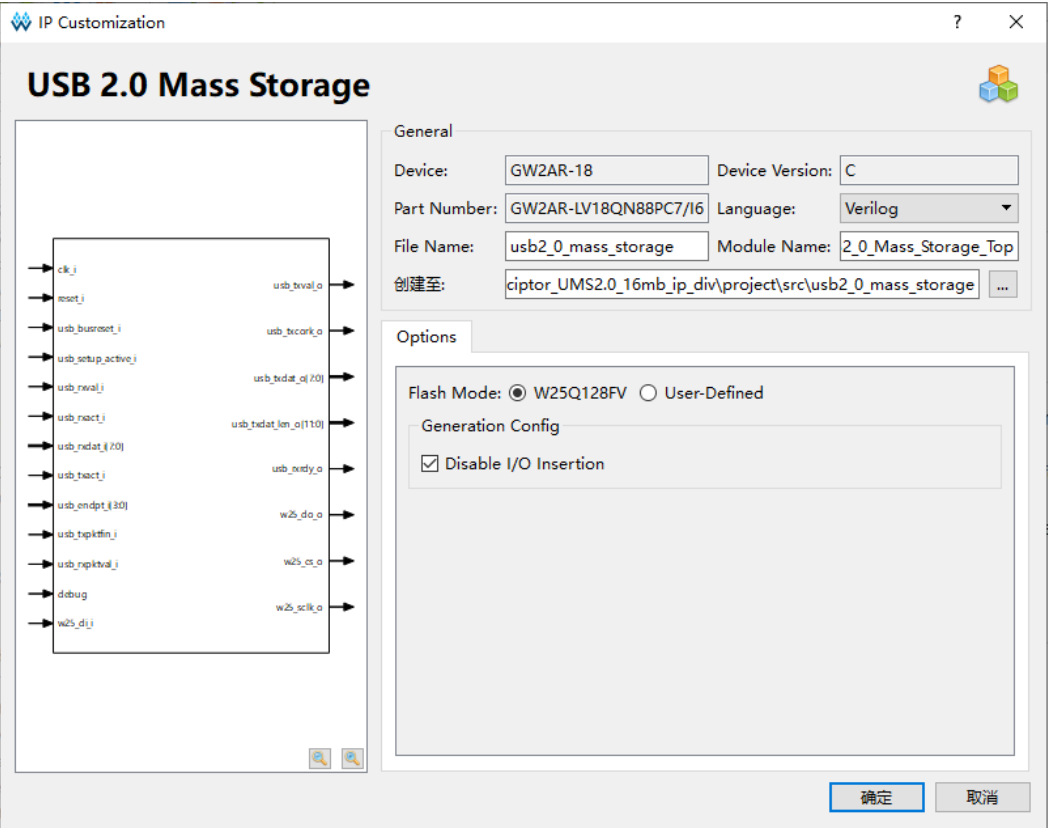


3. USB 2.0 Mass Storage IP Core Configuration Interface

Figure 5-3 shows USB 2.0 Mass Storage IP core configuration interface. The interface diagram is displayed on the left. Options are displayed on the right.

- You can configure the generated file name in “File Name” text box.
- You can configure the generated top module name in “Module Name” text box.
- Click “Options” to configure Flash mode.

Figure 5-3 USB 2.0 Mass Storage IP Configuration Interface

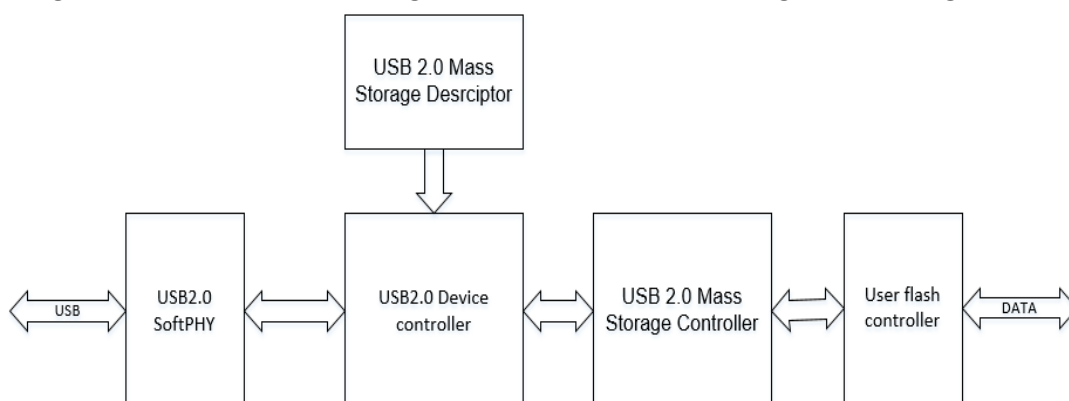


6 Reference Design

6.1 USB Reference Design

This chapter introduces the structure and usage of USB 2.0 Mass Storage Controller IP reference design. This reference design is an instance of a USB mass storage device based on the W25Q128FV Flash. Its basic structure is shown in Figure 6-1.

Figure 6-1 USB 2.0 Mass Storage Controller Reference Design Block Diagram



In this design example, USB signals are converted into parallel UTMI signals by Gowin USB 2.0 SoftPHY IP module, and then USB data packet parsing is completed by USB 2.0 Device Controller. The USB 2.0 Mass Storage Descriptor module contains USB mass storage device descriptor information.

The USB 2.0 Mass Storage Controller module sends configuration commands to the USB Host, processes commands and data from the USB side, and writes/reads data to/from the user-selected Flash.

6.2 USB CDC Driver Installation

You can install the CDC driver on the device through the zadig software as follows.

Open zadig (Administrator rights required) and select List All Devices in the Options drop-down list.

6.3 Data Transfer Testing

After inserting Gowin USB 2.0 Mass Storage, the computer recognizes the device and displays it, as shown in Figure 6-2 and Figure 6-3.

Figure 6-2 Device Manager Recognition for USB 2.0 Mass Storage IP

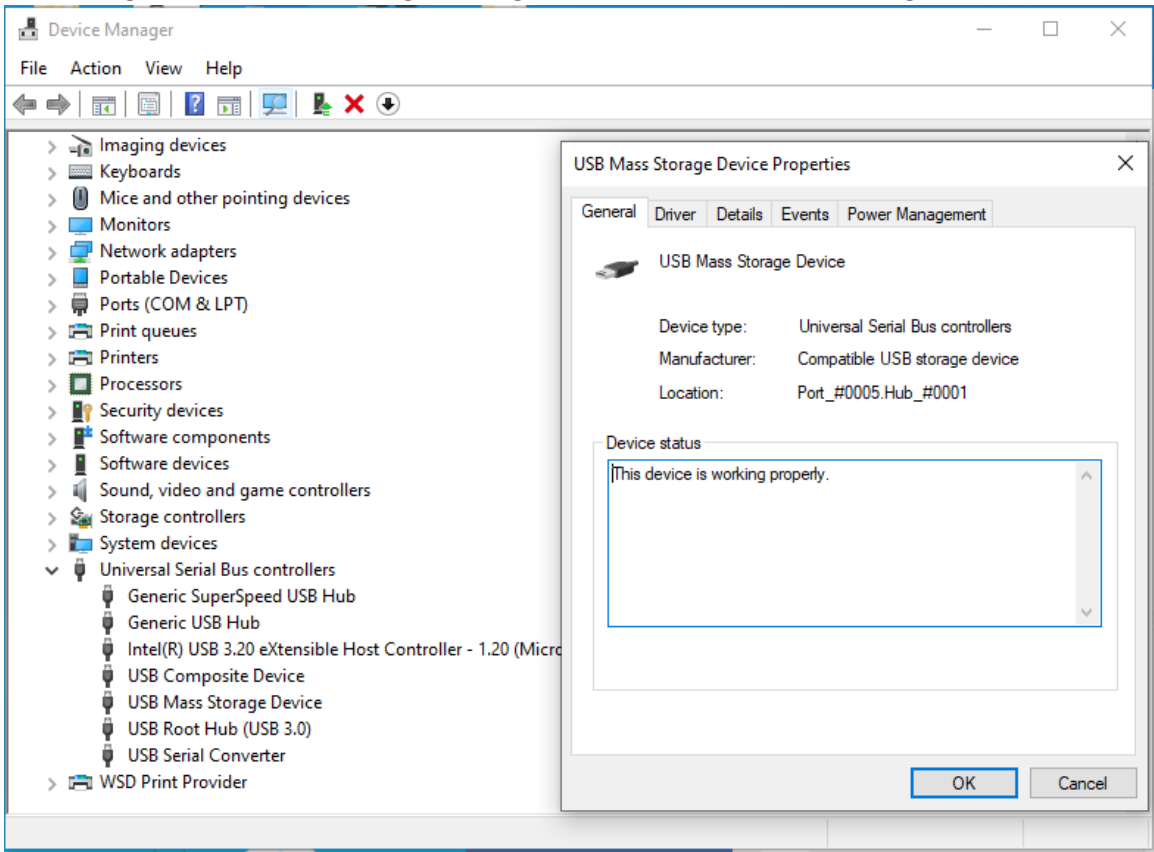
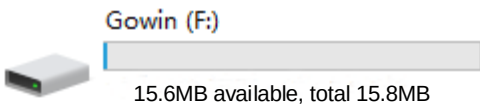


Figure 6-3 My Computer Recognition for USB 2.0 Mass Storage IP



As shown in Figure 6-4, after inserting Gowin USB 2.0 Mass Storage, data can be read from and written to the Flash.

Figure 6-4 Write Data to USB 2.0 Mass Storage IP

