



Gowin Equalizer IP

User Guide

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Revision History

Date	Version	Description
05/09/2024	1.0E	Initial version published.

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1 About This Guide

1.1 Purpose

Gowin Equalizer IP User Guide mainly includes the description of the functions, features, ports, timing, configuration and call, and reference design, etc. It helps users quickly understand the features and usage of Gowin Equalizer IP. The software screenshots and the supported products listed in this manual are based on Gowin Software V1.9.9 Beta-3. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at www.gowinsemi.com:

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS821, GW1NS series of FPGA Products Data Sheet](#)
- [DS881, GW1NSER series of FPGA Products Data Sheet](#)
- [DS861, GW1NSR series of FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS971, GW2AN-18X & 9X Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
ALU	Arithmetic Logical Unit
LUT	Look-up Table
IP	Intellectual Property

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

Gowin Equalizer IP can adjust the intensity of audio signals at various frequencies, thereby altering the overall sound of the audio. Gowin Equalizer IP utilizes second-order IIR filters for audio processing.

Table 2-1 Gowin Equalizer IP

Gowin Equalizer IP	
Logic Resource	See Table 2-2.
Delivered Doc.	
Design Files	Verilog
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9.Beta-3 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.1 Features

- The input data width ranges from 2 to 36 bits
- The coefficient bit width ranges from 2 to 36 bits
- The number of multipliers can be selected as 2 or 5
- Gain can be reloaded
- The number of gains can be selected as 3 or 5
- The frequency band ranges from 10~32

2.2 Max. Frequency

The max. frequency of Gowin Equalizer IP is mainly determined by speed grade of the selected devices.

2.3 Latency

The latency of Gowin equalizer IP is determined by the configuration

parameters.

2.4 Resource Utilization

Gowin Equalizer IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW2A-55 series of FPGA as an instance, the resource utilization is as shown in Table 2-2. For the resource utilization of other devices, please refer to later release information.

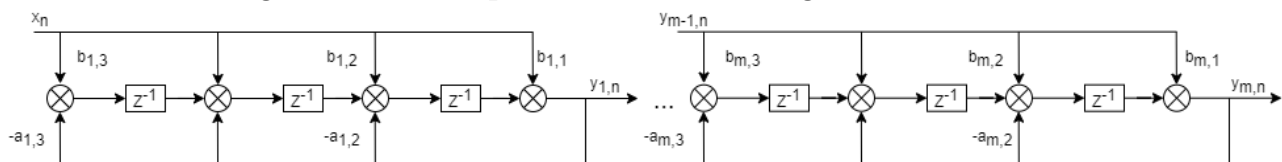
Table 2-2 Resource Utilization

Device	Speed Grade	Resource Name	Resource Utilization
GW2A-55	C8/I7	Registers	8769
		LUTs	5897
		ALUs	326
		I/O Buffer	86

3 Functional Description

To implement an m-band IIR equalizer, m different IIR filters are required; and each filter is adjusted to handle a specific frequency band of the audio signal. These IIR filters are cascaded, allowing the audio signal to pass through each filter sequentially, thereby altering the overall sound of the audio. The figure below shows the basic implementation steps.

Figure 3-1 Gowin Equalizer IP Structure Diagram



4 Port List

The details of Gowin Equalizer IP IO port are shown in Table 4-1, and the port diagram is as shown in Figure 4-1.

Figure 4-1 Gowin Equalizer IP IO Port Diagram

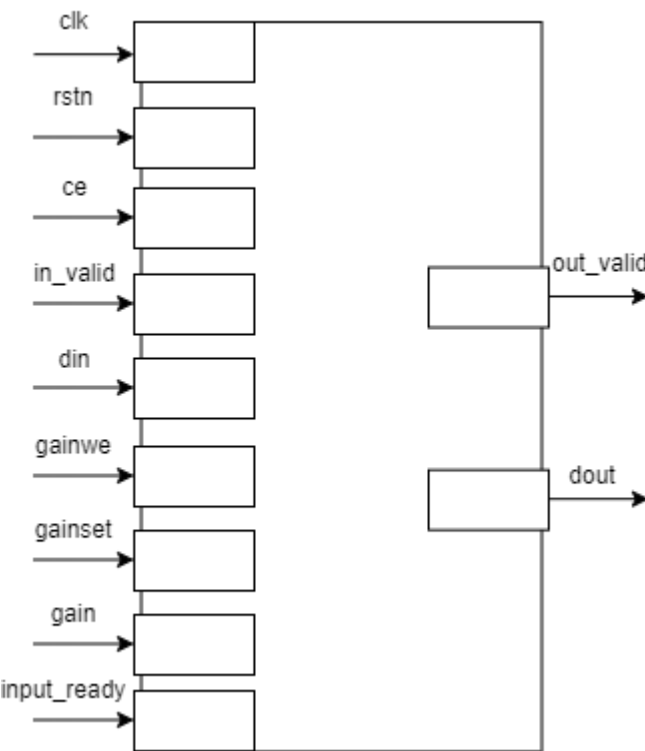


Table 4-1 I/O List of Gowin Equalizer IP

Signal	I/O	Description
clk	input	Input clock signal
rstn	input	Reset signal, active-low
ce	input	Module enable signal
in_valid	input	High level means the input data is valid.
din	input	Input signal
gainwe	input	Set to high level when loading gain
gainset	input	After the gain is loaded, set to high level in the next

Signal	I/O	Description
		clock cycle to indicate that the gain loading is complete.
gain	input	Input gain signal
input_ready	input	High level means that the data can be input
out_valid	Output	Output valid signal, active-high.
dout	Output	Output signal

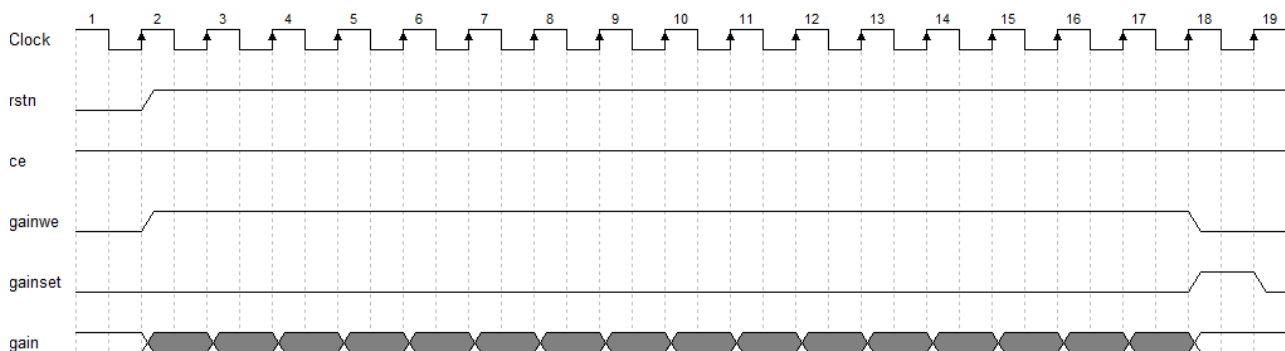
5 Timing Description

This section describes the timing of Gowin Equalizer IP.

5.1 Signal Timing

The loading of coefficients is as shown in Figure 5-1, and the band size is 16.

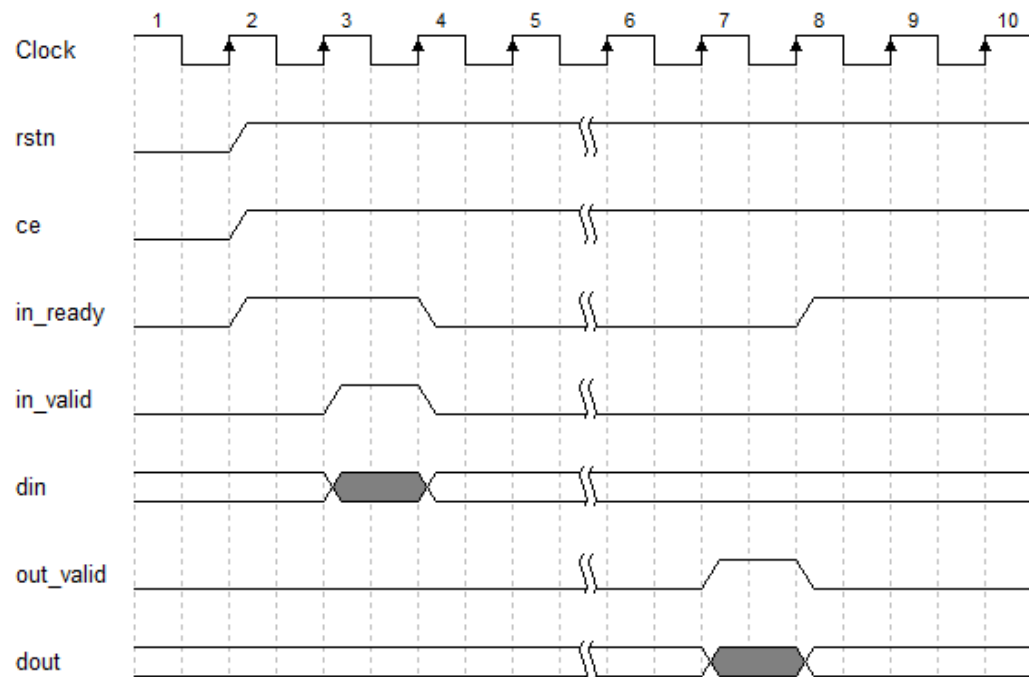
Figure 5-1 Timing Diagram for Loading Gain Coefficient



When loading gain coefficients, the gainwe signal should be set to high simultaneously, and one coefficient should be written in each clock cycle. The number of coefficients written should match the configured band sizes. After the gain coefficient loading is completed, the gainset signal should be set to high level in the next clock cycle.

5.2 Read and Write Timing

Figure 5-2 Equalizer Read and Write Timing



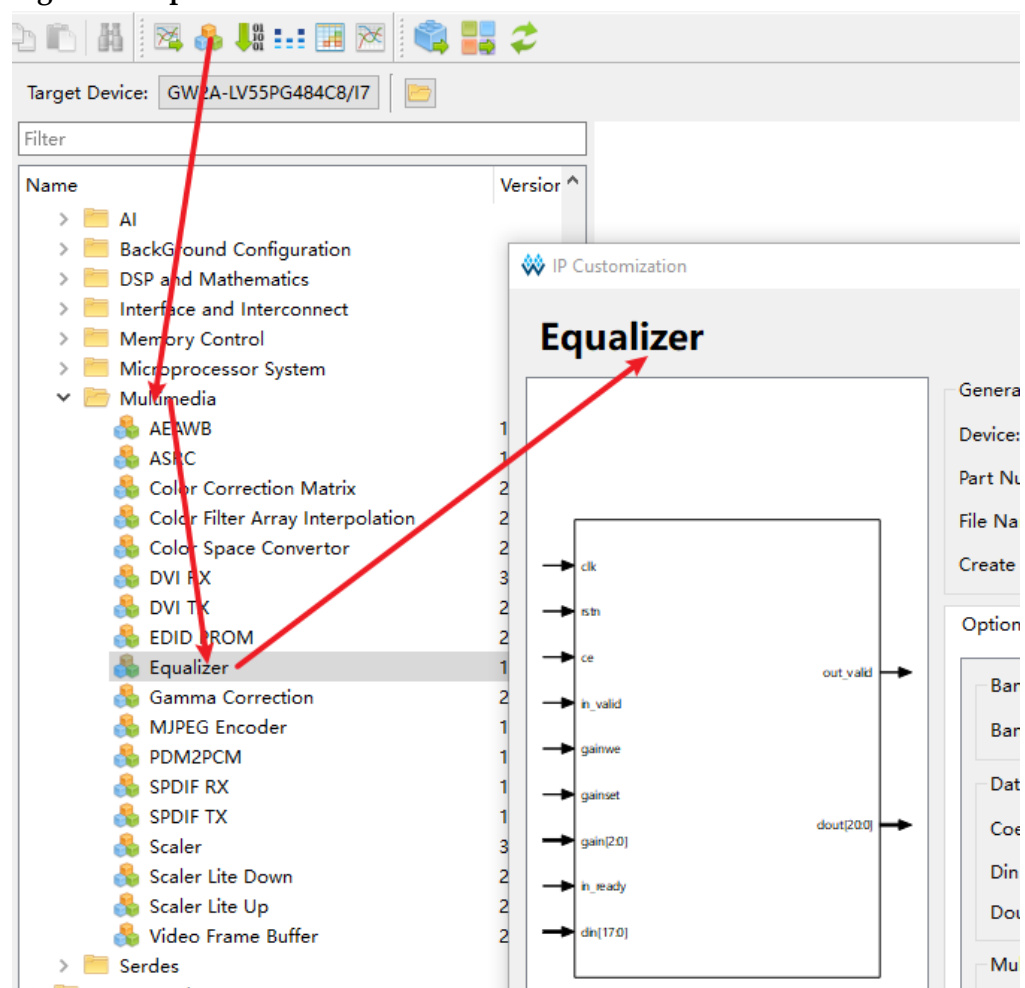
When *in_ready* is high, it indicates that Gowin Equalizer IP is ready to receive input data. When inputting data, the *in_valid* signal needs to be pulled high to indicate that the input is valid. After the delay of several clock cycles, the output signal *dout* can be obtained, and at the same time, the *out_valid* signal will also become high, indicating that the output is valid.

6 GUI Configuration

6.1 IP Generation

Click "Tools > IP Core Generator > Multimedia" to call and configure Equalizer; toolbar icon is also available to open the IP as shown in Figure 6-1.

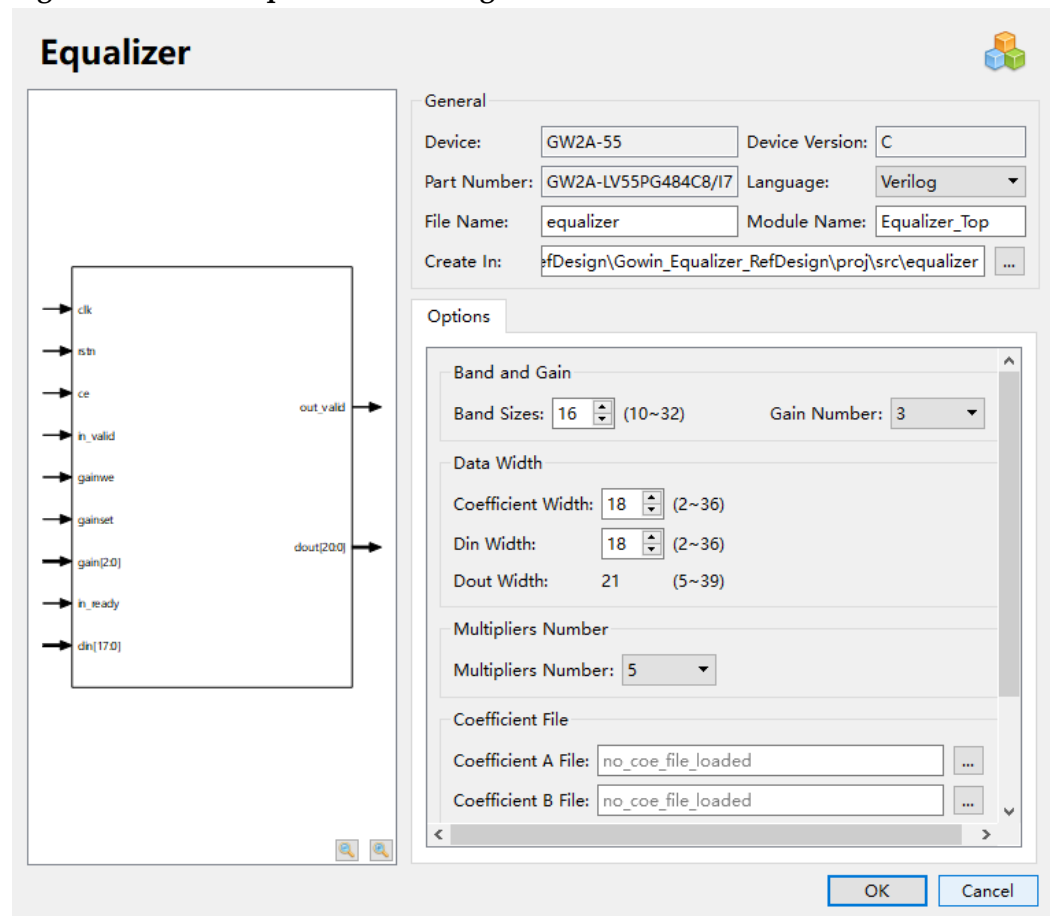
Figure 6-1 Open the IP via Toolbar Icon



6.2 Configuration Interface

Gowin Equalizer IP configuration interface is shown in Figure 6-2.

Figure 6-2 Gowin Equalizer IP Configuration Interface



This manual takes GW2A-LV55PG484C8/I7 part number as an example.

- You can configure the path of generated IP core folder in the "Create In" text box.
- You can configure the generated IP file name in the "File Name" text box.
- You can configure the generated IP module name in the "Module Name" text box.

6.3 Description of Initialization Coefficient File

Gowin Equalizer IP supports coefficient initialization function. When Gowin Equalizer IP is called, the initialization coefficient file must be specified. If the filter is as follows:

$$y_n = b_1x_n + b_2x_{n-1} + b_3x_{n-2} - a_1y_{n-1} - a_2y_{n-2}$$

Then in the feedback coefficient file, the data should be placed in the following position:

...
am,1
am,2

In the feedforward coefficient file, the data should be placed in the following position:

...
bm,1
bm,2
bm,3

m is the band size.

And all data is decimal plain text. The size of the initialization coefficient should be within the range of the selected coefficient bit width, otherwise the GUI interface will prompt a data error.

The Equalizer coefficient data format conversion can be generated by referring to the following MATLAB example.

Figure 6-3 MATLAB Example

```
% constants
EQORDER = 2; % Filter order for each stage
SAMPLERATE = 44100; % Sampling rate for audio processing
FRACTION_WIDTH = 18; % Fractional width for fixed-point representation

STRUCTURE = 'Cascade'; % Equalizer structure
BANDWIDTH = '1 octave'; % Equalizer bandwidth configuration
GAIN_RANGE = 12; % -12dB~12dB
GAIN_NUM = 3; % Number of gain stages

% Create a graphic equalizer object with specified settings
equalizer = graphicEQ('EQOrder', EQORDER, 'Bandwidth', BANDWIDTH, 'Structure', STRUCTURE, 'SampleRate', SAMPLERATE);

% Get the preferred frequency bands from the equalizer object
freq_bands = info(equalizer).PreferredFrequencies;
num_bands = length(freq_bands);

% Initialize coefficient arrays
Coeff_B = zeros(EQORDER+1, GAIN_NUM, num_bands);
Coeff_A = zeros(EQORDER+1, GAIN_NUM, num_bands);

% Generate coefficients for different gain stages and frequency bands
for i = 1:GAIN_NUM % 1,2,3 mean -12dB, 0dB and +12dB
    for j = 1:num_bands
        GAINS = zeros(1, num_bands);
        GAINS(j) = GAIN_RANGE*i - GAIN_RANGE*2;
        equalizer.Gains = GAINS;

        [b,a] = coeffs(equalizer);
        Coeff_B(:,i,j) = b(:,j);
        Coeff_A(:,i,j) = a(:,j);
    end
end

% Convert to fixed-point representation with a given fractional width
Coeff_B_fi = round(Coeff_B*2^FRACTION_WIDTH);
Coeff_A_fi_temp = round(Coeff_A*2^FRACTION_WIDTH);
Coeff_A_fi = Coeff_A_fi_temp([ 2 3 ],:);

% Write the coefficients to external files for later use
writematrix(Coeff_B_fi(:), 'coeff_b_in.dat')
writematrix(Coeff_A_fi(:), 'coeff_a_in.dat')
```

7 Reference Design

Please see [reference design](#) for details at Gowinsemi website.

8 File Delivery

The delivery file of Gowin Equalizer IP includes documentation and reference design.

8.1 Documentation

The folder mainly contains the user guide in PDF version.

Table 8-1 Document List

Name	Description
IPUG1048, Gowin Equalizer IP User Guide	Gowin Equalizer IP User Guide, namely this one

8.2 Reference Design

The Ref. Design folder contains the netlist file, user reference design, constraints file, top-level file, and the project file, etc.

Table 8-2 Gowin Equalizer IP RefDesign Folder Content List

Name	Description
top.v	The top module of reference design
Equalizer.cst	Project physical constraints file
Equalizer.sdc	Project timing constraints file
Equalizer.rao	Configuration file
Equalizer.v	Generates Equalizer IP top-level file, encrypted.

