



Gowin Adder Subtractor IP User Guide

IPUG1046-1.0E, 05/09/2024

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Revision History

Date	Version	Description
05/09/2024	1.0E	Initial version published.

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1 About This Guide

1.1 Purpose

The purpose of Gowin Adder Subtractor IP User Guide is to help you learn the features and usage of this product by providing the descriptions of functions, ports, timing, GUI and reference design, etc. The software screenshots and the supported products listed in this manual are based on Gowin Software V1.9.8.11-1. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at www.gowinsemi.com:

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS821, GW1NS series of FPGA Products Data Sheet](#)
- [DS861, GW1NSR series of FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS971, GW2AN-18X & 9X Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
ALU	Arithmetic Logical Unit
LUT	Look-up Table
IP	Intellectual Property

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

Gowin Adder Subtractor IP is designed to realize integer addition and subtraction operations with less logic resources, supporting addition and subtraction operations for both signed and unsigned integers.

Table 2-1 Gowin Adder Subtractor IP Overview

Gowin Adder Subtractor IP	
Logic Resource	Please refer to Table 2-2.
Delivered Doc.	
Design Files	Verilog
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSythesis
Application Software	Gowin Software (V1.9.8.11 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.1 Features

- Supports addition and subtraction operations for both signed and unsigned integers
- The input data width ranges from 2 to 96 bits
- Supports input/output carry
- Supports configurable output latency

2.2 Max. Frequency

The max. frequency of Gowin Adder and Subtractor IP is mainly determined by speed grade of the selected devices.

2.3 Latency

The latency of Gowin Adder Subtractor IP is determined by the

configuration parameters.

2.4 Resource Utilization

Gowin Adder and Subtractor IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades.

Take GW2A-55 FPGA as an example. See Table 2-2 for the resource utilization. For the applications on the other GOWINSEMI devices, please refer to the later release.

Table 2-2 Resource Utilization

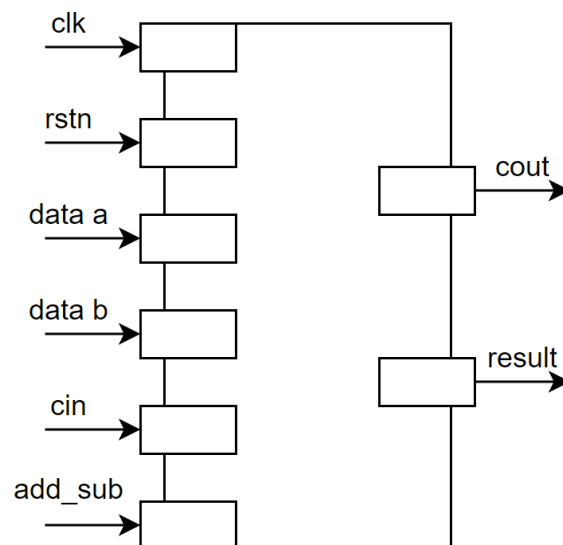
Device	Speed Grade	Resource Name	Resource Utilization
GW2A-55	C8/I7	Registers	746
		LUTs	24
		ALUs	5609
		I/O Buf	296

3 Functional Description

3.1 Structure and Function

Gowin Adder and Subtractor IP can realize addition and subtraction operations for both signed and unsigned integers. And you can configure parameters as required when generating the module. The diagram is as shown in Figure 3-1.

Figure 3-1 Gowin Adder Subtractor IP Interface



3.2 Data Setting

The input data can be configured as Signed and Unsigned on the GUI, and the bit width of the input data can be configured separately. The maximum bit width is 96 bits, and the minimum bit width is 2 bits.

3.3 Function Selection

You can select the operating mode through GUI, including Adder, Subtractor, and Adder/Subtractor.

4 Port Description

The details of Gowin Adder and Subtractor IP I/O ports are shown in Table 4-1, and the interface diagram is as shown in Figure 3-1.

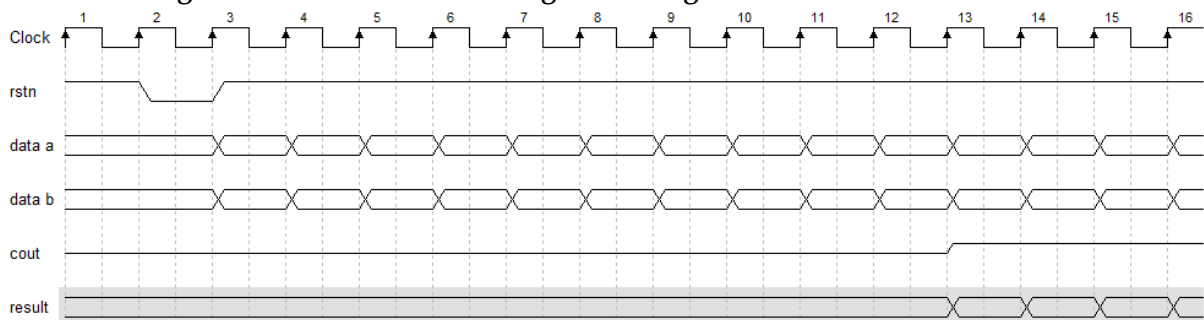
Table 4-1 Gowin Adder Subtractor IP IO List

Signal	I/O	Description
clk	Input	Clock signal (optional)
rstn	Input	Reset signal, active-low (optional)
data_a	Input	Input a
data_b	Input	Input b
cin	Input	Input carry (optional)
add_sub	Input	Select addition or subtraction (optional)
cout	Output	Output carry (optional)
result	Output	Output data

5 Timing Description

This section describes the timing of Gowin Adder and Subtractor IP. Adder and Subtractor signal timing is as shown in Figure 5-1.

Figure 5-1 Adder Subtractor Signal Timing



Note!

data a width = 8, data b width = 8, Latency=10.

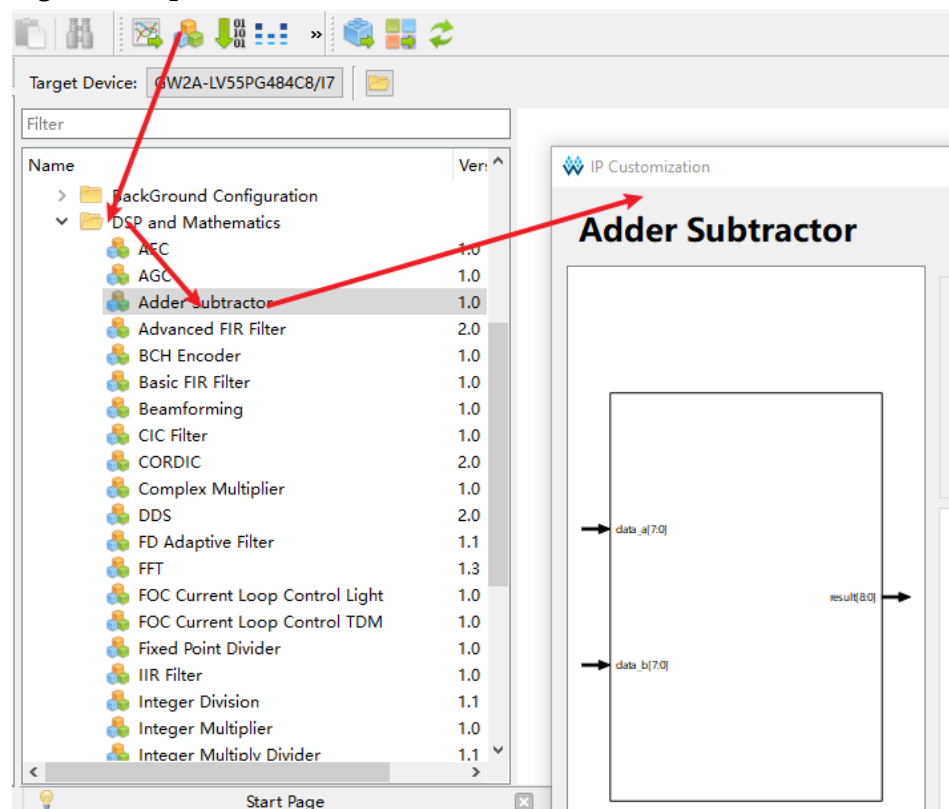
As shown in the diagram, when the latency is set to 10, the result of adding or subtracting the first input data will be outputted after 10 clock cycles.

6 GUI Configuration

6.1 IP Generation

Click "Tools > IP Core Generator > DSP and Mathematics" to call and configure Adder Subtractor; toolbar icon is also available to open the IP as shown in Figure 6-1.

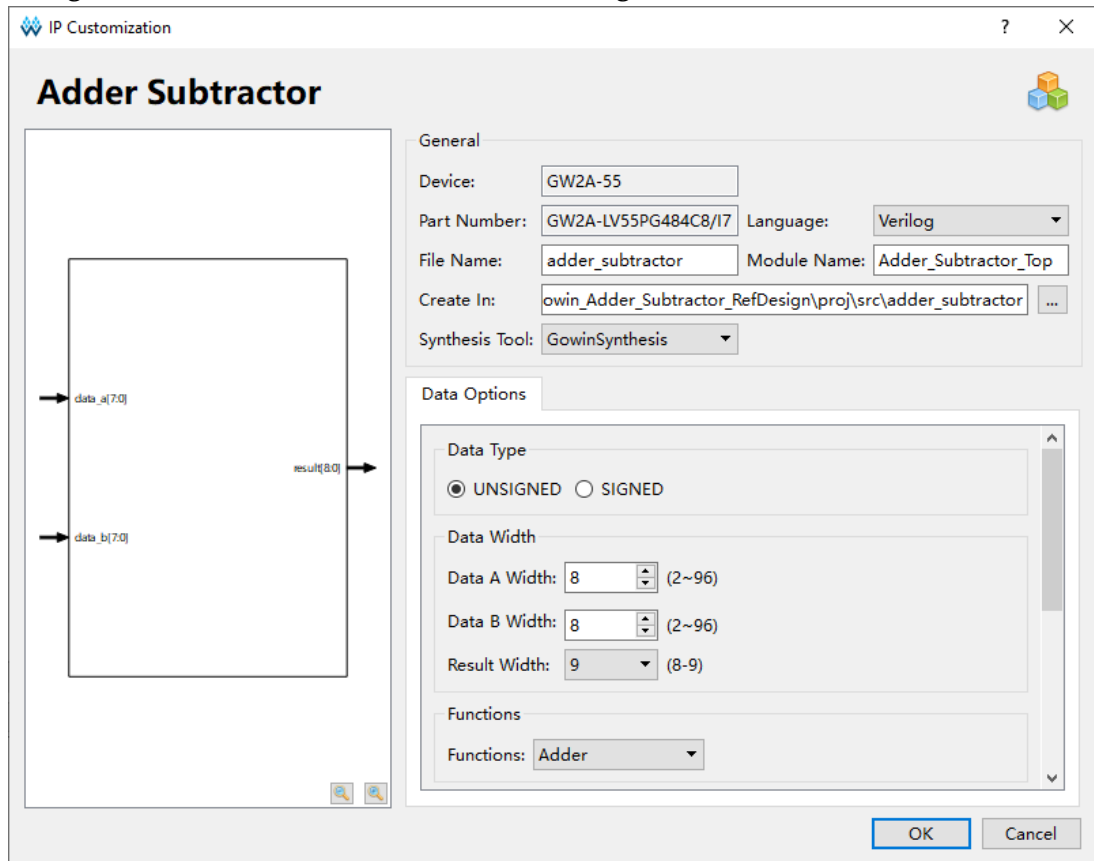
Figure 6-1 Open the IP via Toolbar Icon



6.2 Configuration Interface

Gowin Adder Subtractor IP configuration interface is shown in Figure 6-2.

Figure 6-2 Gowin Adder Subtractor IP Configuration Interface



This manual takes GW2A-55 chip and GW2A-LV55PG484C8/I7 part number as an example.

- You can configure the path of generated IP core folder in the "Create In" text box.
- You can configure the generated IP file name in the "File Name" text box.
- You can configure the generated IP module name in the "Module Name" text box.

7 Reference Design

Please refer to the related test cases in Gowin Adder Subtractor IP [RefDesign](#).

