



Gowin FP Add Sub IP

User Guide

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Revision History

Date	Version	Description
05/09/2024	1.0E	Initial version published.
03/27/2026	1.1E	● Updated section 1.2 Related Documents. ● Updated section 2.4 Resource Utilization. ● Added Table 6-1 Configuration Options.

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1 About This Guide

1.1 Purpose

Gowin FP Add Sub IP User Guide includes the descriptions of the functions, features, ports, timing, call and configuration, and reference design, etc. It helps users quickly learn the features and usage of Gowin FP Add Sub IP. The software screenshots and the supported products listed in this manual are based on Gowin Software V1.9.12.02. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at www.gowinsemi.com:

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS821, GW1NS series of FPGA Products Data Sheet](#)
- [DS861, GW1NSR series of FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS971, GW2AN-18X & 9X Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1118, GW5ART series of FPGA Products Data Sheet](#)

- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
ALU	Arithmetic Logical Unit
FP	Floating Point
IP	Intellectual Property
LUT	Look-up Table
NaN	Not a Number

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

Gowin FP (Floating Point) Add Sub IP is designed to realize integer addition and subtraction operations with less logic resources, supporting addition or subtraction operations of two single-precision floating-point numbers. This IP supports optional output ports such as zero, overflow, underflow, and NaN (Not a Number).

Table 2-1 Gowin FP Add Sub IP Overview

Gowin FP Add Sub IP	
Logic Resource	Please refer to Table 2-2
Delivered Doc.	
Design Files	Verilog
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9 Beta-1 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.1 Features

- Supports addition and subtraction operations.
- Supports optional output ports such as zero, overflow, underflow, and NaN.
- Supports an optional latency of 3-4 clock cycles.

2.2 Max. Frequency

The max. frequency of Gowin FP Add Sub IP is mainly determined by speed grade of the selected devices. The max. frequency of Gowin IP is mainly determined by speed grade.

2.3 Latency

The latency of Gowin FP Add Sub IP is determined by the configuration parameters.

2.4 Resource Utilization

Gowin FP Add Sub IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades.

Take GW2A-55 FPGA as an example. See Table 2-2 for the resource utilization. For the applications on the other GOWINSEMI devices, please refer to the later release.

Table 2-2 Resource Utilization

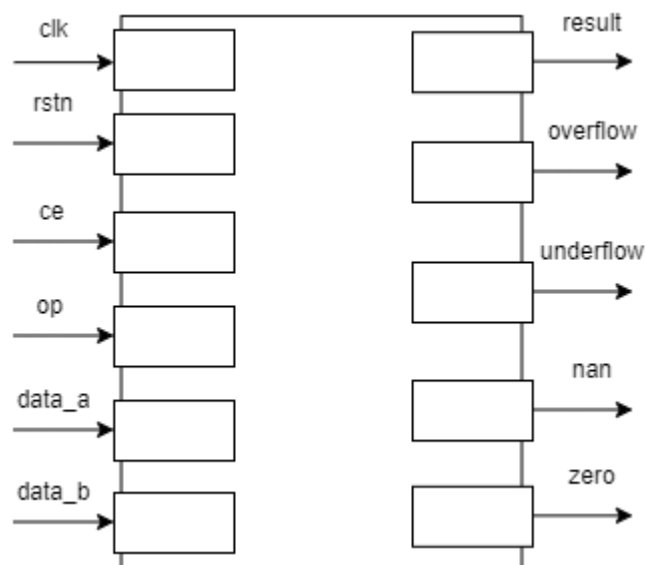
Device	Speed Grade	Resource	Resource Utilization	Note
GW2A-55	C8/I7	Registers	138	● Add/Sub input; ● Overflow, Underflow, NaN, and Zero outputs; ● 3 clock cycles latency.
		LUTs	747	
		ALUs	107	

3 Functional Description

3.1 Structure and Function

Gowin FP Add Sub IP enables addition and subtraction operations for two single-precision floating-point numbers. Users can configure parameters according to their requirements when generating this module. The structure is as shown in Figure 3-1 .

Figure 3-1 FP Add Sub Interface



3.2 Mode Selection

You can select the operating mode through GUI, including Addition, Subtraction, and Add_Sub (input port to select the adder or subtractor).

4 Port Description

The details of Gowin FP Add Sub IP I/O ports are shown in Table 4-1. The port diagram is as shown in Figure 3-1 .

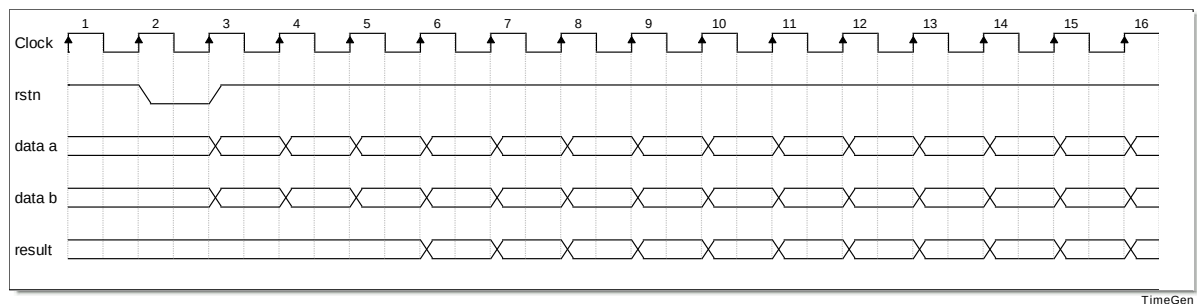
Table 4-1 Gowin FP Add Sub IP IO List

Signal	I/O	Description
clk	input	Clock signal
rstn	input	Reset signal, active-low
ce	input	Clock enable signal, active-high (optional)
op	input	Select addition or subtraction (optional)
data_a	input	Input a
data_b	input	Input b
overflow	Output	Overflow (optional)
underflow	Output	Underflow (optional)
nan	Output	NaN (optional)
zero	Output	Zero (optional)
result	Output	Output result

5 Timing Description

This chapter describes Gowin FP Add Sub IP timing. The FP Add Sub timing is as shown in Figure 5-1.

Figure 5-1 FP Add Sub Timing



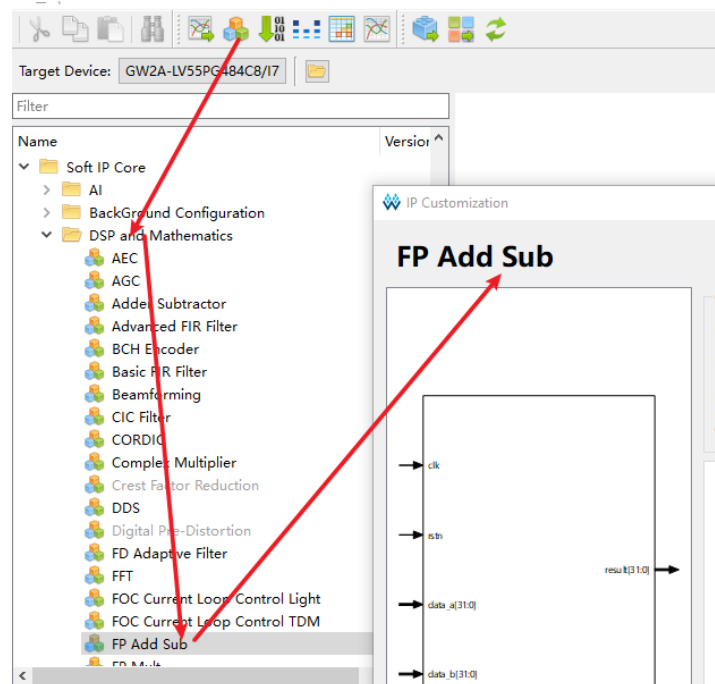
- When the latency is set to 3, the addition/subtraction result is available 3 clock cycles after the input data is accepted.
- When the latency is set to 4, the addition/subtraction result is available 4 clock cycles after the input data is accepted.

6 GUI Configuration

6.1 IP Generation

Click "Tools > IP Core Generator > DSP and Mathematics" to call and configure FP Add Sub; toolbar icon is also available to open the IP as shown in Figure 6-1.

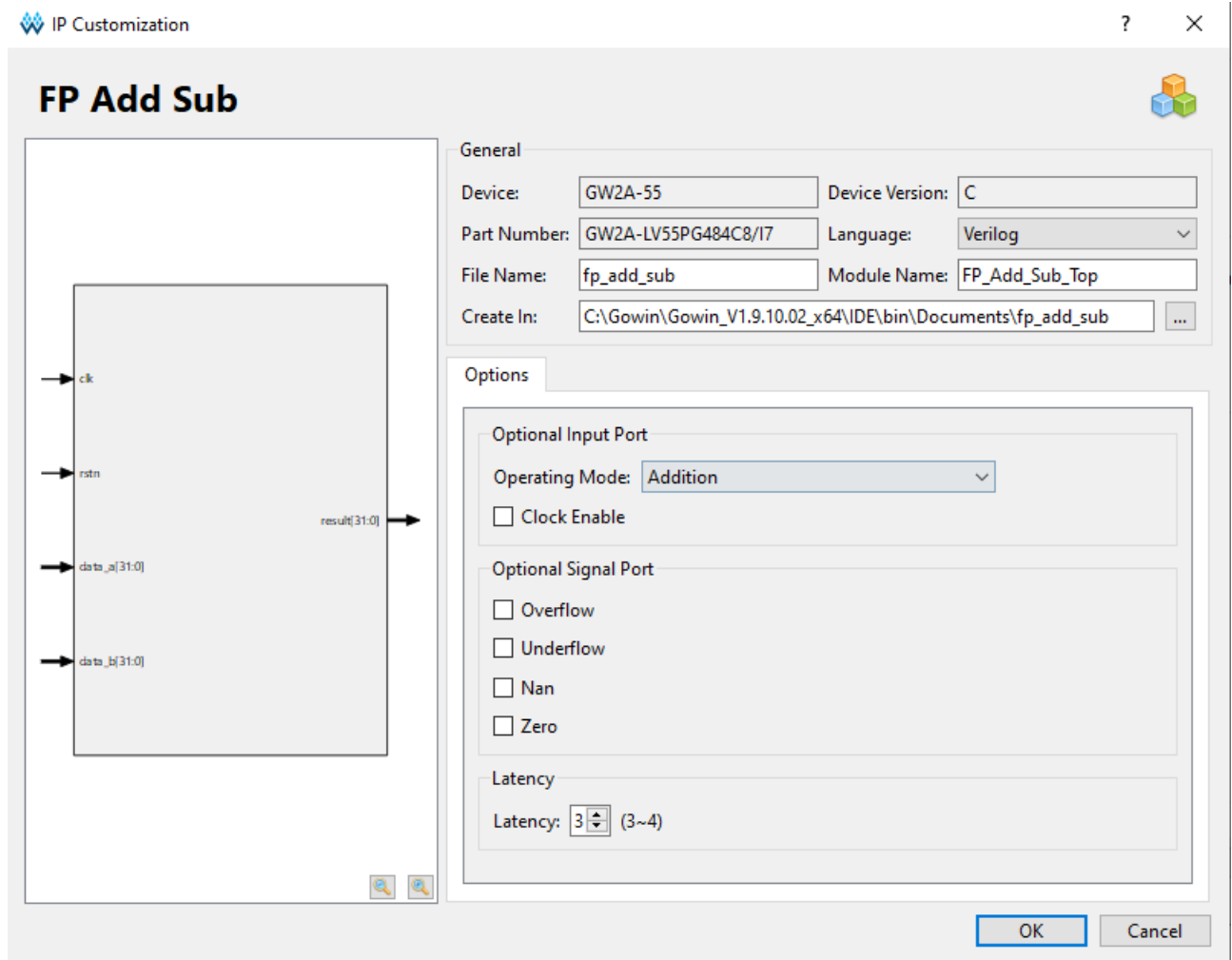
Figure 6-1 Open the IP via Toolbar Icon



6.2 Configuration Interface

Gowin FP Add Sub IP configuration interface is shown in Figure 6-2.

Figure 6-2 Gowin FP Add Sub IP Configuration Interface



This manual uses GW2A-55 chip and GW2A-LV55PG484C8/I7 part number as an example.

- The "Create In" option is used to specify the folder path where the IP core files will be generated. Users can modify this path.
- The "File Name" option is used to specify the name of the generated IP core file. Users can modify this name.
- The "Module Name" option is used to specify the name of the generated IP module. Users can modify this name.

The IP configuration interface provides three configurable settings: "Optional Input Port", "Optional Signal Port", and "Latency", as shown in Table 6-1. Users can adjust these settings according to their requirements.

Table 6-1 Configuration Options

Option	Description
Optional Input Port	Used to select addition, subtraction, or add/sub mode; supports clock enable.
Optional Signal Port	Output ports for Overflow, Underflow, NaN, and Zero.
Latency	Optional 3 or 4 clock cycles latency; selecting 4 cycles allows the IP to achieve a higher maximum frequency.

7 Reference Design

Please refer to the related test cases in Gowin FP Add Sub IP
[RefDesign](#).

