



Gowin DDR2 PHY Interface IP

User Guide

IPUG1183-1.1E, 06/13/2025

Copyright © 2025 Guangdong Gowin Semiconductor Corporation. All Rights Reserved.

GOWIN is a trademark of Guangdong Gowin Semiconductor Corporation and is registered in China, the U.S. Patent and Trademark Office, and other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders. No part of this document may be reproduced or transmitted in any form or by any means, electronic, mechanical, photocopying, recording or otherwise, without the prior written consent of GOWINSEMI.

Disclaimer

GOWINSEMI assumes no liability and provides no warranty (either expressed or implied) and is not responsible for any damage incurred to your hardware, software, data, or property resulting from usage of the materials or intellectual property except as outlined in the GOWINSEMI Terms and Conditions of Sale. GOWINSEMI may make changes to this document at any time without prior notice. Anyone relying on this documentation should contact GOWINSEMI for the current documentation and errata.

Revision History

Date	Version	Description
04/19/2024	1.0E	Initial version published.
06/13/2025	1.1E	● Descriptions for CLK Ratio = 1:2 added. ● Parameter configuration descriptions updated.

Contents

Contents	i
List of Figures	ii
List of Tables	iii
1 About This Guide	1
1.1 Purpose	1
1.2 Related Documents	1
1.3 Terminology and Abbreviations	2
1.4 Support and Feedback	2
2 Overview	3
2.1 Introduction	3
2.2 Features	3
2.3 Resource Utilization	4
3 Functional Description	5
3.1 Structure	5
3.2 User Interface and Timing Descriptions	6
3.2.1 User Interface	6
3.2.2 Write Data Timing	9
3.2.3 Write Data Timing	17
3.2.4 Bank Active	17
3.2.5 EYE SCAN	18
3.3 Clock, Reset, and pll _stop	19
4 Port List	20
5 Call and Configure	23
5.1 IP Generation	23
5.2 Parameter Configuration	24

List of Figures

Figure 3-1 Gowin DDR2 PHY Interface IP Structure	5
Figure 3-2 Initialization Completed Signal Timing Diagram	6
Figure 3-3 OSER8 Outputting O_ddr_cs_n Diagram	6
Figure 3-4 O_ddr_cs_n Output Diagram	7
Figure 3-5 O_ddr_cs_n output through OSER4	7
Figure 3-6 O_ddr_cs_n Output Timing Diagram with CLK Ratio of 1:2	7
Figure 3-7 OSER8 Outputting ddr_odt Diagram	8
Figure 3-8 Timing Diagram for Write Data with CL=3, AL=0	10
Figure 3-9 Timing Diagram for Write Data with CL=4, AL=0	11
Figure 3-10 Timing Diagram for Write Data with CL=5, AL=0	12
Figure 3-11 Timing Diagram for Write Data with CL=6, AL=0	13
Figure 3-12 Timing Diagram for Write Data with Burst Length=8, CL=3, AL=0	14
Figure 3-13 Timing Diagram for Write Data with Burst Length=8, CL=4, AL=0	14
Figure 3-14 Timing Diagram for Write Data with Burst Length=8, CL=5, AL=0	15
Figure 3-15 Timing Diagram for Write Data with Burst Length=8, CL=6, AL=0	15
Figure 3-16 Timing Diagram for Write Data with Burst Length=4, CL=6, AL=0	16
Figure 3-17 Data Mask Timing Diagram	16
Figure 3-18 Timing Diagram for Read Data with CLK Ratio=1:4, CL=6, AL=0	17
Figure 3-19 Timing Diagram for Read Data with CLK Ratio=1:2, Burst Length=8, CL=6/4, AL=0	17
Figure 3-20 Active Timing Diagram When CLK Ratio=1:4	18
Figure 3-21 Read/Write Instruction Interface Selection	19
Figure 5-1 IP Core Generator Interface	23
Figure 5-2 DDR2 PHY Interface Configuration Interface	24
Figure 5-3 WR Timing Diagram when WR=4	26

List of Tables

Table 1-1 Terminology and Abbreviations	2
Table 2-1 Gowin DDR2 PHY Interface IP Overview	3
Table 2-2 Resource Utilization	4
Table 4-1 I/O List of Gowin DDR2 PHY Interface IP	20
Table 5-1 DDR2 Time Parameter	26

1 About This Guide

1.1 Purpose

The purpose of Gowin DDR2 PHY Interface IP User Guide is to help you quickly learn the features and usage of Gowin DDR2 PHY Interface IP by providing the descriptions of the functions, ports, timing, and GUI. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.11.02. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at www.gowinsemi.com:

- [SUG100, Gowin Software User Guide](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS981, GW5AST series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS971, GW2AN-18X &9X Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
IP	Intellectual Property
LUT	Look-up Table
PLL	Phase-locked Loop
MC	Memory Controller
DDR2 SDRAM	Double-Data-Rate Synchronous Dynamic Random Access Memory
ODT	On-die Termination
PHY Layer	Physical Layer
REG	Register
FIFO	First Input First Output

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Introduction

Gowin DDR2 PHY Interface IP integrates DQS hardcore and other related hardcore resources to realize DDR2 PHY function, which requires customers to implement MC layer to interface with DDR2 PHY Interface IP, combining them into a complete MC+PHY IP.

Table 2-1 Gowin DDR2 PHY Interface IP Overview

Gowin DDR2 PHY Interface IP	
Logic Resource	See Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.11.02 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features

- Supports Arora Family devices
- Complies with the JESD79-2F standard
- Supports memory data path widths of 8, 16, 24, 32, 40, 48, 56, and 64 bits
- Supports single-rank RDIMM, UDIMM, and SODIMM memory modules
- Supports x8 and x16 data width memory chips
- BURST MODE supports 4 or 8
- Memory clock to User clock frequency ratio is 4:1 or 2:1
- Configurable CL, AL, tFAW, tRAS, tRCD, tRFC, tRRD, tRTP, tWTR

- Supports on-chip ODT

2.3 Resource Utilization

Gowin DDR2 PHY Interface IP is implemented with Verilog HDL. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW5A(R)-25 device as an instance, the resource utilization is as shown in Table 2-2. For the resource utilization of other devices, please refer to later release information.

Table 2-2 Resource Utilization

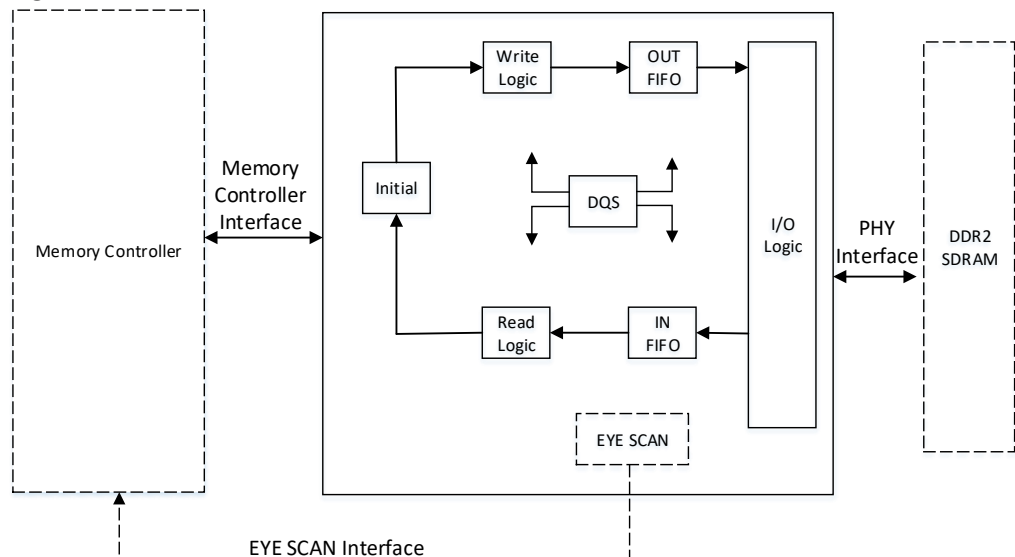
Device	Programming Language	LUTs	REGs	ALUs	BSRAM
GW5A(R)-25	Verilog HDL	2817	3397	117	16

3 Functional Description

3.1 Structure

Gowin DDR2 PHY Interface IP consists of three parts: memory controller, I/O logic and memory logic, as shown in Figure 3-1.

Figure 3-1 Gowin DDR2 PHY Interface IP Structure



- Memory Controller: Users are required to design and implement the memory controller module according to this manual.
- Initial: Initialization module, used to implement Read Calibration.
- Write Logic, Read Logic: Used to implement read and write control logic.
- OUT FIFO, IN FIFO: Used to buffer read and write data as well as instructions.
- EYE SCAN: Used to scan the read data, as detailed in section [3.2.5 EYE SCAN](#).

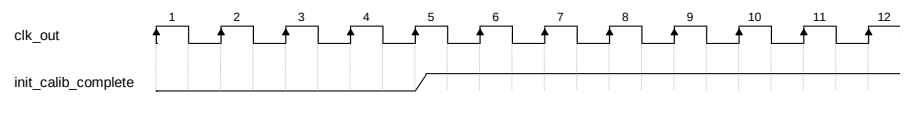
3.2 User Interface and Timing Descriptions

3.2.1 User Interface

Initialization Completed Interface

- **init_calib_complete**: The DDR2 SDRAM needs to be calibrated before write and read. Therefore, after power on, IP will initialize and calibrate the DDR2 SDRAM, and the **init_calib_complete** is pulled high after the initialization is completed, as shown in Figure 3-2.

Figure 3-2 Initialization Completed Signal Timing Diagram

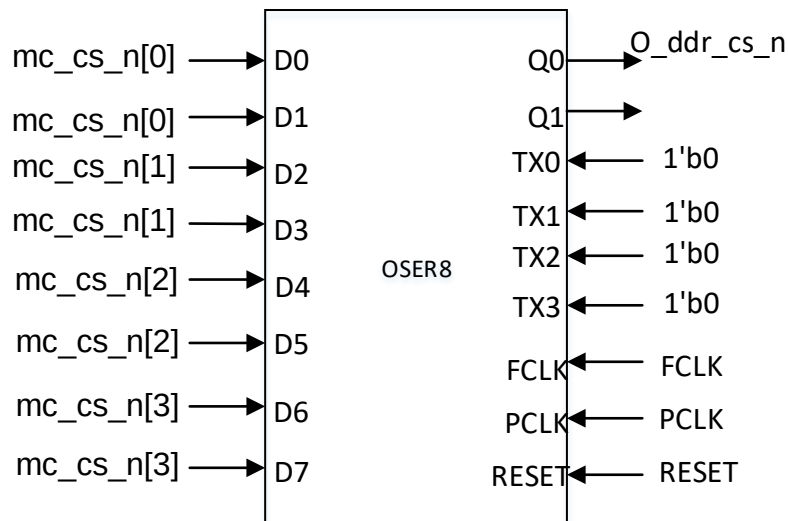


Control Signal and Address Signal Interface

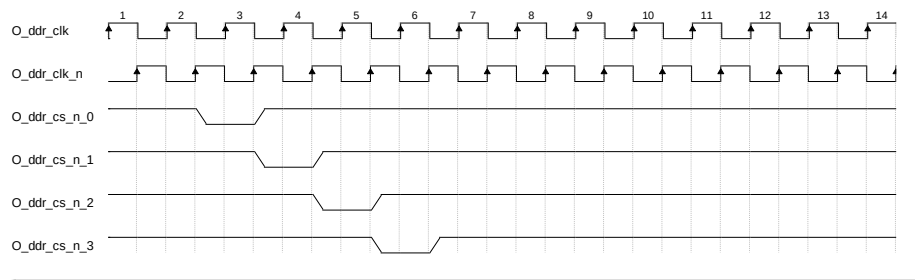
- **mc_cs_n**: This signal is a 4-bit or 2-bit signal, mapped to the 1-bit signal of **O_ddr_cs_n** to output. The reason for setting a 4-bit or 2-bit width to control a 1-bit signal output here is to precisely control the output of **O_ddr_cs_n**. It enables accurate control of **O_ddr_cs_n** output on a specific edge of **O_ddr_clk**.

When CLK Ratio is set to 1:4, the width of **mc_cs_n** is 4 bits. **mc_cs_n** is output through the OSER8, as shown in the following diagram.

Figure 3-3 OSER8 Outputting O_ddr_cs_n Diagram

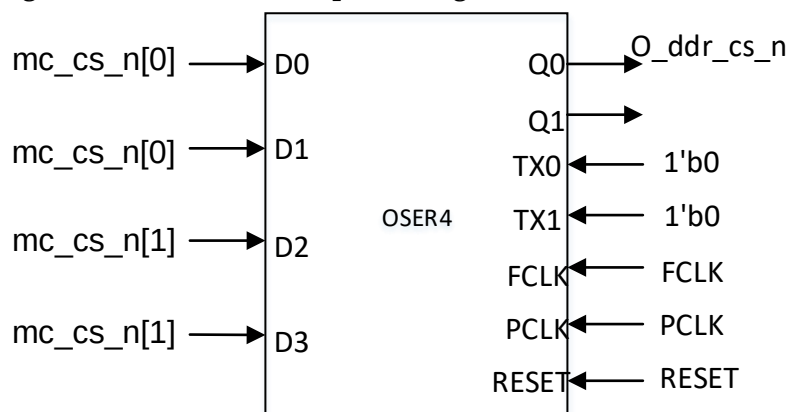


Valid **O_ddr_cs_n** can be output when **mc_cs_n[3:0]** = 4'b1110, 4'b1101, 4'b1011, 4'b0111.

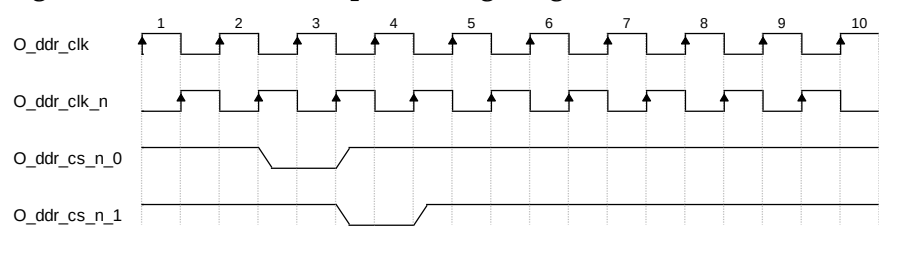
Figure 3-4 O_ddr_cs_n Output Diagram

If $mc_cs_n[3:0] = 4'b1110$, the output of $O_ddr_cs_n$ is the waveform of $O_ddr_cs_n_0$. Then, if $mc_cs_n[3:0] = 4'b1101$, the output of $O_ddr_cs_n$ is the waveform of $O_ddr_cs_n_1$, and so on. For $mc_cs_n[3:0]$, when the binary bit0 is shifted left by one bit, the low level of $O_ddr_cs_n$, after being output by OSER8, will shift right by one clock cycle.

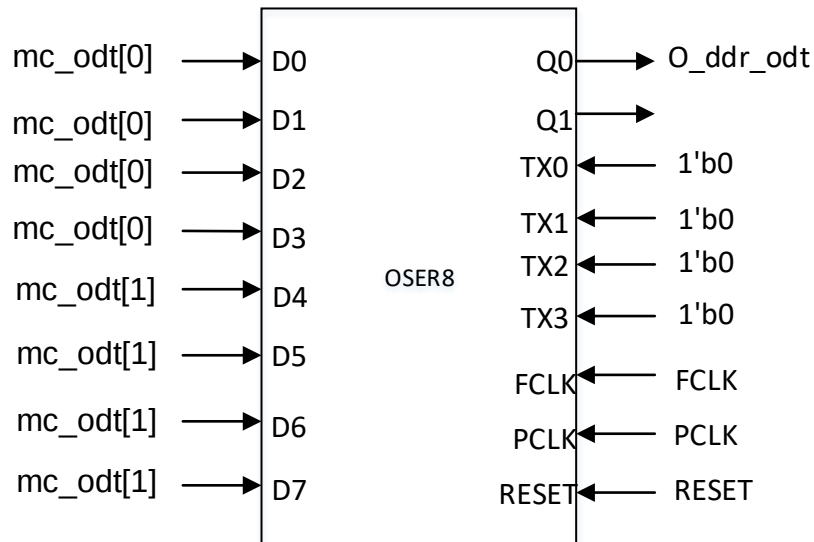
When CLK Ratio is set to 1:2, the width of mc_cs_n is 2 bits, and it is output through the OSER4, as shown.

Figure 3-5 O_ddr_cs_n output through OSER4

Similar to the case when CLK Ratio is set to 1:4, when $mc_cs_n[1:0]$ is set to 2'b10 or 2'b01, a valid $O_ddr_cs_n$ output is generated. The binary bit0 of $mc_cs_n[1:0]$ is shifted left by one position, and after passing through the OSER4, the low level of $O_ddr_cs_n$ will shift right by one clock cycle, as shown in.

Figure 3-6 O_ddr_cs_n Output Timing Diagram with CLK Ratio of 1:2

- `mc_cas_n`, `mc_we_n`, `mc_cke`: These signals are used in the same way as the `mc_cs_n` signal, and will not be described here.
- `mc_odt`: This is a 2-bit signal. When CLK Ratio = 1:4, the logic internally expands `mc_odt` to 4 bits and connects it to the OSER8 to output, as shown in Figure 3-7. When CLK Ratio = 1:2, this signal is connected to the OSER4 to output, with usage similar to the `mc_cs_n` signal. A 1-bit change in the `mc_odt` value results in a corresponding change in the output `O_ddr_odt` waveform lasting 2 `O_ddr_clk` cycles.

Figure 3-7 OSER8 Outputting `ddr_odt` Diagram

Therefore, the value of `mc_odt` changes every 1 bit, and the actual output waveform of `O_ddr_odt` changes every 2 `O_ddr_clk` cycles.

- `mc_address`: This signal is used to transmit Row/Column addresses, with a signal width of `NCK * ROW_WIDTH`. `ROW_WIDTH` is the row address width of the DDR2 chip. `NCK` is the clock ratio parameter; when CLK Ratio is set to 1:4, `NCK` = 4; when CLK Ratio is set to 1:2, `NCK` = 2. The usage of `mc_address` is similar to that of `mc_cs_n` and other signals, but with some differences. The similarity is that `mc_address` is transmitted through the OSER, and the timing control is the same. The difference is that before being transmitted through the OSER, `mc_address` undergoes a mapping transformation. The mapping relationship is as follows:

$$\text{mc_address}[j * \text{ROW_WIDTH} + i] \Rightarrow \text{mc_address_tmp}[i * \text{NCK} + j] \quad (i \geq 0, i < \text{ROW_WIDTH}, j \geq 0, j < \text{NCK}).$$

`mc_address_tmp` is the address after mapping. Every `NCK` bits of `mc_address_tmp` determine the output of one bit of `O_ddr_addr`. For example, when `NCK` = 4, `mc_address_tmp`[3:0] controls the output of `O_ddr_addr`[0], `mc_address_tmp`[7:4] controls the output of `O_ddr_addr`[1], and so on.

Back to the `mc_address` signal: taking `NCK` = 4 as an example, when `j` takes values 0, 1, 2, and 3, for `i` = 0, the corresponding 4 bits of `mc_address` determine the output of `O_ddr_addr`[0]; for `i` = 1, the

corresponding 4 bits of `mc_address` determine the output of `O_ddr_addr[1]`; and so on. When $i = \text{ROW_WIDTH} - 1$, the corresponding 4 bits of `mc_address` determine the output of the highest bit address of `O_ddr_addr`.

Users should map their actual addresses written to the MC before connecting them to `mc_address`.

- `mc_bank`: This signal is used in the same way as `mc_address`.

Data Interface

- `mc_cmd_wren`: This signal can remain at a high level since the control and address lines have pipelined timing.
- `mc_wrddata`: When `init_calib_complete` is 0 and `eye_calib_start` is 1, this signal takes the value of `eye_app_wdf_wdata`. When `init_calib_complete` is 1 and `eye_calib_start` is 0, this signal takes the original value written by the user to the MC.
- `mc_wrddata_mask`: This signal is the mask signal for `mc_wrddata`, where 1 bit corresponds to one byte of `mc_wrddata`, and the low bits correspond to the low byte of `mc_wrddata`.
- `mc_wrddata_en`: When `mc_wrddata_en` is 1, `mc_wrddata` and `mc_wrddata_mask` are valid.
- `phy_rd_data`: Data read from the DDR2 chip.
- `phy_rddata_valid`: When this signal is 1, it indicates that `phy_rd_data` is valid.

3.2.2 Write Data Timing

According to the user interface description, by changing the position of the bit 0 in the binary data of `mc_cs_n`, `mc_cas_n`, and `mc_we_n`, the number of clock cycles between the write command and the first valid write data can be adjusted (i.e., Write Latency, abbreviated as WL, where $WL = CL + AL - 1$, CL is the CAS Latency, and AL is the Additive Latency).

When Arora V devices are used, `IO_ddr_dqs` and `IO_ddr_dqs_n` need to be interrupted in a high-impedance state in advance. This is done to adapt to the hardware characteristics of the Arora V devices. The following lists different write data timings for various CL values, and the clock ratio between `clk_out` and `O_ddr_clk` is 1: 4 or 1: 2.

When CLK Ratio is set to 1:4, the write timing diagram is as shown in Figure 3-8, Figure 3-9, Figure 3-10, and Figure 3-11.

Figure 3-8 Timing Diagram for Write Data with CL=3, AL=0

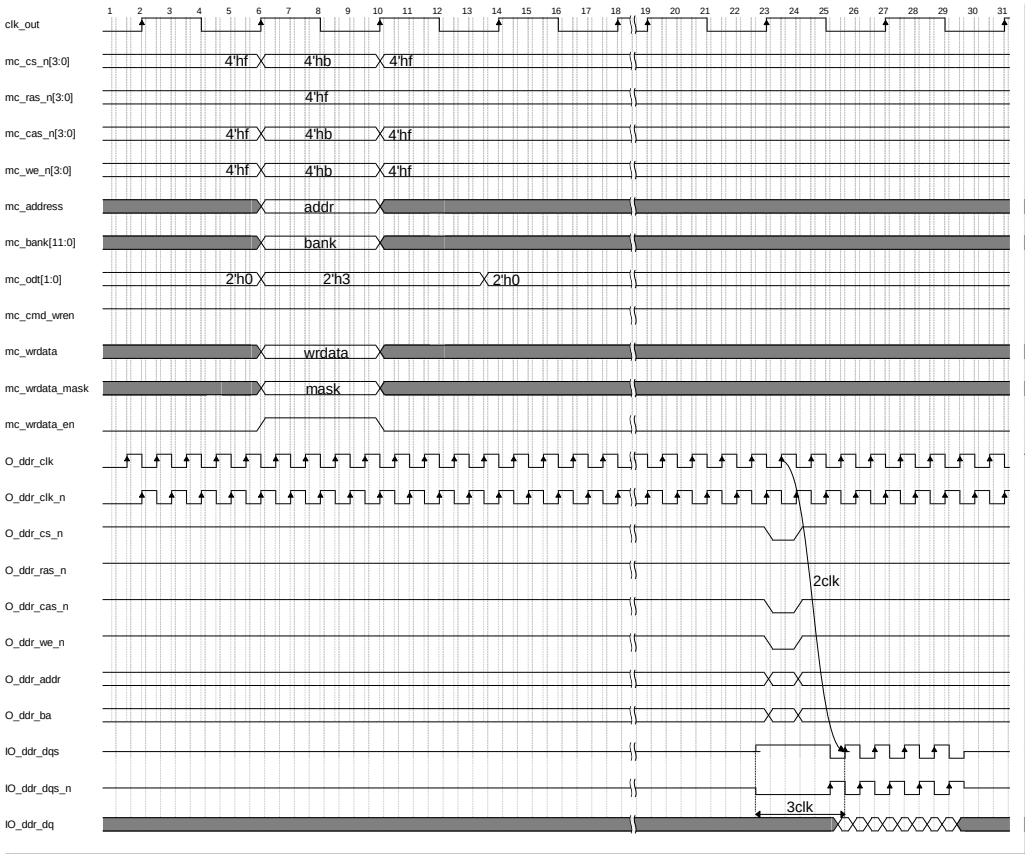


Figure 3-9 Timing Diagram for Write Data with CL=4, AL=0

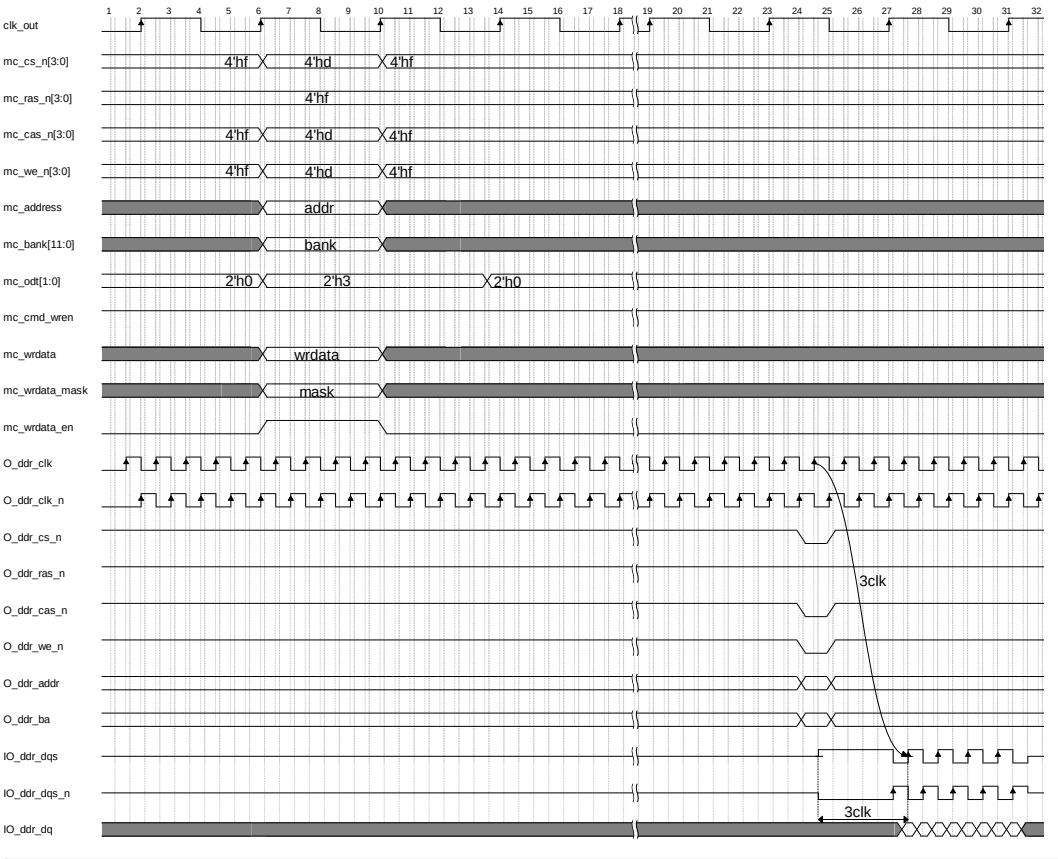


Figure 3-10 Timing Diagram for Write Data with CL=5, AL=0

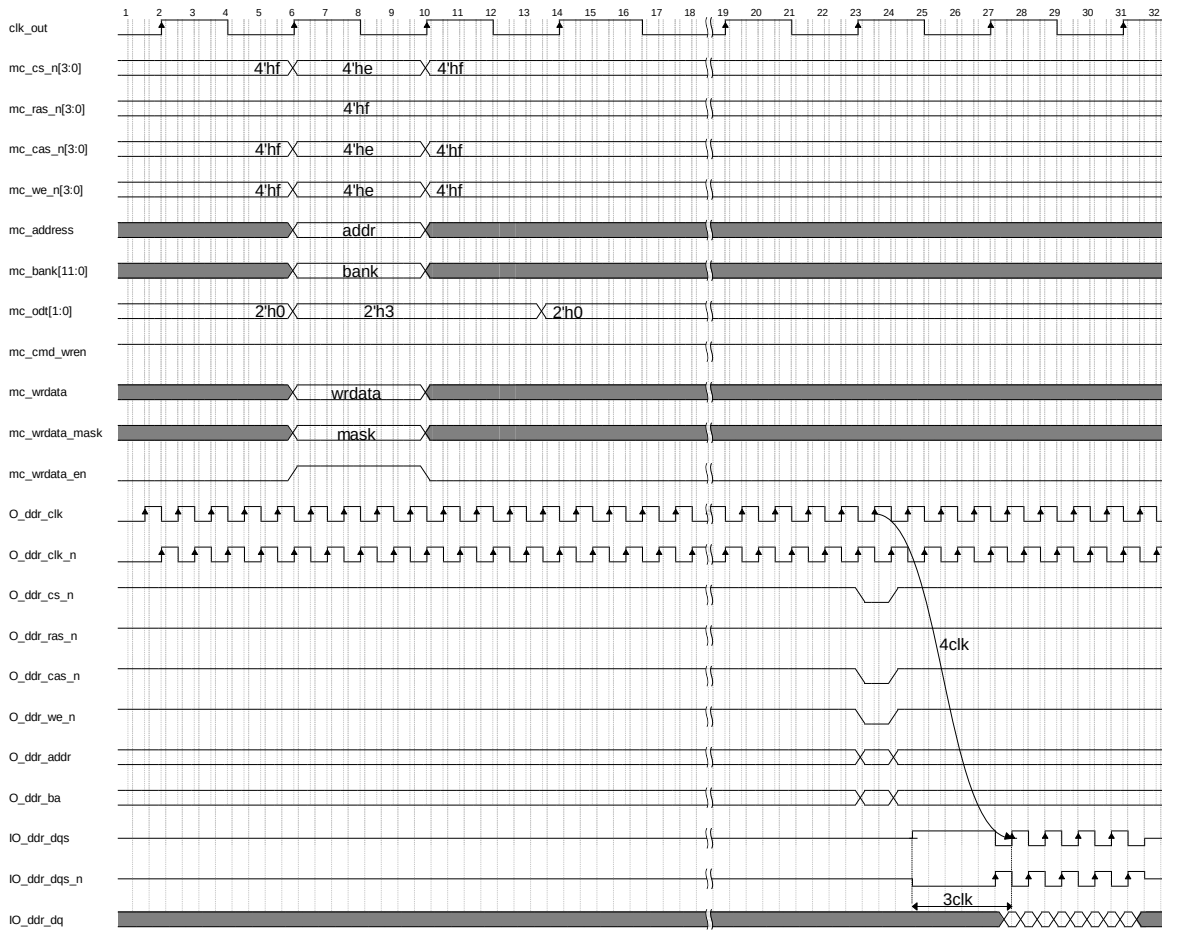
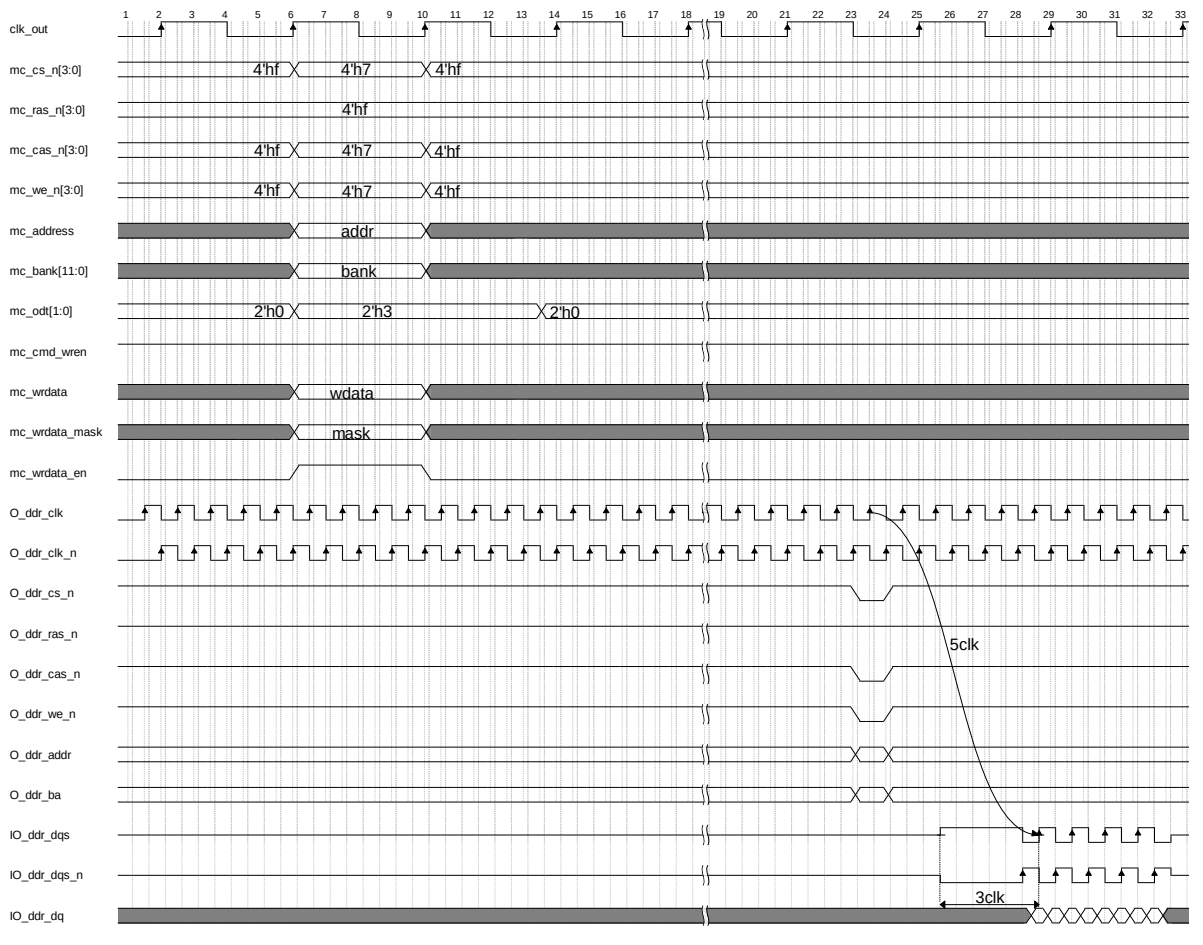


Figure 3-11 Timing Diagram for Write Data with CL=6, AL=0

When CLK Ratio is set to 1:2, the write timing diagram is as shown in Figure 3-12, Figure 3-13, Figure 3-14, Figure 3-15, and Figure 3-16.

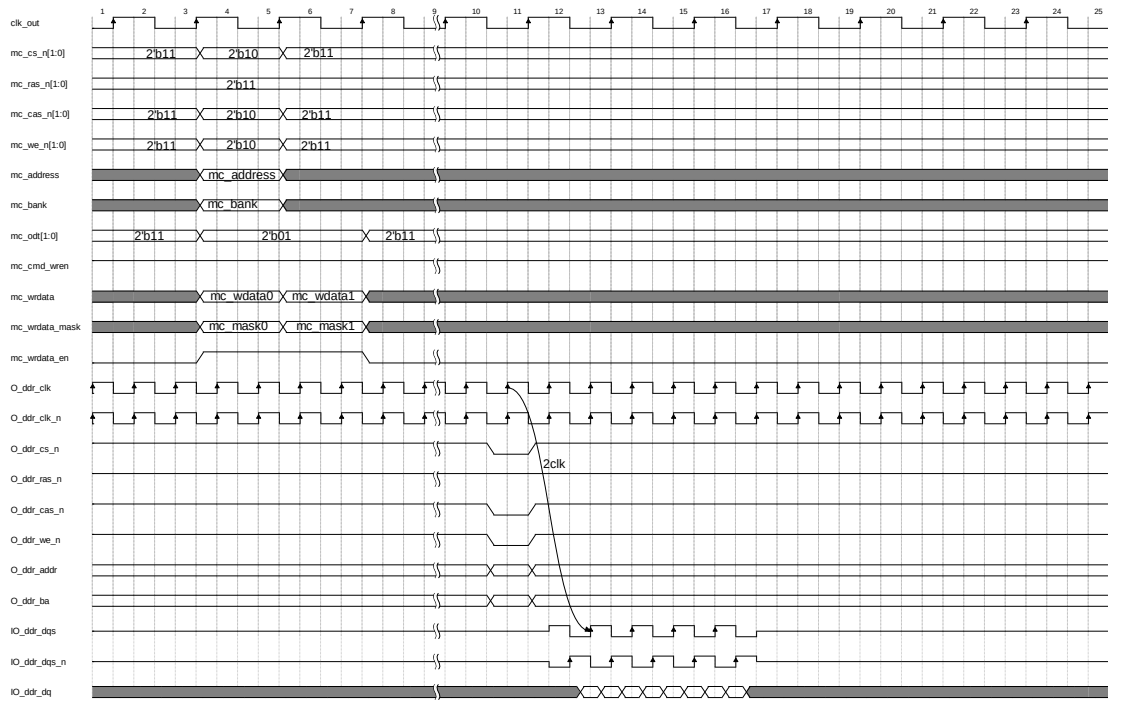
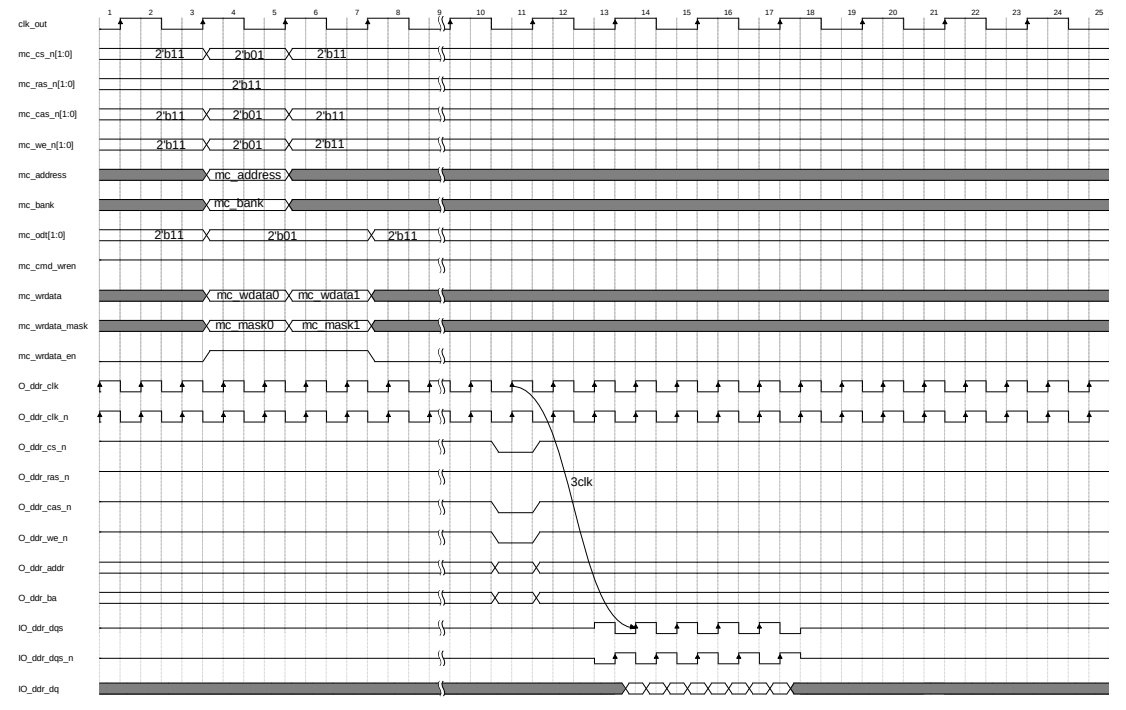
Figure 3-12 Timing Diagram for Write Data with Burst Length=8,CL=3,AL=0**Figure 3-13 Timing Diagram for Write Data with Burst Length=8,CL=4,AL=0**

Figure 3-14 Timing Diagram for Write Data with Burst Length=8, CL=5,AL=0

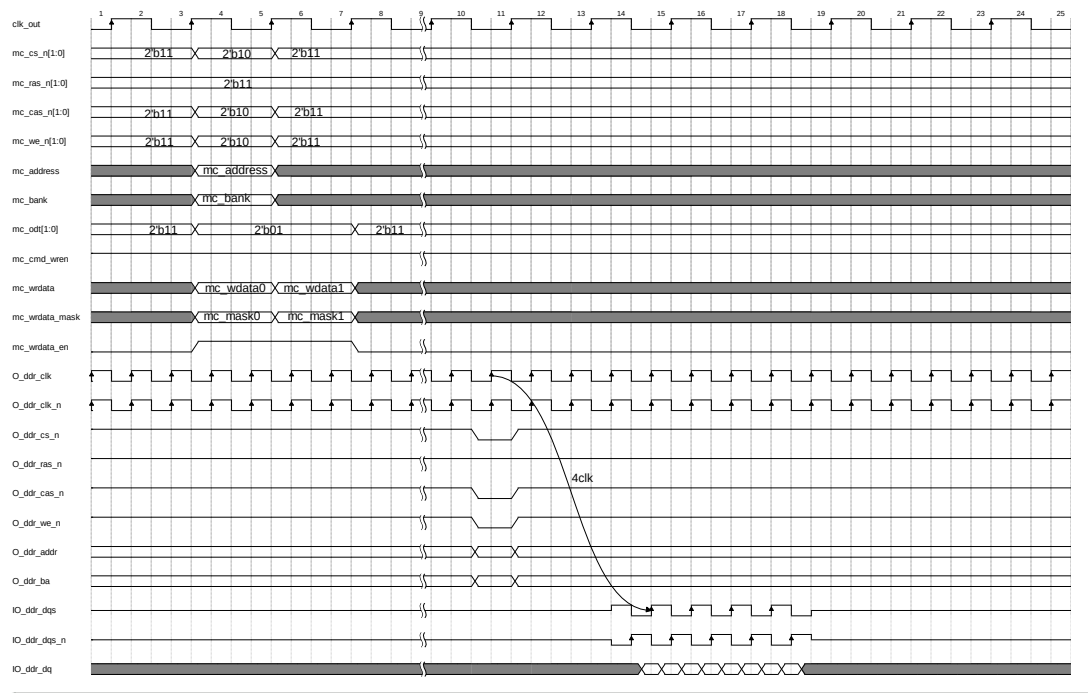


Figure 3-15 Timing Diagram for Write Data with Burst Length=8,CL=6,AL=0

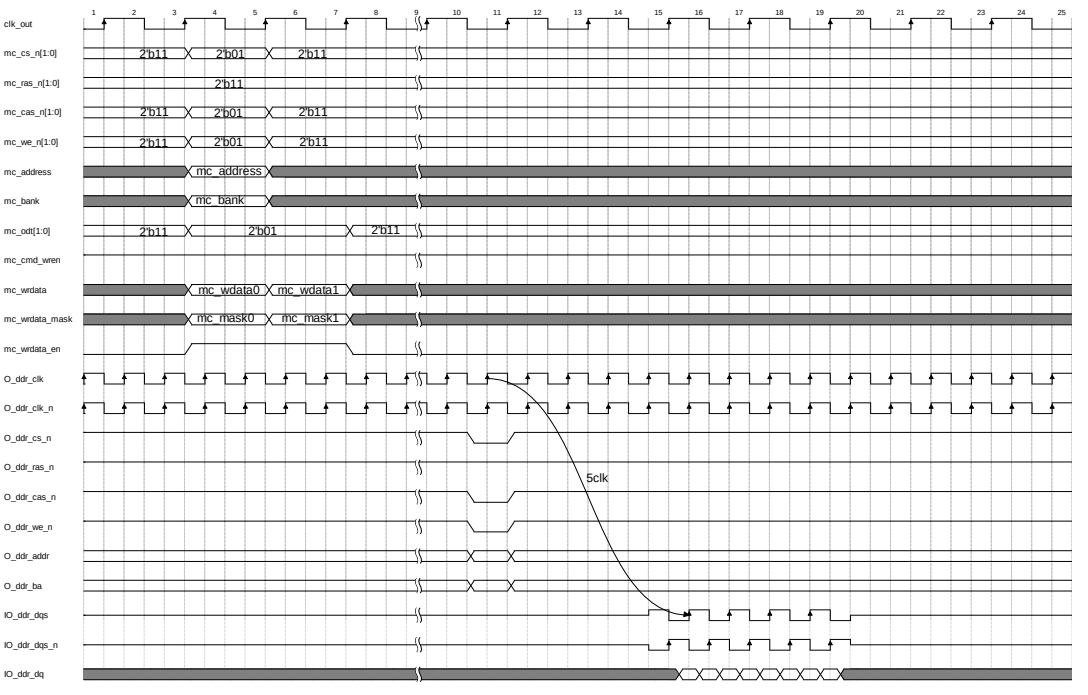
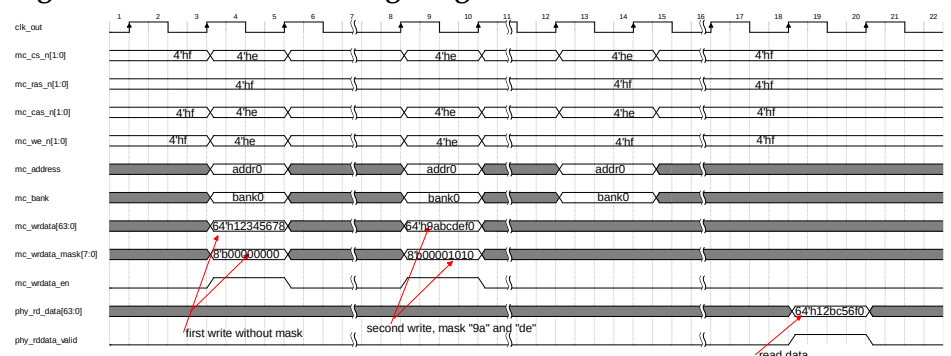


Figure 3-16 Timing Diagram for Write Data with Burst Length=4, CL=6,AL=0

Data Mask

For data that the user does not need, it can be masked by the data mask signal (`mc_wrddata_mask`). Each bit in `mc_wrddata_mask` controls one byte of `mc_wrddata`. When `mc_wrddata_mask[n] = 1'b1`, the *n*th byte of `mc_wrddata` is masked. The mapping relationship is as follows:
`mc_wrddata_mask[0]` controls `mc_wrddata[7:0]`, `mc_wrddata_mask[1]` controls `mc_wrddata[15:8]`, `mc_wrddata_mask[2]` controls `mc_wrddata[23:16]`, and so on.

As shown in Figure 3-17, two consecutive write accesses are performed to bank0, addr0. In the first write access, `mc_wrddata` is set to 64'h12345678 and `mc_wrddata_mask` is set to 8'b00000000, meaning no masking is applied. In the second write access, `mc_wrddata` is set to 64'h9abcdef0 and `mc_wrddata_mask` is set to 8'b00001010, where the 2nd and 4th bytes are masked. When a subsequent read access is performed to bank0, addr0, the data read out is 64'h12bc56f0.

Figure 3-17 Data Mask Timing Diagram

3.2.3 Write Data Timing

When sending read commands, theoretically, it is not necessary to adjust the intervals between read commands and data because the read data is returned by the DDR2 chip. It only needs to complete read calibration to obtain the data returned by the DDR2 chip. However, some of the logic for sending read and write commands inside the DDR2 PHY IP is reused, so the timing for read data on the MC interface is similar to that of write. For example, when CLK Ratio is set to 1:4, CL = 6 and AL = 0, the read commands are `mc_cs_n[3:0]=4'h7`, `mc_ras_n[3:0]=4'hf`, `mc_cas_n[3:0]=4'h7`, `mc_we_n[3:0]= 4'hf`. Since the DDR2 PHY clock ratio is 4:1, when CL=2, the timing for read data is the same as that for CL=6. The timing for read data is only provided for CL=6, and other cases are not described. When `phy_rddata_valid=1`, `phy_rd_data` is valid. The read timing diagram is as shown in Figure 3-18 and Figure 3-19.

Figure 3-18 Timing Diagram for Read Data with CLK Ratio=1:4, CL=6, AL=0

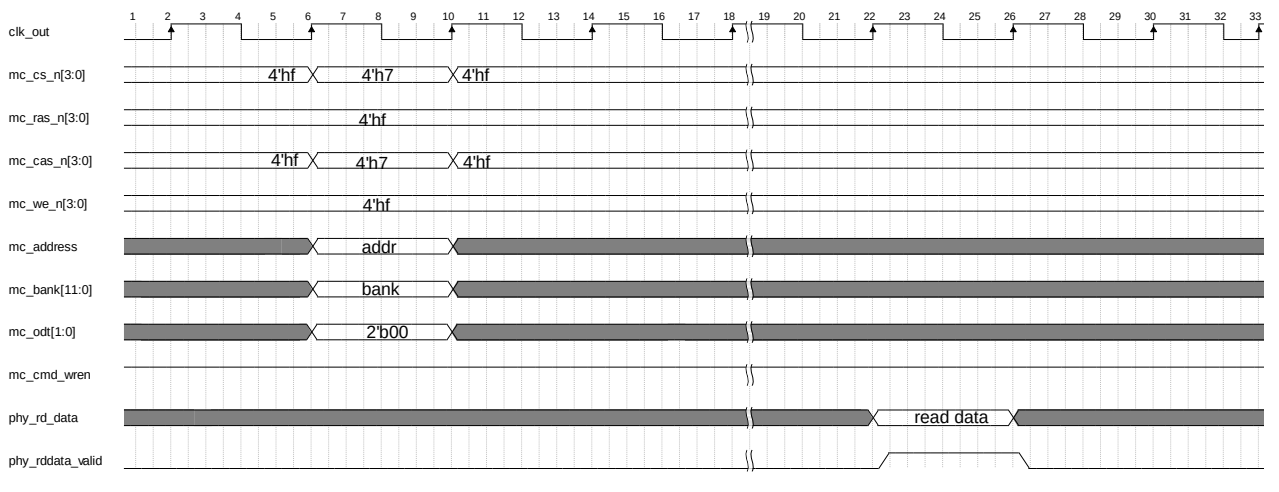
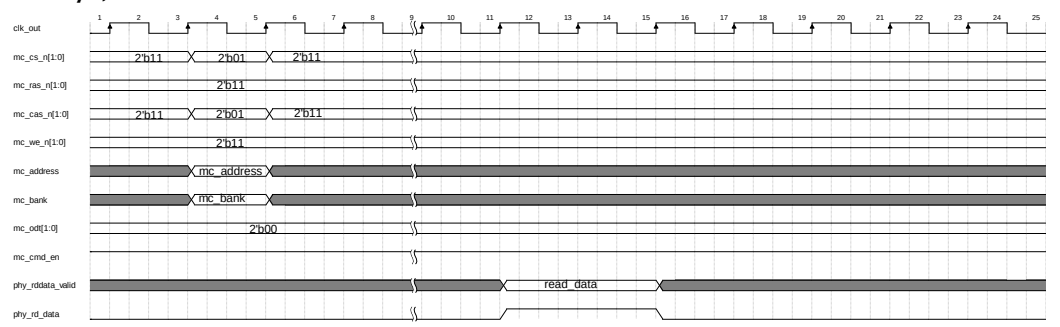
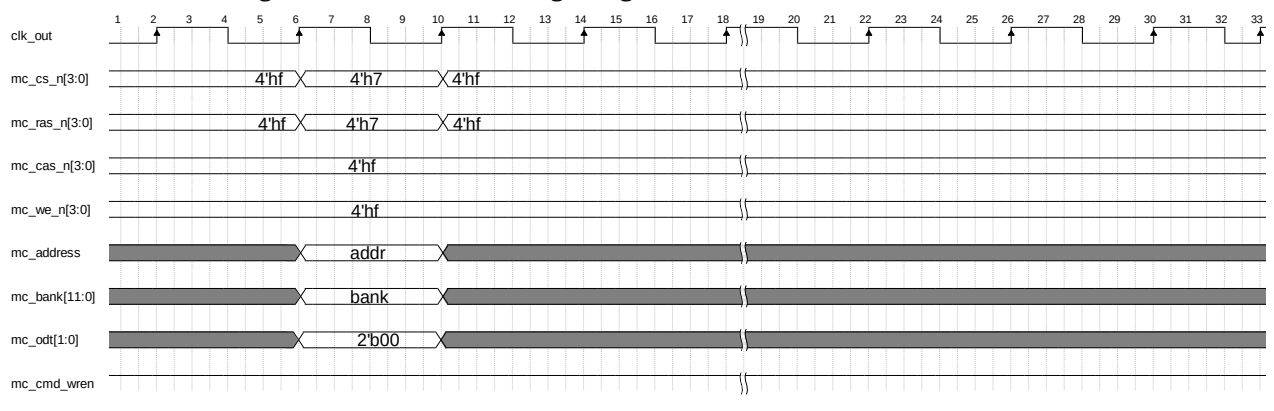


Figure 3-19 Timing Diagram for Read Data with CLK Ratio=1:2, Burst Length=8, CL=6/4, AL=0



3.2.4 Bank Active

The timing diagram for MC sending the active instruction is shown in the following figure. Users can adjust the interval between the active instruction and other instructions according to the description in section [3.2.1 User Interface](#) to improve data read and write efficiency.

Figure 3-20 Active Timing Diagram When CLK Ratio=1:4

Like other instructions of DDR2, such as Precharge, Refresh, etc., the sending format is the same as the instructions mentioned above. These instructions are not described in this manual.

3.2.5 EYE SCAN

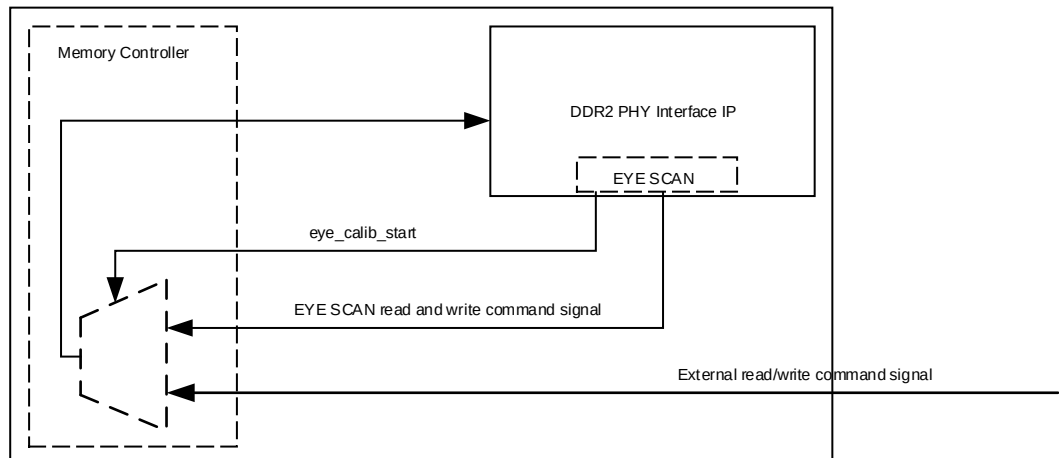
- `eye_calib_start`: Flag indicating the start of the read data window scanning. This signal remains high throughout the entire window scanning.
- `eye_cmd_rdy`: When this signal is high, it indicates that the MC can receive `eye_app_cmd_en` and `eye_app_cmd` from the EYE SCAN module.
- `eye_app_cmd_en`: When this signal is high, it indicates that `eye_app_cmd` is valid.
- `eye_app_addr`: Address for read and write data during data window scanning.
- `eye_wdf_rdy`: When this signal is high, it indicates that the MC can receive `eye_app_wdf_wren` and `eye_app_wdf_wdata`.
- `eye_app_wdf_wren`: When this signal is high, it indicates that `eye_app_wdf_wdata` is valid.
- `eye_app_wdf_wdata`: Write data during data window scanning.

The DDR2 PHY supports the read data window scanning to improve the stability of the dq data sampled by the IO LOGIC. The EYE SCAN module reads and writes data with the help of the MC layer, and the data returned by the DDR2 PHY goes directly to the EYE SCAN module of the PHY IP. The EYE SCAN module reads and writes a set of data for every adjustment of the sampling point, and then determines whether the current sampling point can sample the correct dq data through read data. When correct data is sampled for consecutive sampling points, the IP moves the sampling point to the middle of the sampling window.

The EYE_SCAN read/write instruction interface and the external read/write instruction interface need to enter a selector. When `eye_calib_start` is valid, it selects EYE SCAN read and write instruction

signals to connect to the MC. Otherwise, it selects the external read and write instruction signals to connect to the MC.

Figure 3-21 Read/Write Instruction Interface Selection



3.3 Clock, Reset, and pll _stop

See [IPUG506, Gowin DDR2 Memory Interface IP User Guide](#) for further detailed information.

4 Port List

Table 4-1 I/O List of Gowin DDR2 PHY Interface IP

No.	Signal Name	Type	Data Width	Description
User Interface				
1	clk	Input	1	Reference clock, crystal oscillator input recommended.
2	pll_stop	Output	1	Memory_clk enable signal
3	memory_clk	Input	1	This clock operates at the same frequency as the DDR2 chip interface clock. When GW2A devices are used, this clock is connected to the PLL output or other clock. When GW5A devices are used, this clock should be connected to the PLL output port clkout2, as described in section 3.3 Clock, Reset, and pll_stop .
4	pll_lock	Input	1	When this signal is high, it indicates that the memory_clk has reached a stable status. If memory_clk is connected to the PLL output clock, then this port is connected to the PLL lock pin.
5	rst_n	Input	1	System reset signal, active-low
6	mc_cs_n	Input	NCK ^[1]	Mapped to the output signal O_ddr_cs_n
7	mc_ras_n	Input	NCK	Mapped to the output signal O_ddr_ras_n
8	mc_cas_n	Input	NCK	Mapped to the output signal O_ddr_cas_n
9	mc_we_n	Input	NCK	Mapped to the output signal O_ddr_we_n
10	mc_address	Input	NCK *ROW_WIDTH ^[1]	Mapped to the output signal O_ddr_addr
11	mc_bank	Input	NCK *BANK_WIDTH ^[2]	Mapped to the output signal O_ddr_bank
12	mc_reset_n	Input	1	Keep this signal high in the user

No.	Signal Name	Type	Data Width	Description
				logic
13	mc_odt	Input	2	Mapped to the output signal O_ddr_odt
14	mc_cke	Input	4	Mapped to the output signal O_ddr_cke
15	mc_wrdata_en	Input	1	mc_wrdata enable signal, active-high.
16	mc_wrdata	Input	NCK *2*DQ_WIDTH ^[3]	The data stored in memory, mapped to the signal IO_ddr_dq to output
17	mc_wrdata_mask	Input	NCK *2*DM_WIDTH ^[4]	The data mask input, mapped to the output signal O_ddr_dqm
18	mc_cmd_wren	Input	1	The enable signals for mc_cs_n, mc_ras_n, mc_cas_n, mc_we_n, mc_address, mc_bank, mc_odt, and mc_cke, active-high. Users are required to keep this signal high.
19	clk_out	Output	1	User Clock; When CLK Ratio is set to 1:4, the frequency is one-fourth of the memory clock (memory_clk). When CLK Ratio is set to 1:2, the frequency is one-half of the memory clock (memory_clk).
20	ddr_rst	Output	1	IP reset output; and it is generally not recommended for use as user logic reset.
21	phy_rddata_valid	Output	1	phy_rd_data valid signal, active-high.
22	phy_rd_data	Output	NCK *2*DQ_WIDTH	Data read from DDR2
23	init_calib_complete	Output	1	Initialization completed signal, active-high.
24	eye_calib_start	output	1	Window scan enable, command, and data signals; for details, refer to Section 3.2.5 EYE SCAN.
25	eye_cmd_rdy	Input	1	
26	eye_app_cmd_en	Output	1	
27	eye_app_cmd	Output	3	
28	eye_app_addr	Output	[ADDR_WIDTH ^[5] -1:0]	
29	eye_wdf_rdy	Input	1	
30	eye_app_wdf_wren	Output	1	
31	eye_app_wdf_wdata	Output	[APP_DATA_WID TH ^[6] -1:0]	
DDR2 SDRAM Interface				
29	O_ddr_addr	Output	ROW_WIDTH	PHY interface signal; ROW/Column address signal lines
30	O_ddr_ba	Output	BANK_WIDTH	PHY interface signal; bank signal line

No.	Signal Name	Type	Data Width	Description
31	O_ddr_cs_n	Output	1	PHY interface signal, chip selected signal line
32	O_ddr_ras_n	Output	1	PHY interface signal; row address selected signal line
33	O_ddr_cas_n	Output	1	PHY interface signal; column address selected signal line
34	O_ddr_we_n	Output	1	PHY interface signal; write enable signal line
35	O_ddr_clk	Output	1	PHY interface signal; clock differential signal line P
36	O_ddr_clk_n	Output	1	PHY interface signal; clock differential signal line N
37	O_ddr_cke	Output	1	PHY interface signal; clock enable signal line
38	O_ddr_odt	Output	1	PHY interface signal; termination resistor control signal line
39	O_ddr_reset_n	Output	1	PHY interface signal; DDR3 chip reset signal line
40	O_ddr_dqm	Output	DM_WIDTH	PHY interface signal; dq data mask signal line
41	IO_ddr_dq	Inout	DQ_WIDTH	PHY interface signal; dq signal line
42	IO_ddr_dqs	Inout	DQS_WIDTH ^[8]	PHY interface signal; dqs signal line P
43	IO_ddr_dqs_n	Inout	DQS_WIDTH	PHY interface signal; dqs signal line N

Note!

- ^[1] NCK: Clock ratio parameter. When CLK_Ratio is set to 1:4, NCK = 4; when set to 1:2, NCK = 2.
- ^[2] ROW_WIDTH: Row address width of the DDR2 chip.
- ^[3] BANK_WIDTH: Bank address width of the memory.
- ^[4] DQ_WIDTH: Dq data width.
- ^[5] DM_WIDTH: Dqm data width, calculated as DQ_WIDTH/8.
- ^[6] ADDR_WIDTH: Input address width (RANK_WIDTH + BANK_WIDTH + ROW_WIDTH + COL_WIDTH ^[9], with RANK_WIDTH=1).
- ^[7] APP_DATA_WIDTH: User interface data width, calculated as NCK*2*DQ_WIDTH.
- ^[8] DQS_WIDTH: Dqs data width, calculated as DQ_WIDTH/8.
- ^[9] COL_WIDTH: Column address width of the memory

5 Call and Configure

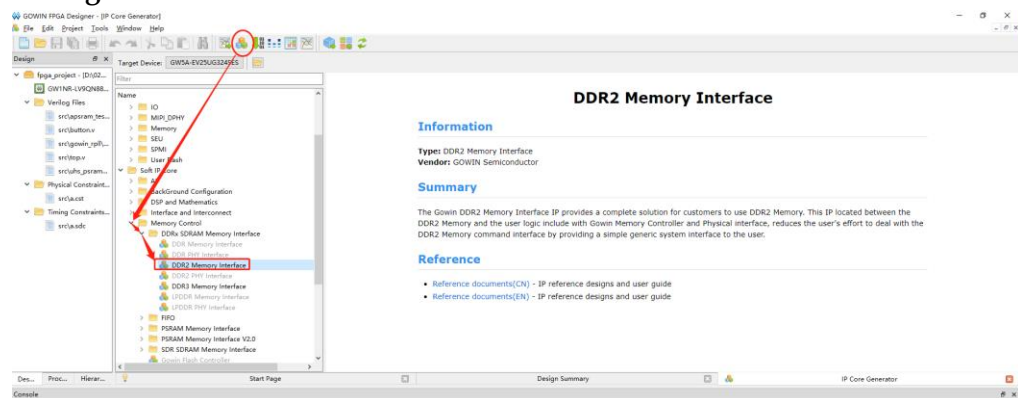
5.1 IP Generation

Click on the shortcut " " or "Tools > IP Core Generator" on the menu bar in Gowin Software to call and configure Gowin DDR2 PHY Interface IP.

1. Open IP Core Generator.

After creating a new project, click "IP Core Generator" to open the IP Core Generator, as shown in Figure 5-1.

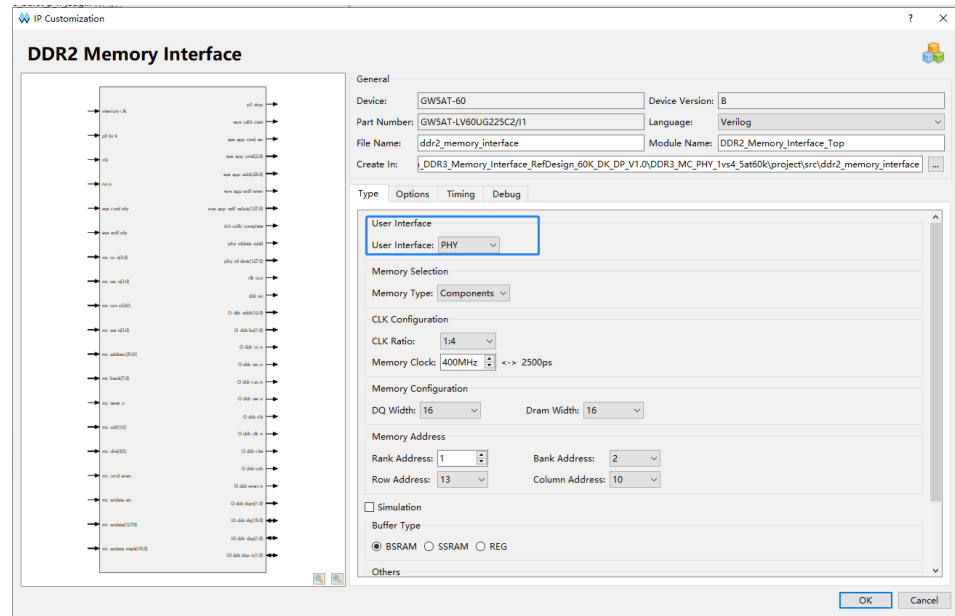
Figure 5-1 IP Core Generator Interface



2. Open Gowin DDR2 PHY Interface IP

Double click "Soft IP Core > Memory Control > DDRx SDRAM Memory Interface > DDR2 Memory Interface" to open the DDR2 Memory Interface IP interface, as shown in Figure 5-2; select "PHY" in "User Interface" option to open this IP.

Figure 5-2 DDR2 PHY Interface Configuration Interface

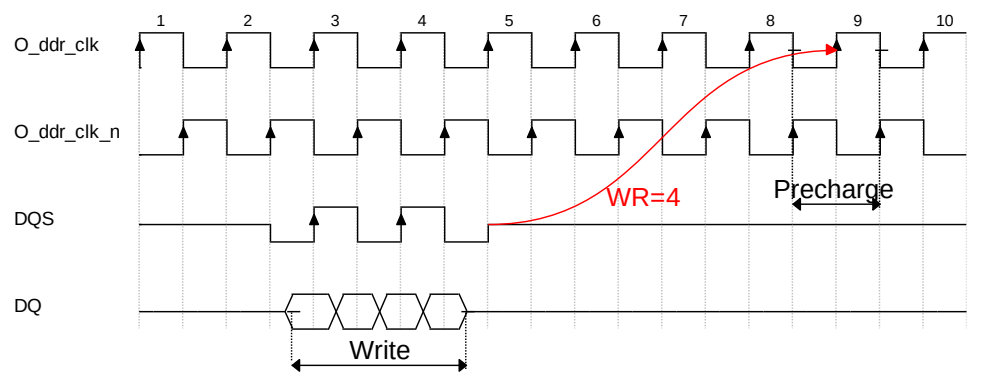


- You can configure the generated file name by modifying "File Name".
- You can configure the top module name by modifying "Module Name".
- You can configure other options by modifying "Options".

5.2 Parameter Configuration

- **Memory Type:** The memory types supported by the IP, including Components and DIMMs (RDIMMs, UDIMMs, SODIMMs). DIMMs are only supported under single-Rank memory modules.
- **Memory Clock:** The interface clock frequency of the memory chip. It is set according to the operational frequency of the memory chip.
- **CLK Ratio:** The ratio between the user interface clock and the memory interface clock. 1:4 and 1:2 are supported.
- **DQ Width:** Total DQ data width. 8, 16, 24, 32, 40, 48, 56, and 64 values are supported. For example, if two memory chips are used, each is with a DQ width of 16, then DQ Width should be set to 32.
- **Dram Width:** Data width of signal memory chip. 8 or 16 values are supported.
- **Rank Address:** The value is fixed to 1. The IP does not support Rank address, so this parameter has no effect.
- **Bank Address:** The width of the Bank address for the memory chip. 2 or 3 values are supported.

- Row Address: The Row address width of the memory chip. 12, 13, 14, 15, or 16 values are supported.
- Column Address: The Column address width of the memory chip. 9 or 10 values are supported.
- Sim: Used to accelerate simulation. Check this option to accelerate simulation. It is not needed during board-level testing.
- Buffer Type: The hardware resource used for data buffer inside the IP. BSRAM, SSRAM, or REG are supported.
- ADDR Width: User interface address width (read-only). It is the sum of Rank Address + Bank Address + Row Address + Column Address. This parameter cannot be modified by the user. The highest bit (Rank Address) is unused and should be fixed to 0.
- Data Width: User interface data width. When CLK Ratio is set to 1:4, the width is 8*DQ Width; when CLK Ratio is set to 1:2, the width is 4*DQ Width.
- Mask Width: Data mask width, calculated as Data Width/8.
- Burst Mode: Burst mode. When CLK Ratio is set to 1:4, this is fixed to 8 (BL8); when CLK Ratio is set to 1:2, it supports 4 (BL4) or 8. For related user interface timing, see [3.2.2 Write Data Timing](#) and [3.2.3 Write Data Timing](#).
- Burst Type: Burst type. Options include SEQ (sequential burst) or INT (interleave burst).
- CAS Latency: Latency between command and data, referred to as CL. 2, 3, 4, 5, or 6 values are supported. Users should select an appropriate CL value according to the datasheet of the selected memory chip.
- Additive Latency: Additive latency, abbreviated as AL. 0, 1, 2, 3, 4, or 5 values are supported. DDR2 supports Posted CAS, which improves efficiency when there is a timing conflict between the Active command and the Read/Write command; $AL = tRCDmin - 1$.
- Write Recovery (WR): 2, 3, 4, 5, or 6 values are supported. This parameter defines the minimum number of clock cycles that must elapse between the completion of a valid write operation in an active Bank and the issuance of a Precharge command. As illustrated in Figure 5-3, if WR=4, a Precharge command can only be issued after waiting for 4 clock cycles following the completion of the write operation.

Figure 5-3 WR Timing Diagram when WR=4

- **Rtt Nom:** Configures the on-die termination resistance of the DDR2 device. OFF, 75, 150, and 50 ohms values are supported. Ideally, the impedance along the physical link from the source (FPGA) to the destination (DDR2) should be continuous. Therefore, the Rtt_Nom value should match the characteristic impedance of the PCB trace.
- **OUTPUT DRV:** Output drive strength control. Full strength or Reduced strength are supported. This parameter is used to configure the output drive strength for the DQS and DQ signals of the DDR2 device. The IP is set to Full strength by default. When it is set to Reduced strength, the output drive strength of the DQS and DQ signals is lower than that of Full strength. This setting affects signal integrity, and users may adjust it if data errors occur.
- **DDR2 DQSN Enable:** Enables the IO_ddr_dqs_n port.

Table 5-1 DDR2 Time Parameter

Option	Description
t _{CKE}	Minimum pulse time of CKE signal (ps)
t _{FAW}	Allowing more than four row activation commands to be sent simultaneously within the same rank, the minimum interval should not be less than four times t _{RRD} .
t _{RAS}	Time from ACTIVE to PRECHARGE
t _{RCD}	Time from ACTIVE to READ or WRITE
t _{REFI}	Memory refresh interval
t _{RFC}	The interval from REFRESH to ACTIVE/REFRESH
t _{RP}	PRECHARGE period
t _{RRD}	The interval from ACTIVE to ACTIVE between different Banks
t _{RTP}	The interval from READ to PRECHARGE
t _{WTR}	The interval from WRITE to READ
t _{RC}	The interval from ACTIVE to ACTIVE within the same Bank
t _{DLLK}	DLL locking time

