



Arora V SEU Handler

User Guide

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Revision History

Date	Version	Description
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1 About This Guide

1.1 Purpose

The Arora V SEU Handler User Guide mainly include the SEU Handler structure, ports, user timing and the configuration information.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1114, GW5AS Data Sheet](#)
- [DS1105, GW5AS-25 Data Sheet](#)
- [DS1104, GW5AST series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Full Name
CRC	Cyclic Redundancy Check
ECC	Error Correction Code
SER	Soft Error Recovery
SEU	Single Event Upset

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

The SEU Handler module integrated in GOWINSEMI's Arora V FPGA products features Configuration Memory Soft Error Recovery. It detects the possible soft errors by continuously monitoring the configuration memory and attempts to correct them within its capabilities. While the FPGA is working, it reads the configuration data frame by frame from the background and performs ECC decoding and CRC checksum comparison to detect errors. If the error can be corrected, the calculated error-corrected data bits are rewritten to the SRAM.

The SEU Handler module functions and features are as follows:

- Based on ECC and CRC detection and correction algorithms
- CRC can report any number of bit errors during configuration of the SRAM.
- ECC supports 2-bit error location report and error correction^[1] and 4-bit error alarm in each SRAM Frame. 138K devices support 1-bit error location report and error correction and 2-bit error alarm in each 64-bit SRAM Frame.
- Can be enabled or disabled by user logic or enabled automatically upon program wakeup.
- Supports single bit error injection by user logic for the functional verification and evaluation.
- Supports faster error correction^[1].

Note!

^[1] SEU Handler can support faster error correction. Please contact local technical support for details.

3 Module Description

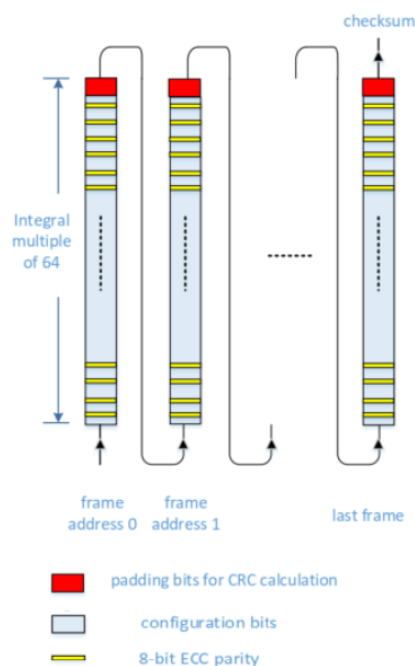
3.1 SEU Handler IP Overview

Table 3-1 SEU Handler IP Overview

Gowin SEU Handler IP	
Devices Supported	GW1NR series GW1NS Series GW1NS Series GW1NS Series GW1NS Series
Delivered Doc.	
Design Files	Verilog (encryption)
Reference Design	Verilog
TestBench	
Test and Design Flow	
Synthesis Software	GowinSynthesis®
Application Software	Gowin Software (V1.9.9.01 and above)

3.2 SEU Handler Structure

Figure 3-1 Arora V Configuration Frame Structure



When ECC is enabled, the SEU Handler module reads back the data configured into the SRAM frame by frame. Within each 72-bit data block, a (72, 64) Hamming code decoding operation is run for single bit error correction and two-bit error detection. In this process, single bit errors can be corrected and the corrected data can be rewritten back into the configuration SRAM; 2-bit errors within a data block can only be detected and reported while a CRC check and calculation is performed. This CRC calculation encompasses the entire SRAM frame data. When the readback of all configuration frames is complete, the calculated CRC check value will be compared to the loaded golden value and any mismatches will be reported. The mismatches mean that there are error bits in the configuration SRAM process.

The SEU Handler supports error injection and two working modes: AUTO and UserLogic. In AUTO mode, the FPGA starts to run the detection and error correction automatically after it's configured and waked up. In UserLogic mode, the SEU Handler can be enabled or disabled by user logic.

3.3 Port Diagram

Figure 3-2 138K SEU Handler Port Diagram

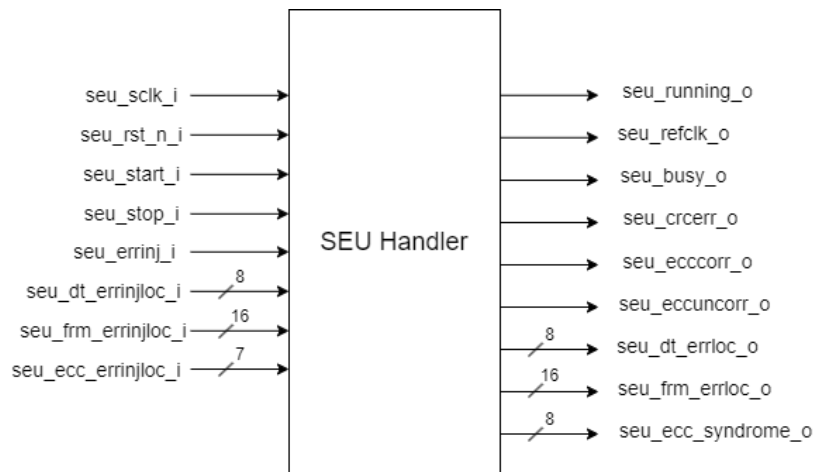
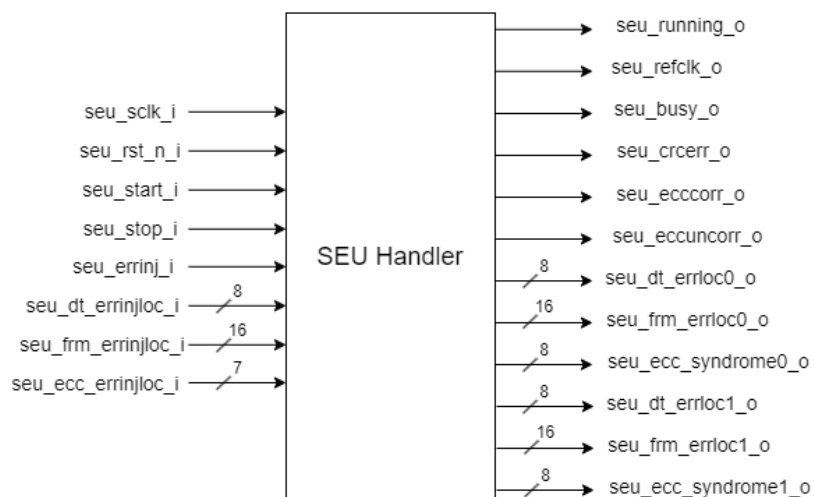


Figure 3-3 25K SEU Handler Port Diagram



3.4 Port Description

Table 3-2 SEU Handler Port Description

Port	I/O	Data Width	Description
seu_sclk_i	Input	1	Clock input
seu_rst_n_i	Input	1	reset input, active-low
seu_start_i	Input	1	Enable SEU Handler at rising edge
seu_stop_i	Input	1	Dsiable SEU Handler at rising edge

Port	I/O	Data Width	Description
seu_errinj_i	input	1	A single-cycle high pulse indicates that an error needs to be injected into the ECC module; this pulse must align with the address information of the injected error within the same clock cycle.
seu_dt_errinjloc_i	input	8	The position of the data block where an error is injected.
seu_frm_errinjloc_i	input	16	The position of the SRAM frame where an error is injected.
seu_ecc_errinjloc_i	input	7	The location of error injection within the ECC block.
seu_running_o	output	1	High indicates that the SEU Handler is running (the state machine is in the IDLE state)
seu_crcerr_o	output	1	A one-cycle high pulse indicates that a CRC error has occurred
seu_ecccorr_o	output	1	A one-cycle high pulse indicates that an ECC error has been corrected
seu_eccuncorr_o	output	1	A one-cycle high pulse indicates that a non-correctable ECC error
seu_dt_errloc_o	output	8	The address of the data block with ECC errors
seu_frm_errloc_o	output	16	The address of the SRAM frame with ECC errors
seu_ecc_syndrome_o	output	8	ECC errors contain the error number and locations
seu_busy_o	output	1	During ECC module error injection and correction, manual error injection functionality is disabled.
seu_refclk_o	output	1	The reference clock used to generate SEU Handler for user designs.

Devices of different sizes have different address ranges, and the range of locations for injection errors is shown in Table 3-3.

Table 3-3 Range of Injection Error Locations for Different Devices

Device	_dt_errinjloc_i[1]	_frm_errinjloc_i[1]	_ecc_errinjloc_i[1]
GW5A-25 ^[1]	0~'d7	0~'d11071	0_nnnnnn: 64-bit ECC data address For example: 0_000000: the ECC data bit[0] 0_111111: the ECC data bit[63]
GW5A-138	0~'d23	0~'d21871	1_xxxnnn: 8-bit parity address (x: "don't care") For example: 1_xxx000: the ECC parity bit[0] 1_xxx111: the ECC parity bit[7]

Note!

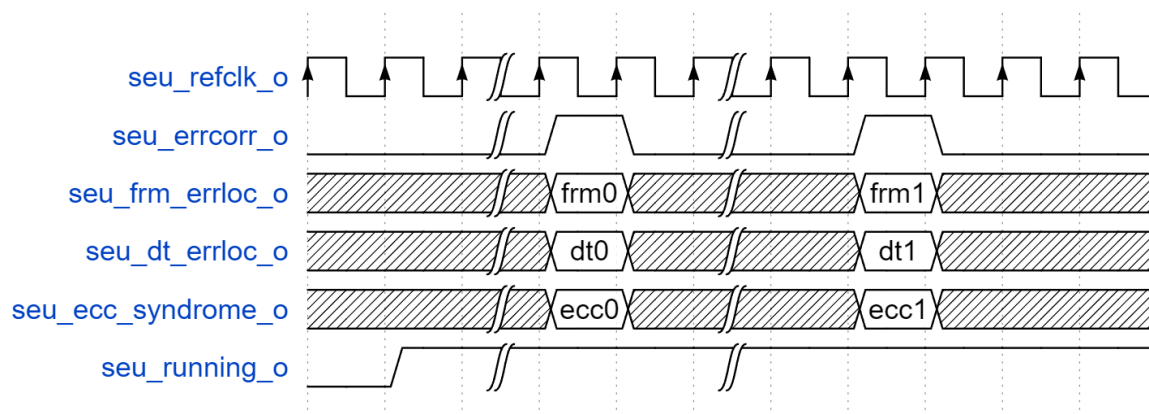
^[1] The GW5A-25 outputs are 2 sets of error position messages, and the interface definition is consistent with that of the GW5A-138K.

3.5 User Design Timing

3.5.1 Error Detection in Progress

When the SEU Handler module detects ECC errors in the scanned SRAM data, the output port "seu_ecccorr_o" signal will be set to 1. Each pulse corresponds to one error. Within the same pulse cycle, the error location is reported through "seu_dt_errloc_o," "seu_frm_errloc_o," and "seu_ecc_syndrome_o". After setting "seu_ecccorr_o" to 1, the SEU module will correct 1-bit errors that are correctable.

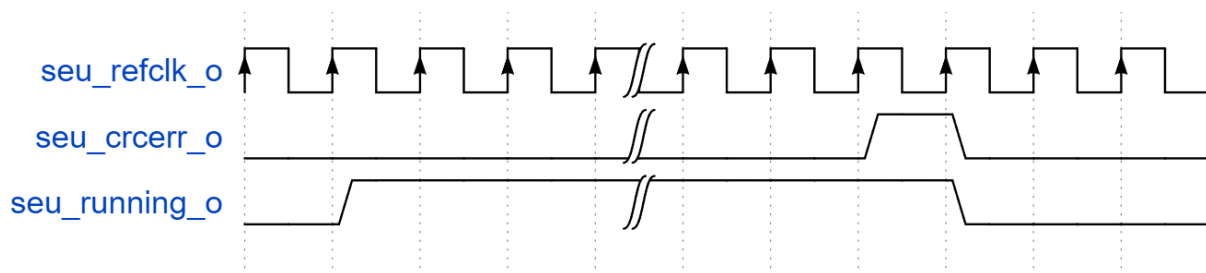
Figure 3-4 ECC Timing Diagram



3.5.2 Stop Working When an Uncorrectable Error is Detected

The SEU module stops after detecting an uncorrectable ECC or CRC error. It will stop at the end of a frame and pull the RUNNING signal low.

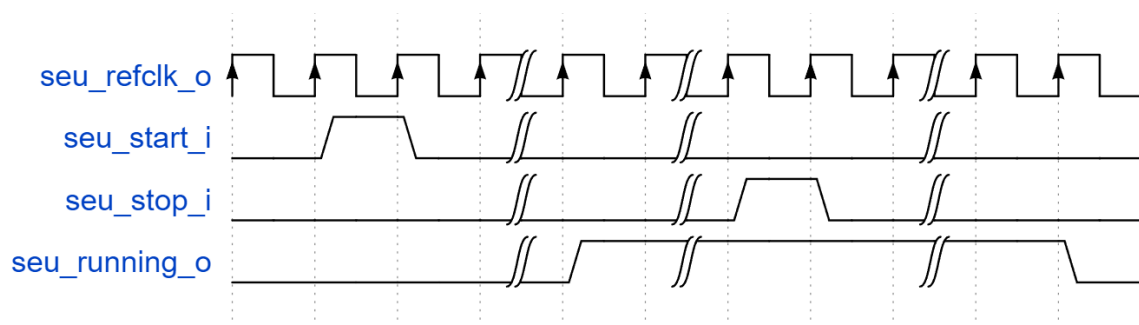
Figure 3-5 Timing Diagram of SEU Handler Stopping Working When an Uncorrectable Error is Detected



3.5.3 Start / Stop Working by UserLogic

The signals "seu_start_i" and "seu_stop_i" can be used to start or stop the SEU Handler operation. The signal "seu_running_o" is 1 when it starts working and 0 when it stops. The timing reference is as shown in Figure 3-6.

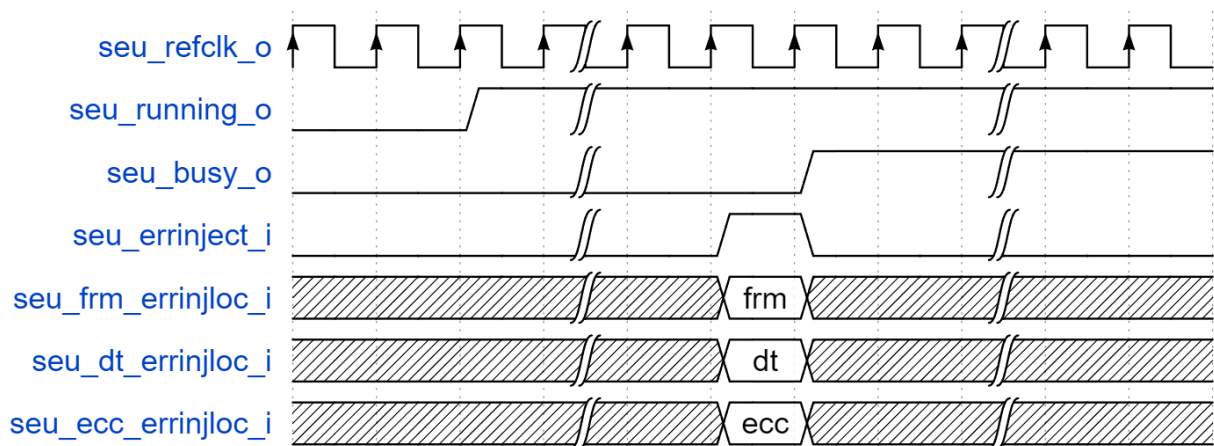
Figure 3-6 Timing Diagram of SEU Handler Stopped by User Logic



3.5.4 Injecting Errors by User Logic

When the "user_logic" mode is enabled, users can inject errors into the configuration bits by generating "seu_errinj_i" pulses through logic. The user can specify the error injection address via "seu_dt_errinjloc_i," "seu_frm_errinjloc_i," and "seu_ecc_errinjloc_i" signals.

Figure 3-7 SEU Handler Error Injection Timing



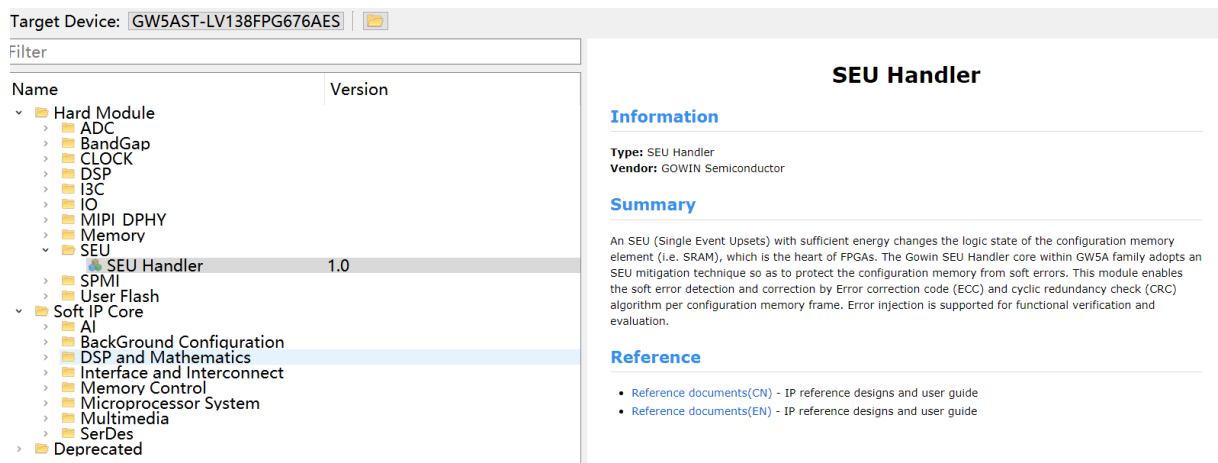
4 Interface Configuration

You can use the IP core generator tool in Gowin Software to call and configure the SEU Handler IP. The functional options of the SEU Handler IP can be configured through the Project -> Configuration -> sysControl interface.

4.1 SEU Handler IP Instantiation

After creating the project, click the "Tools" tab in the upper left, select and open the IP Core Generator from the drop-down list, or click the "IP Core Generator" icon on the toolbar to open the Gowin IP Core Generator, as shown in Figure 4-1.

Figure 4-1 Gowin IP Core Generator Interface

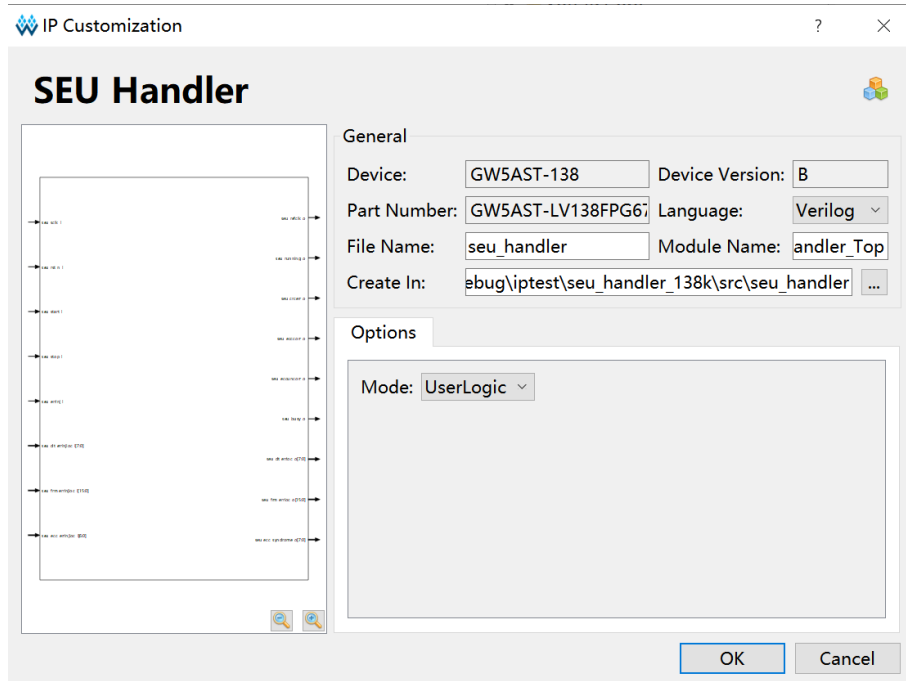


In the Gowin IP Core Generator interface, click "Hard Module"->"SEU"->"SEU Handler" to open the SEU Handler IP instantiation interface, as shown in Figure 4-2.

Mode: Both "UserLogic" and "Auto" modes are supported. UserLogic: With UserLogic control, users can implement functions such as error injection, enabling/disabling the SEU Handler, and more. Auto: The SEU Handler runs automatically.

Note that the Mode selected here must be consistent with the Mode option of the function configuration in section 4.2, otherwise it will result in a mismatch with what is expected.

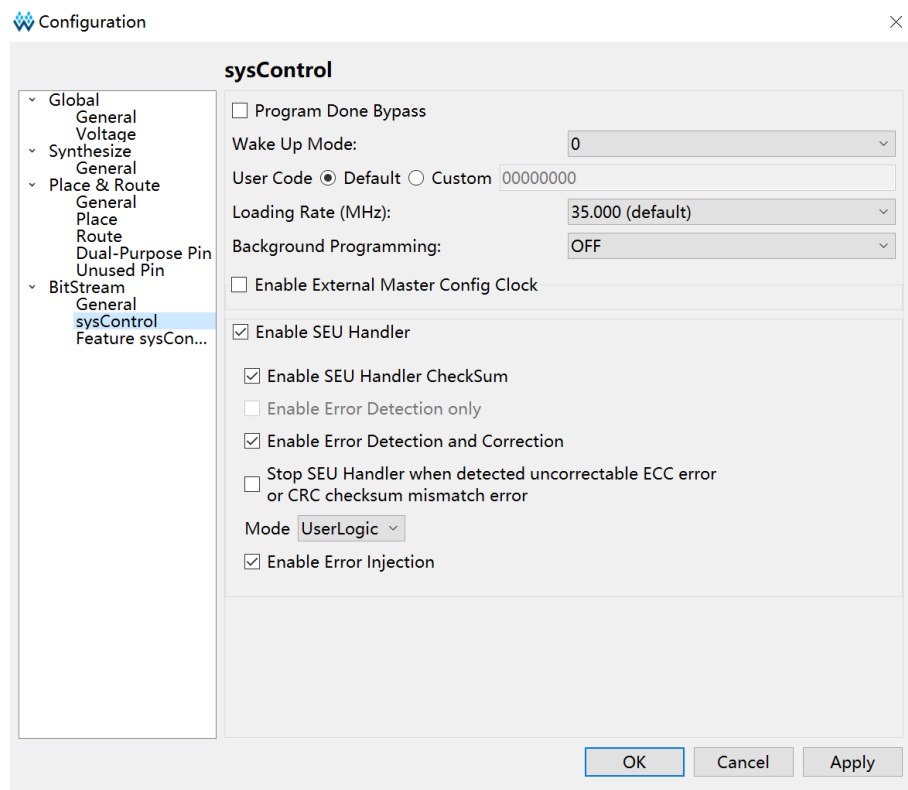
Figure 4-2 SEU Handler IP Customization Interface



4.2 SEU Configuration

After the SEU Handler IP instantiation is completed, click Project->Configuration->sysControl to open the SEU Handler IP configuration interface, as shown in Figure 4-3.

Figure 4-3 SEU Handler IP Configuration Interface



Main functions:

- Enable SEU Handler:
Check to enable the SEU Handler.
- Enable SEU Handler CheckSum:
Check to enable the CRC function in the SEU Handler.
- Enable Error Detection Only:
Check to enable the error detection Only.
- Enable Error Detection and Correction:
Check to enable the error detection and correction.
- Stop SEU Handler when detected uncorrectable ECC error or CRC checksum mismatch error:

When checked, the SEU Handler module will stop if an uncorrectable ECC error or CRC checksum mismatch error is detected.

- Mode:AUTO / UserLogic.

ATUO: When "AUTO" is selected, the SEU Handler will run automatically after the chip is wake-up, without the intervention of the user's logic control.

UserLogic: When "UserLogic" is selected, the user logic controls the functions of the SEU Handler module, such as starting, stopping and manual error injection. Check to enable the manual error injection.

Note!

Note that the Mode selected here must be consistent with the Mode option of the function configuration in 4.1, otherwise it will result in a mismatch with what is expected.

