



Gowin QSGMII IP

User Guide

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Revision History

Date	Version	Description
02/23/2024	1.0E	Initial version published.
10/25/2024	1.1E	● A reset signal added to Management function. ● The reset scheme modified. ● GW5AT-60 devices supported. ● "AFE" configuration added.
02/28/2025	1.2E	The SerDes reset solution fixed, allowing users to perform reset operation on both the PMA and PCS.
05/23/2025	1.3E	● GW5AT-15 devices supported and related descriptions added. ● AFE description added.

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1 About This Guide

1.1 Purpose

The purpose of Gowin QSGMII IP User Guide is to help you learn the features and usage of Gowin QSGMII IP by providing the descriptions of functions, GUI, and reference design, etc. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.11.02 (64-bit). As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at www.gowinsemi.com:

- [SUG100, Gowin Software User Guide](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
AFE	Analog Front End
CRC	Cyclic Redundancy Check

Terminology and Abbreviations	Meaning
FCS	Frame Check Sequence
FFE	Feed-Forward Equalization
IFG	Inter-Frame Gap
IP	Intellectual Property
LUT	Look-up Table
MAC	Media Access Control
PCS	Physical Coding Sublayer
QSGMII	Quad Serial Gigabit Media Independent Interface
SFD	Start of Frame Delimiter
SGMII	Serial Gigabit Media Independent Interface

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

Gowin QSGMII IP implements a solution that combines four SGMII (Serial Gigabit Media Independent Interface) interfaces into a single 5Gb/s interface, while also complying with the QSGMII (Quad Serial Gigabit Media Independent Interface) specification. This IP is designed for communication applications and helps save pin resources.

Table 2-1 Gowin QSGMII IP

Gowin QSGMII IP	
Logic Resource	See Table 2-2.
Delivered Doc.	
Design Files	Verilog (encryption)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9.01 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.1 Features

- Supports QSGMII specification
- SGMII supports 10/100/1000M
- Optional Ethernet MAC for users
- Supports full duplex and half duplex, and collision detection in half duplex mode
- Users can select to automatically add and verify CRC or not
- Can add pad automatically
- Supports Ethernet frame classification statistics
- Supports Ethernet frame error statistics
- Supports IFG configurable function
- Supports Jumbo mode

- Supports Flow Control in full duplex mode
- Supports Management interface mdc, mdio

2.2 Operating Frequency

Gowin QSGMII IP operates at 125 MHz.

2.3 Resource Utilization

Gowin QSGMII IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW5AT series of FPGA as an instance, the resource utilization is as shown in Table 2-2. For the resource utilization of other devices, please refer to later release information.

Table 2-2 Resource Utilization

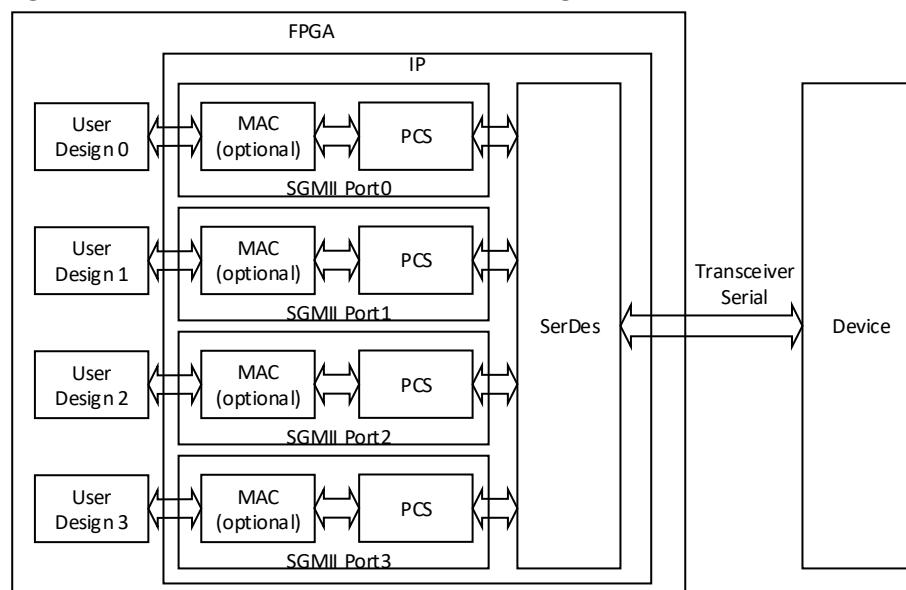
Interface	LUTs	REGs	Device	Speed
MAC Layer	6531	6207	GW5AT-138	ES
PHY Layer	2419	1943	GW5AT-138	ES
PHY Layer (MIIM)	2932	2235	GW5AT-138	ES

3 Functional Description

3.1 Structure

The basic structure of Gowin QSGMII IP is as shown in Figure 3-1, mainly consisting of four SGMII interfaces and a SerDes. Each SGMII interface includes an optional MAC (Media Access Controller) and PCS (Physical Coding Sublayer). The User Design in Figure 3-1 is the User Design in FPGA, and the Device is an externally connected Ethernet device supporting QSGMII.

Figure 3-1 Gowin QSGMII IP Structure Diagram



- SGMII: Implements the functions of both the Ethernet MAC layer and PCS layer.
 - MAC: Converts user data format to Ethernet frame data format, supports CRC, PAD, Flow Control, IFG configuration, frame statistics, error indication, and other functions.
 - PCS: Implements GMII, auto-negotiation, replacement between K28.5 and K28.1 (only for Port0), TX I1 only, and other functions.

- SerDes: Realizes the processing of Ethernet data coding and decoding, serial and parallel conversion, etc.

3.2 IP Reset

The user can perform a global reset operation on Gowin QSGMII IP through the `rstn_i` signal. When `rstn_i` is set to 0, the reset function is triggered.

The reset duration for Gowin QSGMII IP should be configured according to the actual requirements, and the reset operation should last at least until the reference clock output stabilizes.

3.3 User Interface

The IP supports 4 SGMII interfaces, each interface supporting optional MAC layer functions and three selections of speed; for each SGMII interface, the speed, IFG configuration, and Flow Control can be independently configured. Except for the optional MAC layer functions, PHY layer MIIM functions, and MIIM clock division factors can not be configured independently.

The port names for the four SGMII interfaces are differentiated as "ch0," "ch1," "ch2," and "ch3," corresponding to Port0~Port3. For simplicity, "chx" will be used to represent the corresponding portion of the port name in the following descriptions.

3.3.1 Configuration Interface

Mode Configuration

The SGMII includes System Mode and Media Mode. In System Mode, the current rate and duplex mode of the SGMII are determined by the Ethernet device connected externally, which supports three rates of 10M, 100M and 1000M, and full-duplex and half-duplex mode; In Media Mode, the current rate and duplex mode of SGMII can be set, and the supported rates and duplex modes are the same as those in System Mode.

When the user sets `sgmii_mode_chx_i` to 0, SGMII is System Mode, and there is no need to set the rate and duplex mode; when the user sets `sgmii_mode_chx_i` to 1, SGMII is Media Mode, and the rate and duplex mode can be set through `configuration_vector_chx_i[13:11]`. For duplex mode, when `configuration_vector_chx_i[13]` is 1, it means SGMII is full duplex, and when `configuration_vector_chx_i[13]` is 0, it means SGMII is half duplex; for rate, when `configuration_vector_chx_i[12:11]` is 1X, it means SGMII rate is 1000M for transmission; when `configuration_vector_chx_i[12:11]` is 01, it means SGMII rate is 100M for transmission; when `configuration_vector_chx_i[12:11]` is 00, it means SGMII rate is 10M for transmission.

Users can also control the SGMII link time by setting `sgmii_link_timer_chx_i`. The specific link time can be calculated using the following formula:

$$\text{Link time} = \text{sgmii_link_timer_chx_i} * 32.769\mu\text{s}$$

Note!

The SGMII link time is 1.6ms.

Function Configuration

When the user configures `repeater_mode_chx_i` as 1, SGMII can be set to repeater mode. The user can configure `configuration_vector_chx_i` to control the internal auto-negotiation enable/disable, re-negotiation, duplex mode, rate mode, power-down, etc. It should be noted that `configuration_vector_chx_i` only exists when SGMII includes MAC function or only has PHY function and does not support PHY MIIM interface. Users can also configure `signal_detect_chx_i` as 1, which sets SGMII to support signal detection. Meanwhile, `signal_detect_chx_i` and `configuration_vector_chx_i[1]` together control the data synchronization function of SGMII. The bit definitions of `configuration_vector_chx_i` are shown in Table 3-1.

Table 3-1 Bit Definition of `configuration_vector_chx_i`

Location	Name	Description
14	Sgmii Phy Link	SGMII PHY link status in Media Mode 1: Link up 0: Link down
13	Sgmii Phy Duplex	SGMII Full-duplex mode in Media Mode 1: Full duplex 0: Half duplex
12:11	Sgmii Phy Speed	SGMII rate in Media Mode 1X: 1000M 01: 100M 00: 10M
[10:8]	Reserve	–
7	Disparity Check Enable	Disparity check enable 0: Disable 1: Enable
6	Power Down	Power down 1: Power down 0: Power up
5	Unidir En	Unidirection transmission 1: Enable 0: Disable
4	Mr Restart An	Restart auto-negotiation 1->0: Restart auto-negotiation
3	Isolate	Isolate data transmission between user and PHY layer 1: Enable 0: Disable
2	Mr An Enable	Auto-negotiation 1: Enable 0: Disable
1	Mr Loopback	Data synchronization

Location	Name	Description
		1: The IP performs data synchronization, and signal_detect_chx_i is not valid. 0: If signal_detect_chx_i=1, the IP performs data synchronization; if signal_detect_chx_i=0, the IP does not perform data synchronization.
0	Mr Main Reset	Reset 1: Reset 0: Release from reset

3.3.2 Status Interface

status_vector_chx_o indicates the current status of the SGMII, and link_partner_ability_base_chx_o indicates the information of the partner's configuration register at the time of this auto-negotiation. The bit definition of status_vector_chx_o is as shown in Table 3-2 .

Table 3-2 Bit Definition of status_vector_chx_o

Location	Name	Description
10	Decode Disparity Err	Decoding disparity error indication 1: Error 0: Normal
9	Decode Coding Err	Decoding data error indication 1: Error 0: Normal
8	Phy Link Status	PHY Link status indication of its partner in SGMII 1: Link up 0: Link down
7	Duplex Status	Duplex mode indication of its partner in SGMII 1: Full duplex 0: Half duplex
6:5	Speed Status	Rate indication of its partner in SGMII 1x: 1000M 01: 100M 00: 10M
4	Page Received	Its partner configuration register information received indication
3	Power Down	Power down indication 1: Power down 0: Power up
2	An Complete	Auto-negotiation completed indication 1: Auto-negotiation completed successfully 0: Auto-negotiation not completed
1	Link Status	Link status indication 1: Link up 0: Link down
0	Sync Status	Data synchronization status indication

Location	Name	Description
		1: Data synchronized 0: Data not synchronized

3.3.3 PHY Layer Interface

Ethernet Frame Reception

Ethernet frame reception is the process of converting serial data into Ethernet frame data. All reception signals are synchronized with gmii_rx_clk_chx_o.

Normal Ethernet Frame Reception

Figure 3-2 shows the normal Ethernet frame reception at 1000M. Figure 3-3 shows the normal Ethernet frame reception at 10M/100M.

At any rate, gmii_rx_clk_chx_o is 125MHz, and each byte is received repeatedly for 100 cycles at 10M; each byte is received repeatedly for 10 cycles at 100M; each byte is received for only 1 cycle at 1000M.

An Ethernet frame marks the start of a frame with a 7-byte Preamble and a 1-byte SFD at 1000M; while at 10M and 100M, each byte is received repeatedly for 100 and 10 cycles respectively. It should be noted that, at any rate, the presence of the start delimiter in the conversion may result in the loss of 1 byte in the received Preamble.

Throughout the Ethernet frame reception, gmii_rx_dv_chx_o remains at 1 until the end of the frame, then it changes to 0; while gmii_rx_er_chx_o is consistently 0, and gmii_rxd_chx_o is the received data. It should be noted that there is no buffer in IP for the received Ethernet frames, so the user must be ready to receive Ethernet frames at all times. The data of Ethernet frames will be continuously output until the entire frame has been received, with inter-frame gap between frames.

Figure 3-2 Normal Ethernet Frame Reception at 1000M

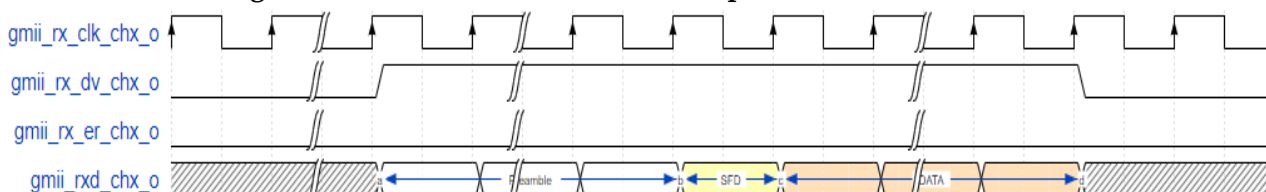
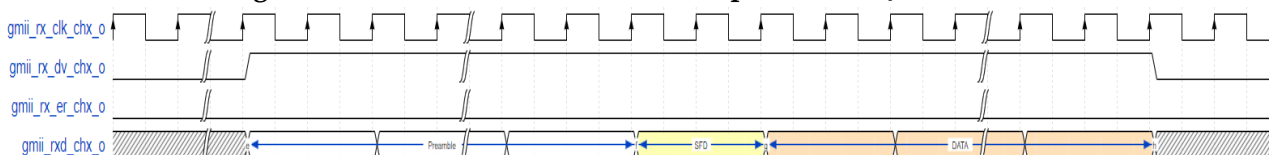


Figure 3-3 Normal Ethernet Frame Reception at 10M/100M



Ethernet Frame Reception with Error

When gmii_rx_dv_chx_o is 1, if gmii_rx_er_chx_o is 1, it means that the current frame has some error data. Figure 3-4 and Figure 3-5 show the

reception with an error frame at 1000M and 10M/100M respectively.

Figure 3-4 Frame Reception with Errors at 1000M

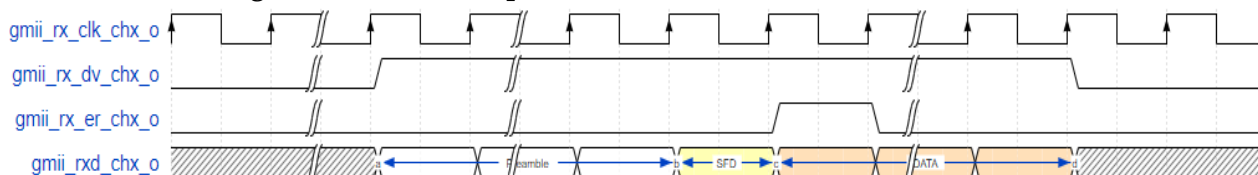
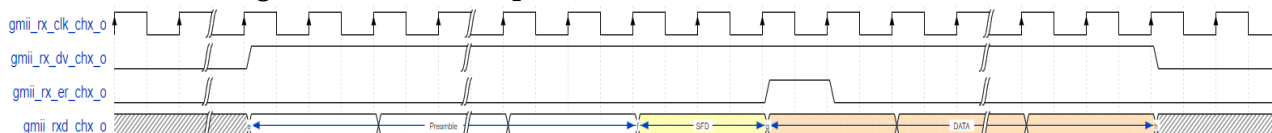


Figure 3-5 Frame Reception with Errors at 10M/100M



Reception with Carrier Extension

When gmii_rx_dv_chx_o is 0, gmii_rx_er_chx_o is 1, and gmii_rxd_chx_o is 8'h0F, it is the reception with carrier extension, and it should be noted that the carrier extension will immediately follow the Ethernet frame reception. Figure 3-6 shows the reception with carrier extension at 1000M, and Figure 3-7 shows the reception with carrier extension at 10M/100M.

Figure 3-6 Reception with Carrier Extension at 1000M

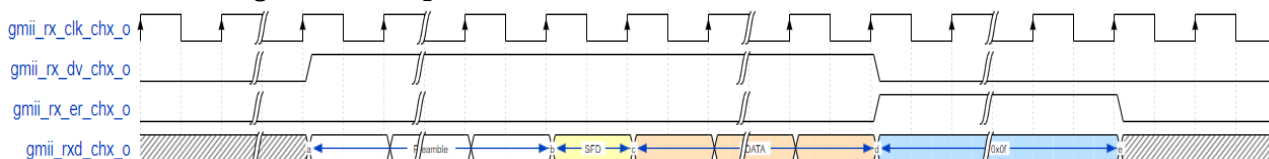
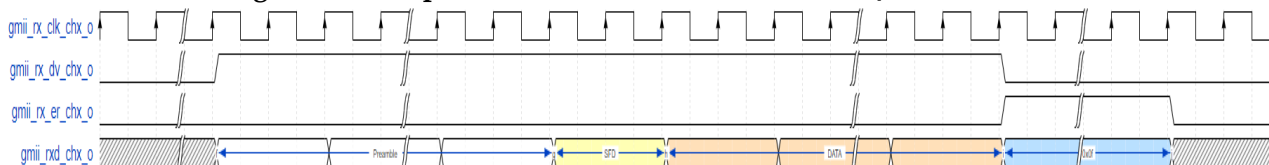
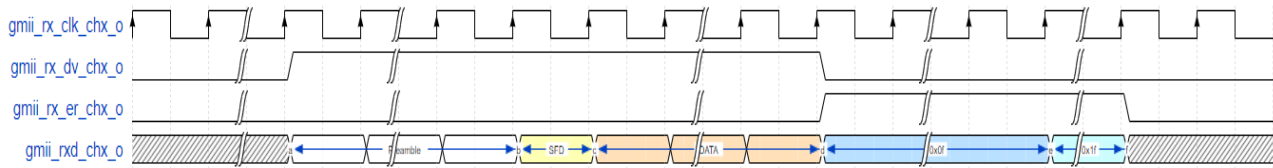
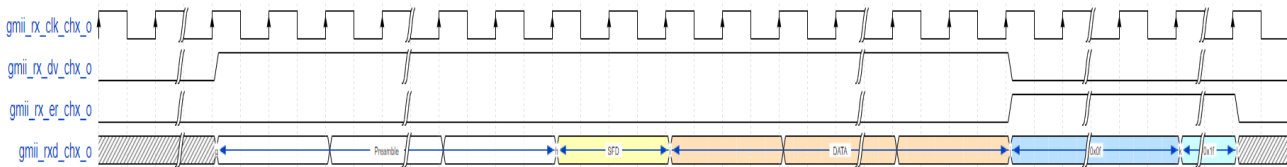


Figure 3-7 Reception with Carrier Extension at 10M/100M



Carrier Extension Reception with Error

On the basis of carrier extension reception, when gmii_rx_dv_chx_o is 0 and gmii_rx_er_chx_o = 1, the situation of gmii_rxd_chx_o being 8'h1F occurs. Figure 3-8 shows the carrier extension reception with error at 1000M. Figure 3-9 shows the carrier extension reception with error at 10M/100M.

Figure 3-8 Carrier Extension Reception with Error at 1000M**Figure 3-9 Carrier Extension Reception with Error at 10M/100M**

Ethernet Transmit

Ethernet transmit is the conversion from Ethernet frame data into serial data. All the transmit signal are synchronized with gmii_tx_clk_chx_o.

Normal Ethernet Frame Transmit

Figure 3-10 shows the normal Ethernet frame transmit at 1000M. Figure 3-11 shows the normal Ethernet frame transmit at 10M/100M.

At any rate, gmii_tx_clk_chx_o is 125MHz, and each byte is transmitted repeatedly for 100 cycles at 10M; each byte is transmitted repeatedly for 10 cycles at 100M; each byte is transmitted for only 1 cycle at 1000M.

An Ethernet frame marks the start of a frame with a 7-byte Preamble and a 1-byte SFD at 1000M; while at 10M and 100M, each byte is transmitted repeatedly for 100 and 10 cycles respectively.

Throughout the Ethernet frame transmit, gmii_tx_en_chx_i remains at 1 until the end of the frame, then it changes to 0; while gmii_tx_er_chx_i is consistently 0; when gmii_tx_en_chx_i is 1, the byte to be transferred is assigned to gmii_txd_chx_i. It should be noted that there is no buffer in the IP for transmitted Ethernet frames. Therefore, when the first byte starts to be transmitted, the user needs to prepare subsequent bytes; and assign the data to gmii_txd_chx_i in time when gmii_tx_en_chx_i is 1, until the whole frame is transmitted.

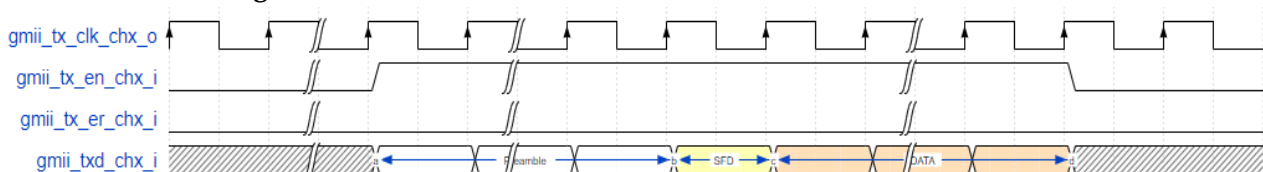
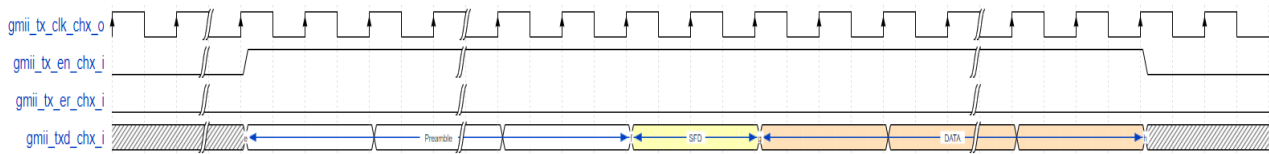
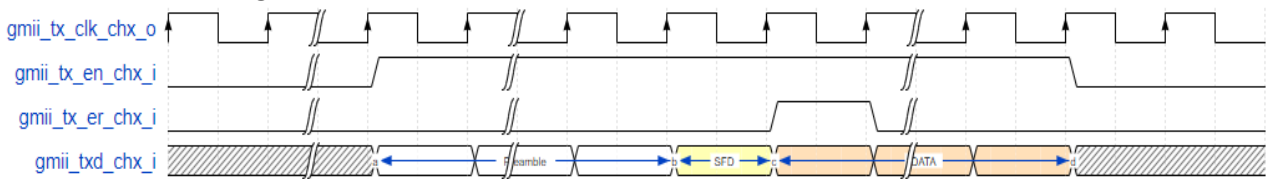
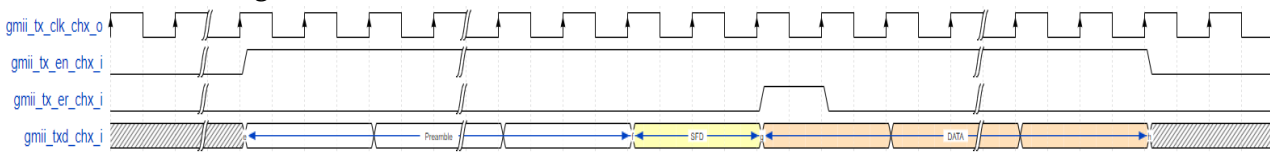
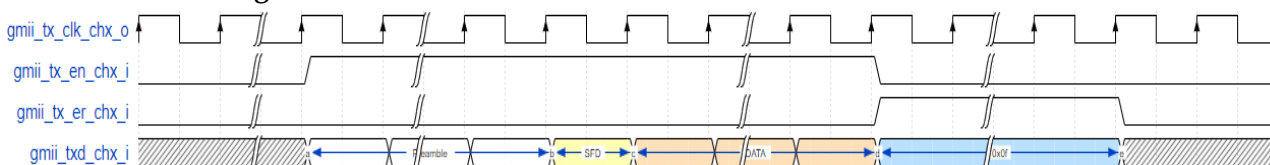
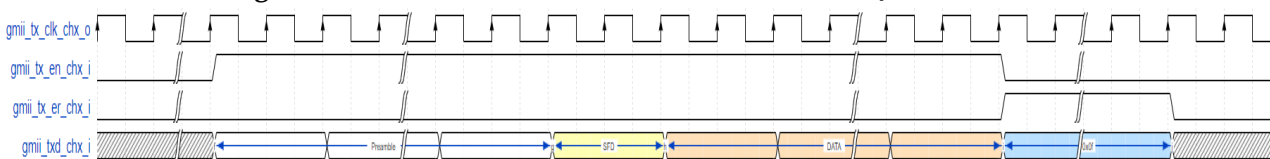
Figure 3-10 Normal Ethernet Frame Transmit at 1000M

Figure 3-11 Normal Ethernet Frame Transmit at 10M/100M**Ethernet Frame Transmit with Error**

During the transmit, when gmii_tx_en_chx_i and gmii_tx_er_chx_i are both 1, it indicates that there is an error in the current frame. Figure 3-12 shows the Ethernet frame transmit with error at 1000M. Figure 3-13 shows the Ethernet frame transmit with error at 10M/100M.

Figure 3-12 Ethernet Frame Transmit with Error at 1000M**Figure 3-13 Ethernet Frame Transmit with Error at 10M/1000M****Transmit with Carrier Extension**

When gmii_tx_en_chx_i is 0, gmii_tx_er_chx_i=1, and gmii_txd_chx_i is 8'h0F, it is the transmit with carrier extension, and it should be noted that the carrier extension will immediately follow the Ethernet frame transmit. Figure 3-14 shows the transmit with carrier extension at 1000M, and Figure 3-15 shows the transmit with carrier extension at 10M/100M.

Figure 3-14 Transmit with Carrier Extension at 1000M**Figure 3-15 Transmit with Carrier Extension at 10M/100M**

Carrier Extension Transmit with Error

On the basis of carrier extension transmit, when gmii_tx_en_chx_i is 0 and gmii_tx_er_chx_i=1, gmii_txd_chx_i will first output a continuous 8'h0f, followed by a continuous 8'h1f. Figure 3-16 shows the carrier extension transmit with error at 1000M. Figure 3-17 shows the carrier extension transmit with error at 10M/100M.

Figure 3-16 Carrier Extension Transmit with Error at 1000M

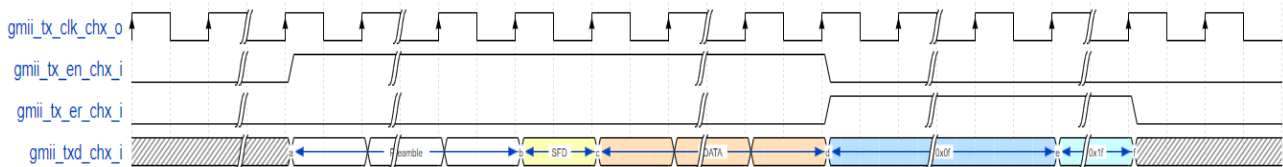
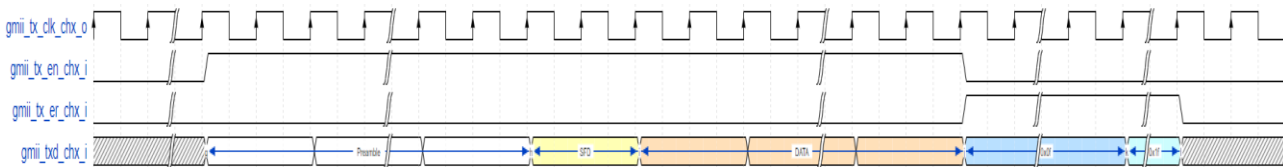


Figure 3-17 Carrier Extension Transmit with Error at 10M/100M



Transmit in Half Duplex Mode

In half-duplex mode, the gmii_crs_chx_o and gmii_col_chx_o signals are detected before transmit, if both are 0, the Ethernet frame can be transmitted in half-duplex mode, otherwise continue to wait; during the transmit, if the user detects that gmii_col_chx_o is 1, it is necessary to immediately set gmii_tx_en_chx_i and gmii_tx_er_chx_i to 0, which is used to end the transmit of this Ethernet frame. After gmii_crs_chx_o and gmii_col_chx_o are both 0, the user can decide whether to re-transmit the frame or not. Figure 3-18 shows the transmit in half-duplex mode at 1000M. Figure 3-19 shows the transmit collision at 1000M.

Figure 3-18 Transmit in Half Duplex Mode at 1000M

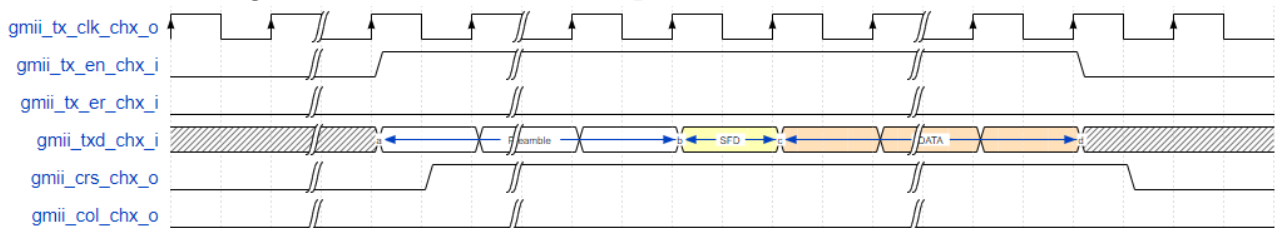
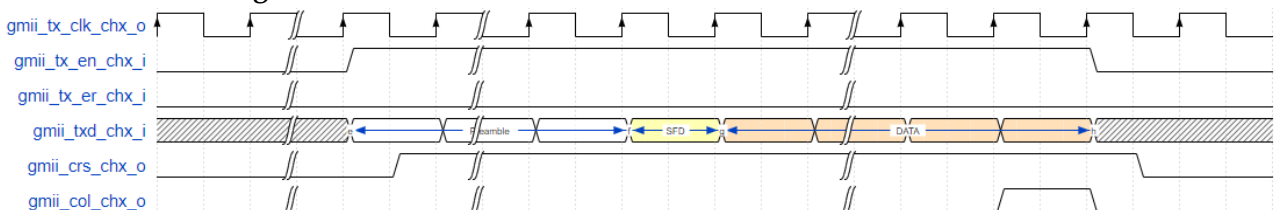


Figure 3-19 Transmit Collision at 1000M



3.3.4 MAC Layer Interface

MAC Frame Reception

Ethernet frame reception is the conversion from serial data to user data. All reception signals are synchronized with rx_mac_clk_chx_o.

Normal MAC Frame Reception

Figure 3-20 shows the normal MAC frame reception at 1000M.

Figure 3-21 shows the normal MAC frame reception at 10M/100M.

When rx_mac_valid_chx_o is 1, it means that rx_mac_data_chx_o in this cycle is valid; When rx_mac_valid_chx_o and rx_mac_last_chx_o are both 1, it means rx_mac_data_chx_o in this cycle is valid and is the last byte of the MAC frame for this frame. It should be noted that there is no buffer in IP for the received MAC frames, so the user must always be ready to receive MAC frames. When the first byte of the frame begins to appear in the user interface, the data is received continuously until the whole frame is received.

Figure 3-20 Normal MAC Frame Reception at 1000M

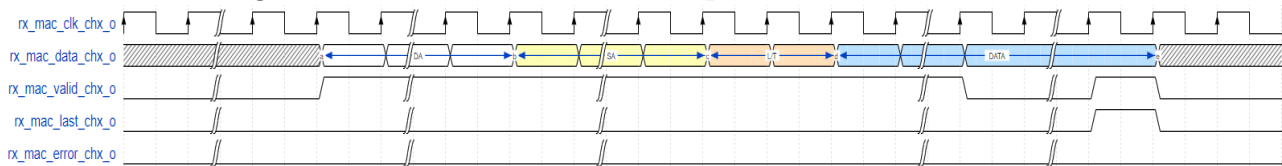
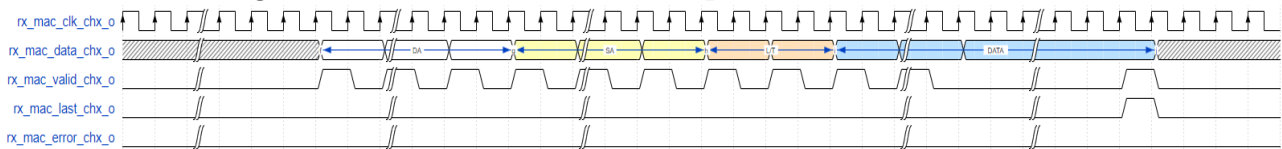


Figure 3-21 Normal MAC Frame Reception at 10M/100M



MAC Frame Reception with Error

When rx_mac_error_chx_o is 1, it indicates that there are some errors in the current frame, and the specific error type can be checked through rx_statistics_valid_chx_o and rx_statistics_vector_chx_o signals.

rx_mac_error_chx_o indicates the error status of the current frame only when rx_mac_last_chx_o is 1. Figure 3-22 and Figure 3-23 show the reception of an error MAC frame at 1000M and 10M/100M respectively.

Figure 3-22 MAC Frame Reception with Error at 1000M

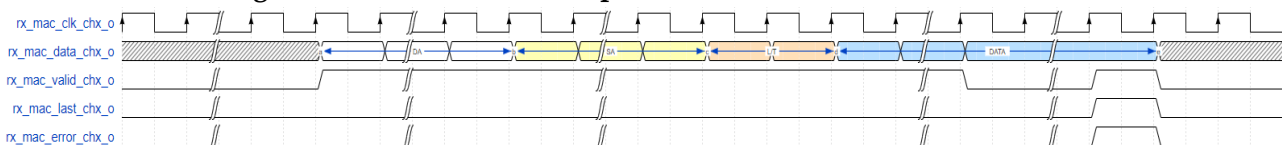
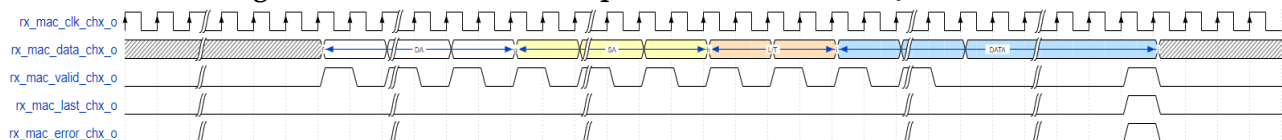


Figure 3-23 MAC Frame Reception with Error at 10M/1000M



When the following errors occur, rx_mac_error_chx_o will indicate:

1. Receive FCS frame with error
2. Receive align frame
3. In the reception, the signal gmii_rx_er_chx_o at PHY layer interface is valid
4. Collision occurred in half duplex
5. Frame length error; when the Jumbo is disabled, receive non-VLAN frame of less than 64 or more than 1518 bytes, and VLAN frames of less than 64 or more than 1522 bytes; When Jumbo is enabled, receive frame of less than 64 bytes.

MAC Frame FCS Forward Reception

When the user sets the IP to FCS Forward reception mode, IP will send the received FCS field to the user side, as shown from Figure 3-24 to Figure 3-27. At this time, the IP still automatically verifies the FCS field and indicates thorough rx_mac_error_chx_o and rx_statistics_vector_chx_o.

Figure 3-24 Normal MAC Frame Reception When FCS Forward Enabled at 1000M

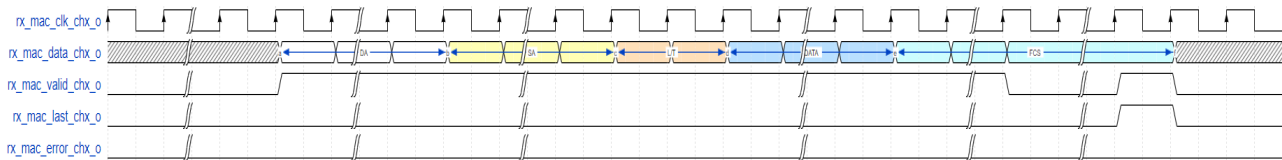


Figure 3-25 MAC Frame Reception with Error When FCS Forward Enabled at 1000M

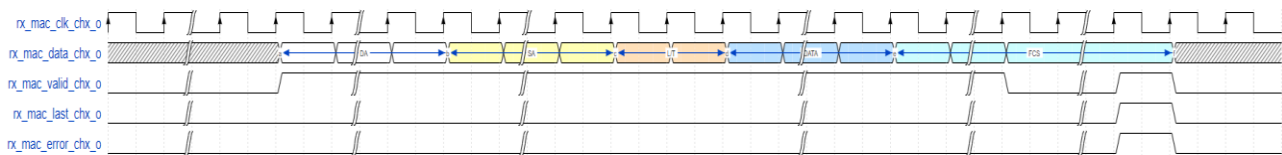


Figure 3-26 Normal MAC Frame Reception When FCS Forward Enabled at 10M/100M

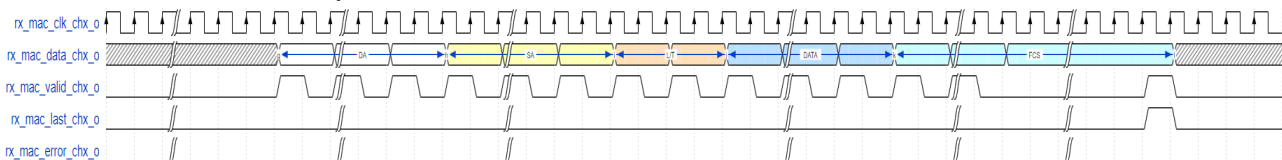
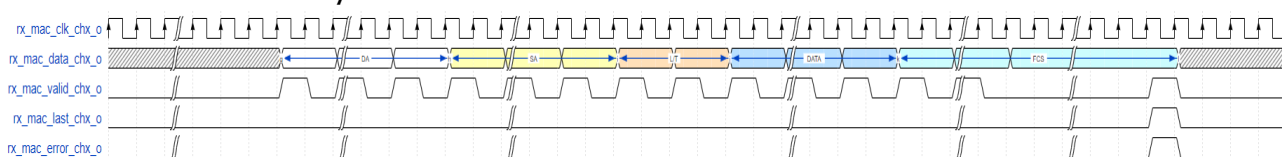


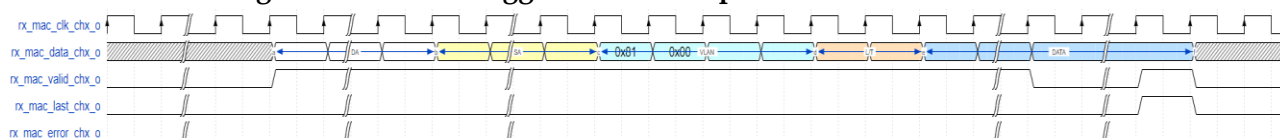
Figure 3-27 MAC Frame Reception with Error When FCS Forward Enabled at 10M/100M



VLAN Tagged Frame Reception

When the IP receives a VLAN Tagged frame, it will indicate that this frame is a VLAN Tagged frame through `rx_statistics_vector_chx_o`. VLAN Tagged frame is a frame with two bytes 0x8100 after the source MAC address. The VLAN field is defined as 4 bytes in IEEE802.3. The first two bytes are 0x8100 and the last two bytes are VLAN tag, as shown in Figure 3-28.

Figure 3-28 VLAN Tagged Frame Reception



MAC Control Frame Reception

When the IP receives a MAC Control frame, it will indicate that this frame is a MAC Control frame through `rx_statistics_vector_chx_o`. MAC Control frame is a frame with L/T field of 0x8808. When the L/T field is 0x8808 in IEEE802.3, this frame is a MAC Control frame.

Abnormal Reception on Ethernet Cable

Single-byte frame may occur on the cable in the event of an abnormal Ethernet cable or a half-duplex collision. At this moment, the first `rx_mac_valid_chx_o` and `rx_mac_last_chx_o` of the user side interface will be both 1, that is, after a byte is received, the frame ends. The occurrence of such an exception can be handled by user applications.

Reception Statistics

Statistics of reception frames are output through `rx_statistics_vector_chx_o` signal. When `rx_statistics_valid_chx_o` is 1, it indicates that `rx_statistics_vector_chx_o` is valid, and `rx_statistics_vector_chx_o` indicates the statistical information of the received frames. The timing diagram is as shown in Figure 3-29, and the bit definition of `rx_statistics_vector_chx_o` is shown in Table 3-3.

Figure 3-29 Reception Statistics

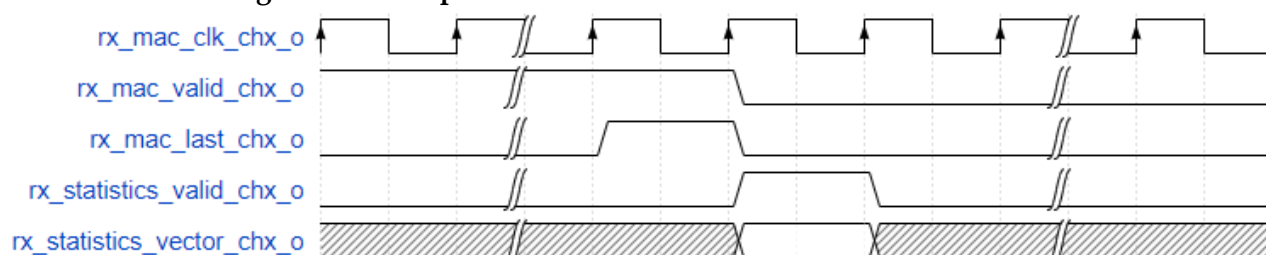


Table 3-3 Bit Definition of `rx_statistics_vector_chx_o`

Location	Name	Description
26	RX Alignment Error	If the received frame is not an integer multiple of bytes, set 1.

Location	Name	Description
25	RX Length Error	If the received frame length does not meet the standard, set 1
24	RX FCS Error	If the received frame has an FCS error, set 1
23	RX_ER Error	If gmii_rx_er_chx_o signal at PHY layer interface is valid during reception, set 1
22	RX Collision Error	In half duplex mode, if a collision occurs during the frame reception, set 1
21:6	RX Frame Length	The length of received frame, including FCS field
5	RX Flow Control Frame	In full duplex mode, if the received frame is a flow control frame, set 1
4	RX MAC Control Frame	If the received frame is a MAC Control frame, set 1
3	RX VLAN Frame	If the received frame is a VLAN frame, set 1
2	RX Multicast Frame	If the received frame is a multicast frame, set 1
1	RX Broadcast Frame	If the received frame is a broadcast frame, set 1
0	RX Unicast Frame	If the received frame is a unicast frame, set 1

MAC Frame Transmit

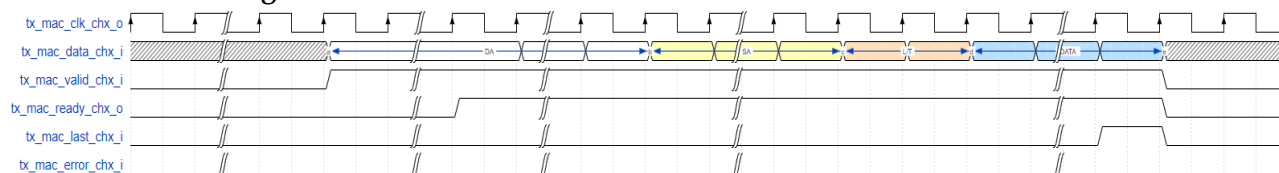
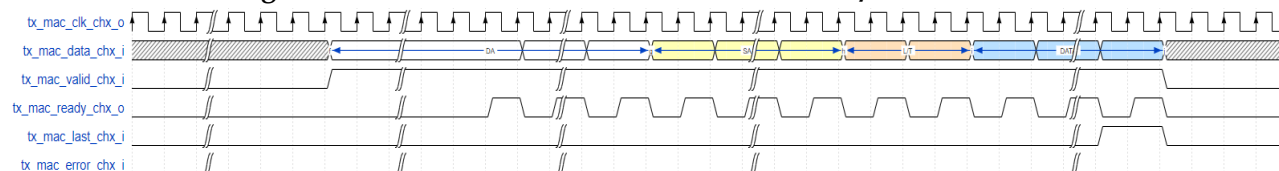
MAC frame transmit is the conversion from user data to serial data. All the transmit signal are synchronized with tx_mac_clk_chx_o.

Normal MAC Frame Transmit

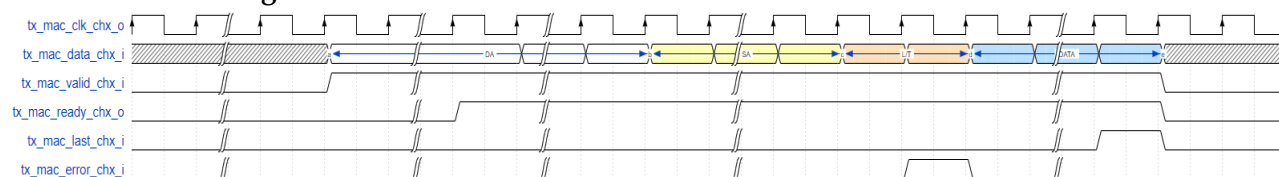
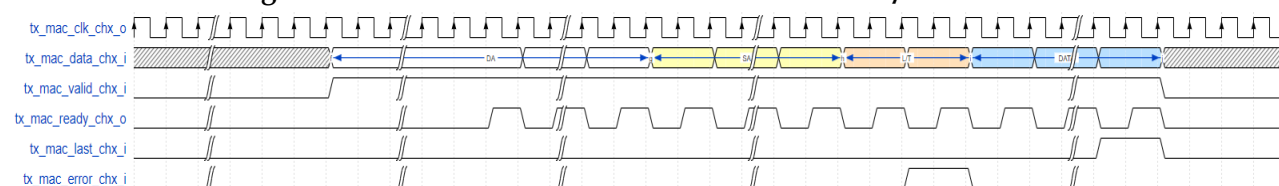
Figure 3-30 shows the normal MAC frame transmit at 1000M. Figure 3-31 shows the normal MAC frame transmit at 10M/100M.

At any rate, tx_mac_clk_chx_o is 125MHz; the difference is that tx_mac_ready_chx_o is valid once per 100 cycles at 10M; tx_mac_ready_chx_o is valid once per 10 cycles at 100M, and tx_mac_ready_chx_o is valid every cycle at 1000M.

Throughout the transmit, tx_mac_valid_chx_i must remain at 1 until the end of the frame, then it changes to 0. When tx_mac_ready_chx_o and tx_mac_last_chx_i are both 1, it indicates tx_mac_data_chx_i is transmitted in this cycle and it is the last byte of the MAC frame for this frame. It should be noted that there is no buffer in the IP for the transmitted MAC frames. Therefore, when the first byte starts to be transmitted, the user side need to prepare subsequent bytes and assign them to tx_mac_data_chx_i in time when tx_mac_ready_chx_o is 1, until the whole frame is transmitted.

Figure 3-30 Normal MAC Frame Transmit at 1000M**Figure 3-31 Normal MAC Frame Transmit at 10M/100M****MAC Frame Transmit with Error**

During the transmit, when tx_mac_error_chx_i and tx_mac_ready_chx_o are both 1, it indicates that there are some errors in the current transmitted frame. And the IP will send data error indication at the PHY layer interface. Figure 3-32 shows the MAC frame transmit with error at 1000M. Figure 3-33 shows the MAC frame transmit with error at 10M/100M.

Figure 3-32 MAC Frame Transmit with Error at 1000M**Figure 3-33 MAC Frame Transmit with Error at 10M/1000M****Transmit MAC Frame FCS Forward**

When the user sets IP to FCS Forward mode, the IP will not automatically add FCS field. After the DATA field are transmitted, the FCS field needs to be calculated and added manually, as shown in Figure 3-34 and Figure 3-35.

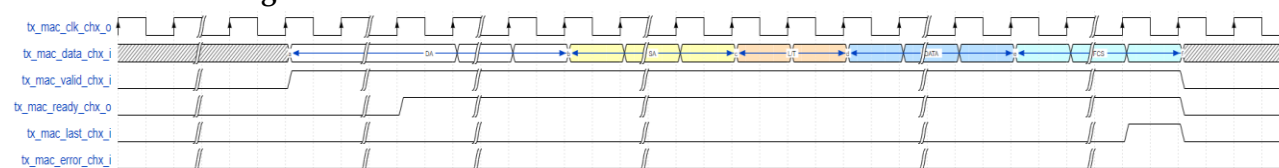
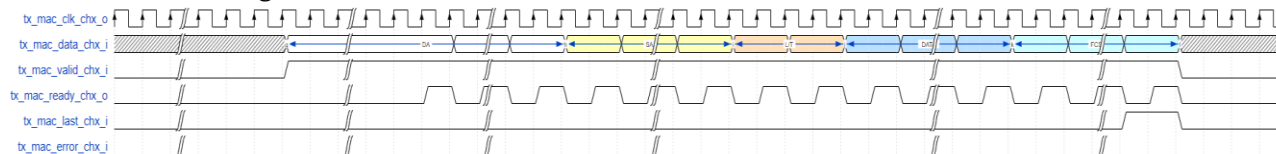
Figure 3-34 MAC Frame Transmit When FCS Forward Enabled at 1000M

Figure 3-35 MAC Frame Transmit When FCS Forward Enabled at 10M/100M

Transmit in Half Duplex Mode

In half duplex mode, IP indicates the transmit status through `tx_collision_chx_o` and `tx_retransmit_chx_o` signals. If the user does not detect any collision during the transmit, the MAC frames can be transmitted in full duplex mode. If the user detects a collision during the transmit, the followings should be done to ensure the data transmit. When the user detects `tx_collision_chx_o` to be 1, it means that there is a collision on the cable. The user must immediately set `tx_mac_valid_chx_i` to 0 when he detects `tx_collision_chx_o` to be 1, so as to end the MAC frame transmit. With the detection of `tx_collision_chx_o` to be 1, and if `tx_retransmit_chx_o` is 1, it indicates that the collision is within a reasonable range, and the user can decide whether to re-transmit the frame or not. If the user prepares to re-transmit the frame, set `tx_mac_valid_chx_i` to 1 within 5 cycles to prepare for the re-transmit. If the user prepares to abort the re-transmit, set `tx_mac_valid_chx_i` to 1 after 5 cycles to prepare for the next frame transmit. With the detection of `tx_collision_chx_o` to be 1, and if `tx_retransmit_chx_o` is 0, it indicates that the collision is not within a reasonable range (a frame with more than 16 collisions, or collisions occurring after 64 bytes having been transmitted), then the user needs to abort the transmit. Figure 3-36 shows the transmit when a conflict occurs. Figure 3-37 and Figure 3-38 show aborting the re-transmit when a conflict occurs respectively.

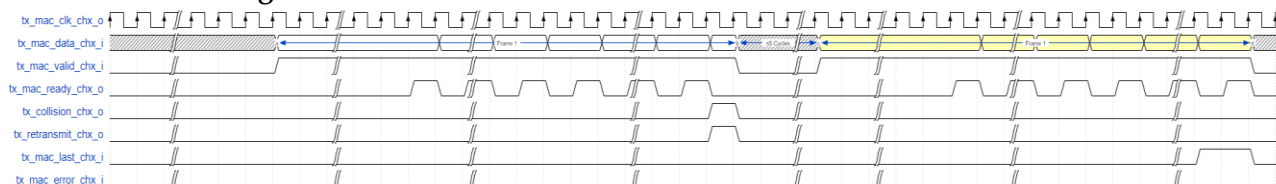
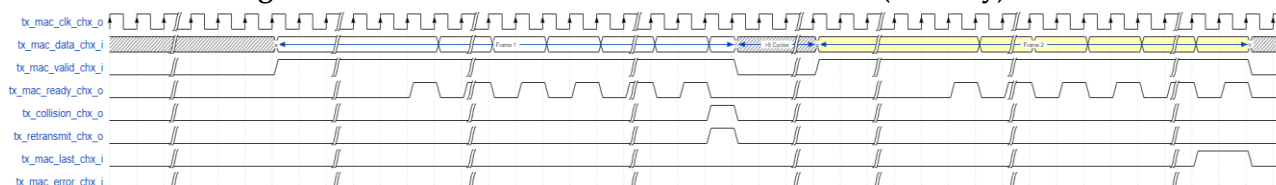
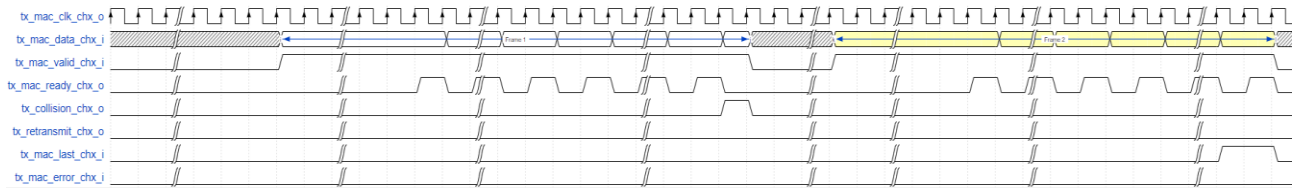
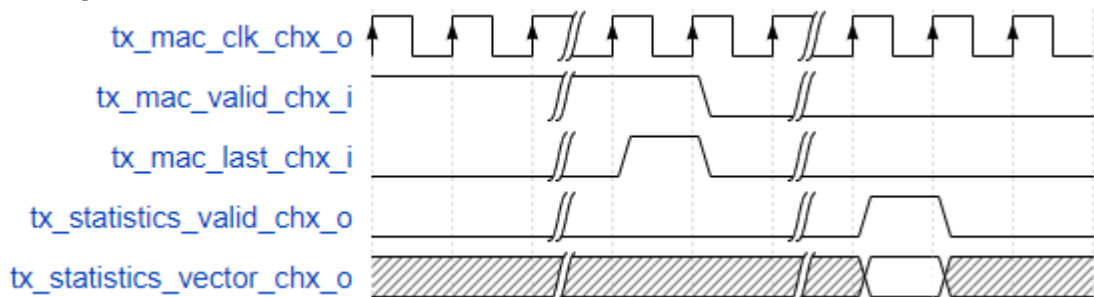
Figure 3-36 Re-transmit in Case of Collision**Figure 3-37 Abort Re-transmit in Case of Collision (Actively)**

Figure 3-38 Abort Re-transmit in Case of Collision (Passively)

Transmit Statistics

Transmit statistics is output through **tx_statistics_vector_chx_o** signal. When **tx_statistics_valid_chx_o** is 1, it indicates that **tx_statistics_vector_chx_o** is valid, and at this time, **tx_statistics_vector_chx_o** indicates the statistics information of the transmitted frames. The timing diagram is as shown in Figure 3-39, and the bit definition of **tx_statistics_vector_chx_o** is shown in Table 3-4.

Figure 3-39 Transmit Statistics**Table 3-4 Bit Definition of tx_statistics_vector_chx_o**

Location	Name	Description
28	TX Collision	In half duplex mode, if a collision occurs when this frame is transmitted, set 1.
27:24	TX Attempts	In half duplex mode, number of attempts to transmit this frame. 0 represents the first transmit; 1 represents the second transmit; 15 represents the 16th transmit.
23	Excessive Collision	In half duplex mode, if the frame is on the 16th attempt to transmit with collision occurring, set 1
22	Late Collision	If the collision occurs after 64 bytes having been transmitted, set 1
21:6	TX Frame Length	Transmit frame length, including FCS field
5	TX Flow Control Frame	In full duplex mode, if the IP is configured to transmit a flow control frame, set 1
4	TX MAC Control Frame	If the transmit frame is a MAC Control frame, set 1
3	TX VLAN Frame	If the transmit frame is VLAN frame, set 1
2	TX Multicast Frame	If the transmit frame is Multicast frame, set 1
1	TX Broadcast Frame	If the transmit frame is Broadcast frame, set 1
0	TX Unicast Frame	If the transmit frame is Unicast frame, set 1

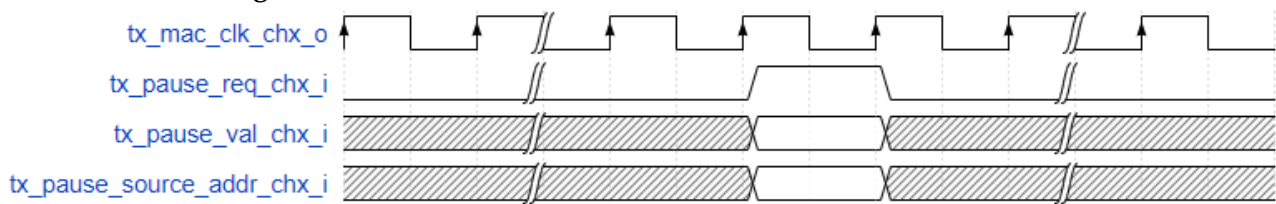
Flow Control Function

The IP supports the Flow Control function in full duplex mode. In full duplex mode, users can configure IP to transmit or receive Pause frame to achieve flow control.

Transmit Pause Frame

Users can set `tx_pause_req_chx_i` to 1 to transmit a pause frame. The value of `tx_pause_val_chx_i` is inserted into the parameter field of the pause frame to calculate the pause time. `tx_pause_source_addr_chx_i` is transmitted as the source MAC address for the pause frame, and the order is from the low to high bytes.

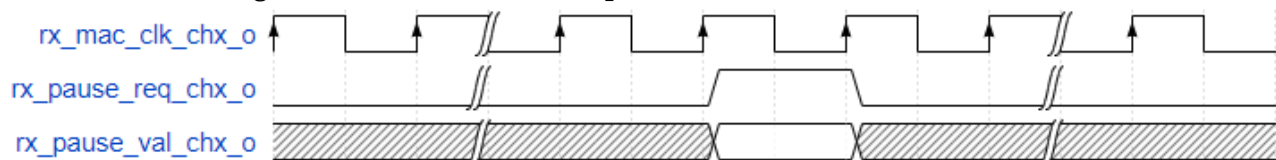
Figure 3-40 Pause Frame Transmit



Receive Pause Frame

When the IP receives a pause, it sets `rx_pause_req_chx_o` to 1. The value of `rx_pause_val_chx_o` is the parameter field of the received pause frame and is used to calculate the pause time.

Figure 3-41 Pause Frame Reception



FCS Forward Function

The IP supports configuring FCS Forward for transmit and reception respectively.

Receive FCS Forward

When the user disables the FCS Forward function, the FCS field will not be output to the user side. The IP automatically verifies the FCS field and its results will be output to the corresponding field of `rx_statistics_vector_chx_o`. When the user enables the FCS Forward function, the FCS field will be output to the user side. The IP still automatically verifies the FCS field and its results will be output to the corresponding field of `rx_statistics_vector_chx_o`.

Transmit FCS Forward

When the user disables the FCS Forward transmit function, the user does not need to calculate and transmit the FCS field. The IP calculates the FCS field and adds it to the Ethernet frame automatically. When the user

enables the FCS Forward function, the user calculates the FCS field and transmits it to the IP on the user side.

PAD Function

When the user disables the FCS Forward function, if the frame transmitted by the user to IP is less than 60 bytes (excluding FCS), IP will automatically pad 0 to 60 bytes then add FCS field to ensure that the Ethernet frame transmit meets the requirement of minimum 64 bytes. When the user enables the FCS Forward function, the IP will not automatically pad to 64 bytes, and the actual transmitted data and length are completely determined by the user.

Transmit IFG

When the IP is operating in full duplex mode, the user can set the minimum IFG transmitted by Ethernet. When the IP is operating in half duplex mode, the minimum transmitted IFG set by users is ignored, and the minimum IFG is still 12 bytes.

When the user disables IFG function, IP transmits a minimum IFG of 12 bytes, i.e. 96 bits. When the user enables IFG function, IP determines the minimum IFG based on the user settings. If the minimum IFG set by the user is less than 8 bytes, the actual minimum IFG of IP is 8 bytes; if the user sets the minimum IFG to be greater than or equal to 8 bytes, the actual minimum IFG of IP is the value set by the user. The minimum IFG can be set to a maximum of 255 bytes.

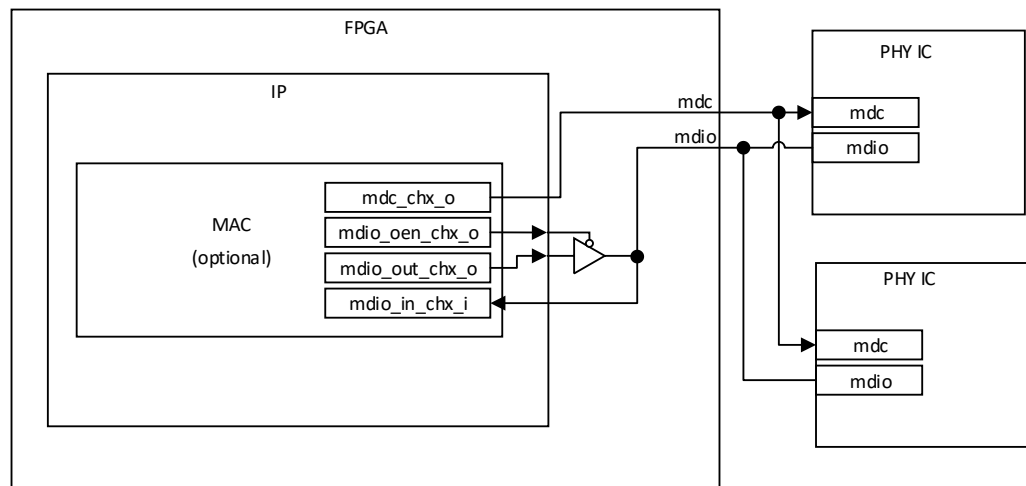
Jumbo Function

The IP supports the Jumbo function. When the user disables Jumbo function, IP judges that the normal Ethernet frame length is 64 bytes to 1518 bytes (non-VLAN frames) or 64 bytes to 1522 bytes (VLAN frames). If the Ethernet frames received are not within the above range, rx_mac_error_chx_o will indicate that there are some errors on this frame and RX Length Error is 1 in rx_statistics_vector_chx_o. When the user enables Jumbo function, the IP judges there is an error only if the Ethernet frames received are smaller than 64 bytes.

Management Function

The IP provides users with MIIM interface to facilitate them to configure PHY chip registers through MDC and MDIO.

MDC clock is divided by the input clock miim_hs_clk_chx_i. Users need to configure frequency divider according to the input clock miim_hs_clk_chx_i to make MDC clock frequency meet the requirements of PHY chip. See Table 5-1 for configuration method; MDC and MDIO connection is as shown in Figure 3-42.

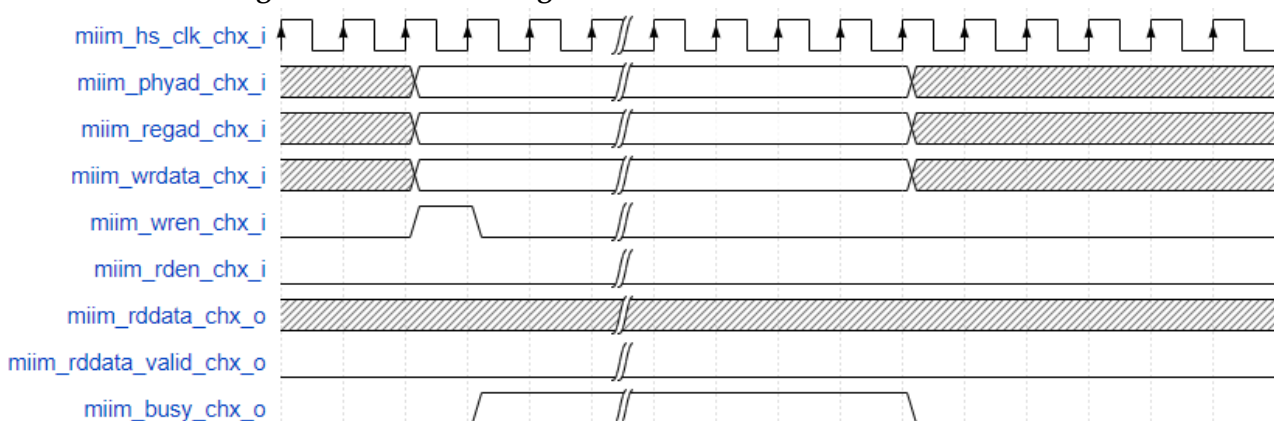
Figure 3-42 Connection Diagram of MDC and MDIO

The MDIO connection reference verilog is as follows:

```
assign mdio_in_chx_i = mdio;
assign mdio = (!mdio_oen_chx_o) ? mdio_out_chx_o : 1'bz;
```

All miim interface signals are synchronized with miim_hs_clk_chx_i clock.

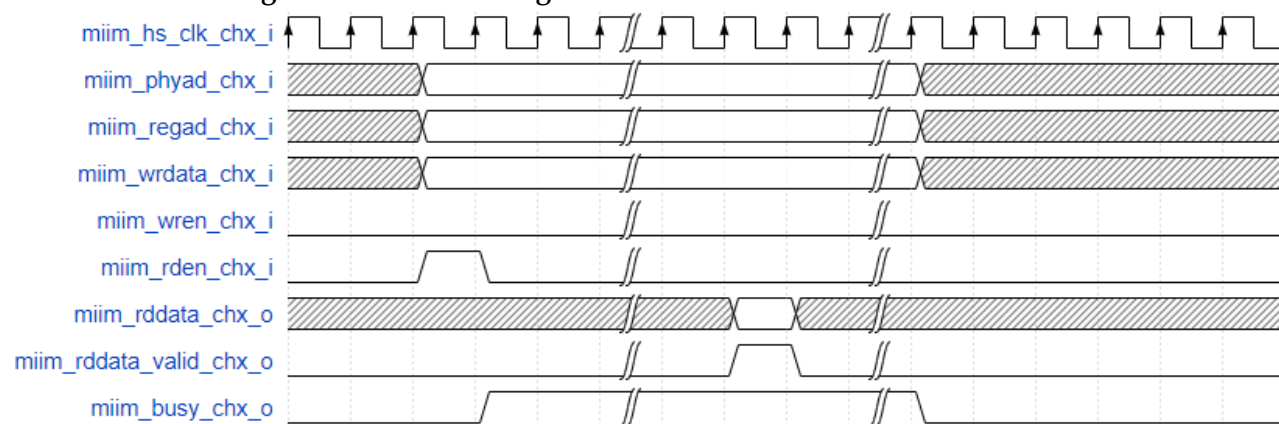
For the write operations, the user needs to set miim_wren_chx_i to 1 for one cycle. The IP will pull up miim_busy_chx_o, indicating that the miim bus is performing write operations. When miim_busy_chx_o is 0 again, it indicates this write ends, and the user can be ready for the next read or write. miim_phyad_chx_i, miim_regad_chx_i, and miim_wrdata_chx_i signals need to be ready on the bus when miim_wren_chx_i is 1, and it holds when miim_busy_chx_o is 1. See Figure 3-43 for miim write timing diagram.

Figure 3-43 Write Timing of miim

For read operations, the user need to set miim_rden_chx_i to 1 for one cycle. The IP will pull up miim_busy_chx_o, indicating that the miim bus is performing read operations. When miim_busy_chx_o is 0 again, it indicates that this read operation ends and the user can be ready for the next read or

write. `Miim_phyad_chx_i` and `miim_regad_chx_i` signals are ready on the bus when `miim_rden_chx_i` is 1, and it holds when `miim_busy_chx_o` is 1. During the read, the user monitors the `miim_rddata_valid_chx_o` signal. When `miim_rddata_valid_chx_o` is 1, the user can sample the value of this read on the `miim_rddata_chx_o` signal. See Figure 3-44 for `miim` read timing diagram.

Figure 3-44 Read Timing of `miim`



3.4 AFE (Analog Front End)

AFE means analog front end. Gowin QSGMII IP operates at a speed of 5 Gbps. Users can configure the analog parameters of the IP through the interface to ensure signal integrity.

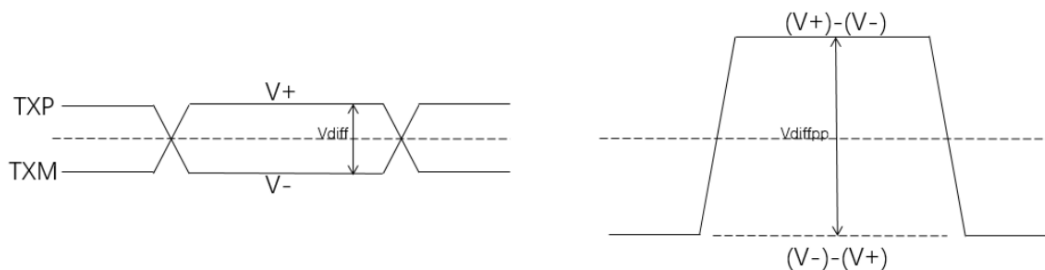
3.4.1 Transmit

On the TX side, the user can configure the differential swing and FFE parameters of the TX signals.

Transmit Differential Swing

As shown in Figure 3-45, the differential voltage of TX signal is $V_{diff} = (V+) - (V-)$, and the TX differential signal swing is $V_{diffpp} = 2 * V_{diff}$, and the user can configure V_{diffpp} through the interface with the range of 180mV~900mV.

Figure 3-45 TX Differential Signal Swing V_{diffpp}



TX FFE

FFE means Feed-Forward Equalization (FFE); the IP supports auto and manual adjustments of TX FFE coefficients. When the user configures FFE Mode as Auto, IP automatically adjusts the FFE coefficient according to the hardware environment, at this time C_m , C_0 and C_1 configuration is

invalid. When the user configures FFE Mode as Manual, the user can manually adjust the 3-tap coefficients and configure the de-weighting of the TX signal.

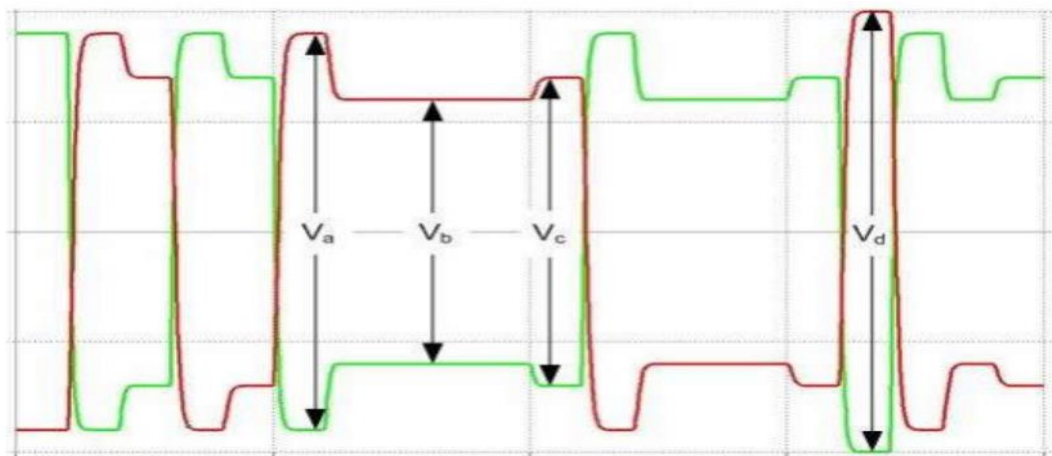
As shown in Figure 3-46, when the user configures the FFE Mode as Manual, the voltage amplitude of V_a , V_b and V_c can be adjusted by adjusting the values of C_m , C_0 and C_1 , and the calculation formula is as follows:

$$V_a = V_{diffpp} * (-C_m + C_0 + C_1) / 40$$

$$V_b = V_{diffpp} * (-C_m + C_0 - C_1) / 40$$

$$V_c = V_{diffpp} * (C_m + C_0 - C_1) / 40$$

Figure 3-46 FFE TX Voltage Definition



3.4.2 Receive

Receive Differential Signal Threshold

On the RX side, the user can configure the SD Threshold option to adjust the effective voltage threshold of RX signal. When the RX differential signal is greater than SD threshold, SerDes judges that the valid data is received; when the RX differential signal is less than SD threshold, SerDes judges that the valid data is not received, then enters the Electrical Idle state.

3.5 Reference Clock

To ensure proper operation of the SerDes, a stable reference clock is required. Users must ensure both the accuracy and stability of the reference clock frequency during SerDes operation.

3.5.1 GW5AT-15

GW5AT-15 SerDes provides four reference clocks including two from dedicated SerDes reference clock inputs, one from GPIO, and one from the internal OSC clock. Table 3-5 shows the mapping between the schematic package and reference clocks on the IP interface.

If the user chooses to use GPIO as the SerDes reference clock, the IP

port `gpio_refclk_i` must be connected to a top-level input during SerDes IP instantiation, and the corresponding IO location must be constrained in the CST file. If unused, the `gpio_refclk_i` can be left floating. If the internal oscillator (OSC) of the FPGA is used as the reference clock, the OSCB primitive must be instantiated in the design, and the OSCREF of the OSCB primitive should be connected to the IP port `mclk_i`. If unused, the `mclk_i` can be left floating.

Table 3-5 Reference Clock Mapping for GW5AT-15

Reference Clock	Schematic Package	IP GUI Option	IP Pin
Quad0 Refclk0	Q0_REFCLKP/M_0	Q0 REFCLK0	-
Quad0 Refclk1	Q0_REFCLKP/M_1	Q0 REFCLK1	-
GPIO	Q0REF_T/C_IN	Q0 REFIN	<code>gpio_refclk_i</code>
Internal OSC	-	MCLK	<code>mclk_i</code>

3.5.2 GW5AT-60

GW5AT-60 SerDes provides six reference clocks including four from dedicated SerDes reference clock inputs and two from GPIOs. Table 3-6 shows the mapping between the schematic package and reference clocks on the IP interface.

If the user chooses to use GPIO0 or GPIO1 as the SerDes reference clock, the IP ports `gpio_refclk0_i` or `gpio_refclk1_i` must be connected to top-level inputs during IP instantiation, and the corresponding IO locations must be constrained in the CST file. If unused, these pins can be left floating.

Table 3-6 Reference Clock Mapping for GW5AT-60

Reference Clock	Schematic Package	IP GUI Option	IP Pin
Quad0 Refclk0	Q0_REFCLKP/M_0	Q0 REFCLK0	-
Quad0 Refclk1	Q0_REFCLKP/M_1	Q0 REFCLK1	-
Quad0 Refclk2	Q0_REFCLKP/M_2	Q0 REFCLK2	-
Quad0 Refclk3	Q0_REFCLKP/M_3	Q0 REFCLK3	-
GPIO0	Q0REF_T/C_IN0	Q0 REFIN0	<code>gpio_refclk0_i</code>
GPIO1	Q0REF_T/C_IN1	Q0 REFIN1	<code>gpio_refclk1_i</code>

3.5.3 Other Devices

For other devices, the SerDes supports four reference clocks, and all are from dedicated SerDes reference clock inputs. Each of Quad0 and Quad1 contains two reference clocks. Reference clocks can be shared across quads, but only one reference clock is allowed to cross quads in the same configuration. Table 3-7 shows the mapping between the schematic package and reference clocks on the IP interface.

Table 3-7 Reference Clock Mapping for Other Devices

Reference Clock	Schematic Package	IP GUI Option	IP Pin
Quad0 Refclk0	Q0_REFCLKP/M_0	Q0 REFCLK0	-
Quad0 Refclk1	Q0_REFCLKP/M_1	Q0 REFCLK1	-

Reference Clock	Schematic Package	IP GUI Option	IP Pin
Quad1 Refclk0	Q1_REFCLKP/M_0	Q1 REFCLK0	-
Quad1 Refclk1	Q1_REFCLKP/M_1	Q1 REFCLK1	-

4 Port List

The IO port of Gowin QSGMII IP is shown in Figure 4-1.

The "chx" in the signal names in the table and the figure below take the values "ch0", "ch1", "ch2", and "ch3", corresponding to the four SGMII interfaces.

Figure 4-1 Gowin QSGMII IP IO Port Diagram

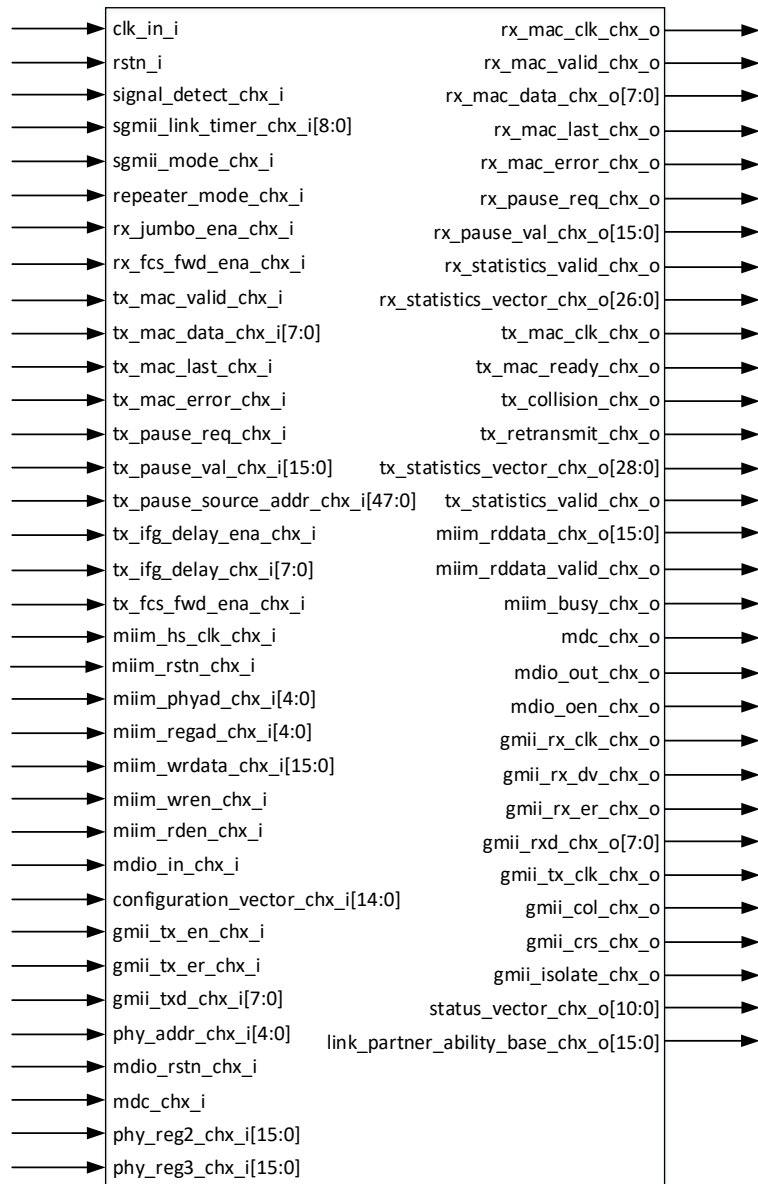


Table 4-1 Gowin QSGMII IP IO Port List

Signal	I/O	Data Width	Description	Clock Domain
Clock input				–
clk_in_i	input	1	Continuous clock signal with frequency not higher than 50MHz	–
Reset				–
rstn_i	input	1	Reset signal, active-low	–
IP Configuration				–
signal_detect_chx_i	input	1	The signal detection function configuration, and it is in combination with configuration_vector_chx_i[1] to control the data synchronization,	MAC layer: rx_mac_clk_chx_o PHY layer:

Signal	I/O	Data Width	Description	Clock Domain
			and it is recommended to be 1'b1. 1: Enable signal detection 0: Disable signal detection	gmii_rx_clk_ch x_o
sgmii_link_timer_chx_i	input	9	Link time in SGMII protocol, 9'd48 recommended	
sgmii_mode_chx_i	input	1	SGMII mode selection signal 1: Media Mode 0: System Mode	
repeater_mode_chx_i	input	1	Repeater mode selection signal, 1'b0 recommended 1: Enable repeater mode 0: Disable repeater mode	
configuration_vector_chx_i	input	15	Function configuration signal	
IP Status				
status_vector_chx_o	output	11	Function status indication	MAC layer: rx_mac_clk_ch x_o
link_partner_ability_base_chx_o	output	16	Partner configuration register information indication	PHY layer: gmii_rx_clk_ch x_o
GMII Interface				-
gmii_rx_clk_chx_o	output	1	GMII RX clock	gmii_rx_clk_ch x_o
gmii_rx_dv_chx_o	output	1	GMII RX enable	
gmii_rxd_chx_o	output	8	GMII RX data	
gmii_rx_er_chx_o	output	1	GMII RX error	
gmii_tx_clk_chx_o	output	1	GMII TX clock	gmii_tx_en_ch x_i
gmii_tx_en_chx_i	input	1	GMII TX enable	
gmii_txd_chx_i	input	8	GMII TX data	
gmii_tx_er_chx_i	input	1	GMII TX error	
gmii_col_chx_o	output	1	GMII collision signal, and this signal is valid only in half duplex	-
gmii_crs_chx_o	output	1	GMII carrier signal, and this signal is valid only in half duplex	
gmii_isolate_chx_o	output	1	GMII transmission isolation	gmii_rx_clk_ch x_o
MAC Layer Interface				-
rx_mac_clk_chx_o	output	1	Receive Clock	rx_mac_clk_ch x_o
rx_mac_valid_chx_o	output	1	RX enable	
rx_mac_data_chx_o	output	8	RX Data	
rx_mac_last_chx_o	output	1	The indication of receiving last byte	
rx_mac_error_chx_o	output	1	The indication of receiving frame with error	
rx_statistics_valid_chx_o	output	1	The indication of receiving valid	

Signal	I/O	Data Width	Description	Clock Domain
			statistics	
rx_statistics_vector_chx_o	output	27	Receive the statistics information	
tx_mac_clk_chx_o	output	1	Transmit clock	tx_mac_clk_chx_o
tx_mac_valid_chx_i	input	1	TX enable	
tx_mac_data_chx_i	input	8	TX Data	
tx_mac_last_chx_i	input	1	The indication of transmitting last byte	
tx_mac_error_chx_i	input	1	The indication of transmitting frame with error	
tx_mac_ready_chx_o	output	1	Transmit a handshake signal, and it indicates that tx_mac_data_chx_i is received with the value of 1.	
tx_collision_chx_o	output	1	Collision indication signal for TX. When the value is 1, it indicates that there is a collision in this transmission and the user needs to end this transmission immediately. This signal is valid only in half duplex.	
tx_retransmit_chx_o	output	1	Re-transmit indication signal, which appears with tx_collision_chx_o at the same time, and the value of 1 means that this frame needs to be re-transmitted. This signal is valid only in half duplex.	
tx_statistics_valid_chx_o	output	1	The indication of valid transmit statistics	
tx_statistics_vector_chx_o	output	29	Transmit statistics information	
MAC Layer Configuration				–
rx_fcs_fwd_ena_chx_i	input	1	Receive FCS Forward 1: Enable receiving FCS Forward 0: Disable receiving FCS Forward	rx_mac_clk_chx_o
rx_jumbo_ena_chx_i	input	1	Receive Jumbo 1: Enable receiving Jumbo 0: Disable receiving Jumbo	
rx_pause_req_chx_o	output	1	The indication of receiving pause frame	
rx_pause_val_chx_o	output	16	Receive parameter field of pause frame, which represents the pause time required by the side.	
tx_fcs_fwd_ena_chx_i	input	1	Transmit FCS Forward 1: Enable transmitting FCS Forward 0: Disable transmitting FCS	tx_mac_clk_chx_o

Signal	I/O	Data Width	Description	Clock Domain
			Forward	
tx_ifg_delay_ena_chx_i	input	1	Transmit the minimum IFG configuration enable: 1: Enable the minimum IFG configuration 0: Disable minimum IFG configuration, and the default minimum IFG is 12 bytes	
tx_ifg_delay_chx_i	input	8	Transmit minimum IFG: When tx_ifg_delay_ena_chx_i is 1, the minimum IFG transmitted by IP is determined by tx_ifg_delay_chx_i. When tx_ifg_delay_chx_i is less than 8, the minimum IFG is 8; When tx_ifg_delay_chx_i is greater than or equal to 8, the minimum IFG is set by the user. When tx_ifg_delay_ena_chx_i is 0, this setting is invalid.	
tx_pause_req_chx_i	input	1	Transmit pause frame enable signal	
tx_pause_val_chx_i	input	16	Transmit the parameter field of pause frame, which means the counterpart needs to pause time.	
tx_pause_source_addr_chx_i	input	48	Transmit the source address of pause frame	
Management Interface				–
miim_hs_clk_chx_i	input	1	Management module clock input (MAC layer)	miim_hs_clk_chx_i
miim_rstn_chx_i	input	1	Management module reset input (MAC layer)	
miim_phyad_chx_i	input	5	PHY address (MAC layer)	
miim_regad_chx_i	input	5	Register address (MAC layer)	
miim_wrdata_chx_i	input	16	Write data (MAC layer)	
miim_wren_chx_i	input	1	Write enable (MAC layer)	
miim_rden_chx_i	input	1	Read enable (MAC layer)	
miim_rddata_chx_o	output	16	Read data (MAC layer)	
miim_rddata_valid_chx_o	output	1	Read data valid (MAC layer)	
miim_busy_chx_o	output	1	MIIM interface status indication (MAC layer) 1: Reading/Writing 0: Idle	
mdc_chx_o	output	1	MDC clock output (MAC layer)	MAC layer: miim_hs_clk_chx_i
mdio_in_chx_i	input	1	MDIO input (MAC layer, PHY layer)	
mdio_out_chx_o	output	1	MDIO output (MAC layer, PHY	

Signal	I/O	Data Width	Description	Clock Domain
			layer)	PHY layer: mdc_chx_i
mdio_oen_chx_o	output	1	MDIO output enable (MAC layer, PHY layer)	
phy_addr_chx_i	input	5	PHY address (PHY layer)	mdc_chx_i
mdio_rstn_chx_i	input	1	MIIM reset (PHY layer)	
mdc_chx_i	input	1	MDC clock input (PHY layer)	
phy_reg2_chx_i	input	16	Register data with address 0x2 (PHY layer)	
phy_reg3_chx_i	input	16	Register data with address 0x3 (PHY layer)	

5 Parameter Configuration

You can configure the static parameters of Gowin QSGMII IP according to the design requirements, as shown in Table 5-1.

Table 5-1 Gowin QSGMII IP Parameter

Name	Description	Option
PHY Configuration		
Channel Selection	Lane selection	- For GW5AT-15 devices, Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3 - For GW5AT-60 devices: Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3 - For other devices: Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2, Q1 Lane3
Loopback Mode	Loopback mode selection	OFF, LB_NES, LB_FES, LB_ENC
Reference Clock Source	Reference clock source selection	- For GW5AT-15 devices, Q0 REFCLK0, Q0 REFCLK1, Q0 REFIN, MCLK - For GW5AT-60 device: Q0 REFCLK0, Q0 REFCLK1, Q0 REFCLK2, Q0 REFCLK3, SERDES Q0CLKIN0, SERDES Q0CLKIN1, SERDES Q0CLKIN2, SERDES Q0CLKIN3, Q0 REFIN0, Q0 REFIN1 - For other devices: Q0 REFCLK0, Q0 REFCLK1, Q1 REFCLK0, Q1 REFCLK1
Reference Clock Frequency	Reference clock frequency setting	User input
Line Rate	Line rate	The default is 5.0 Gbps, and it cannot be configured.
PLL Selection	PLL selection	QPLL0, QPLL1, CPLL
MAC Configuration		
Enable MAC	Ethernet MAC layer enable	Check/Uncheck
Enable PHY MIIM	Ethernet PHY MIIM interface enable, used to configure	Check/Uncheck

Name	Description	Option
	registers in the PHY layer	
MIIM Clock Divider	miim_hs_clk_chx_i input clock division value, and the divided clock is output to mdc_chx_o as the management interface clock output, only used when Ethernet MAC layer enabled. If this option is less than 2, the actual frequency value is 2; If this option is greater than or equal to 2, the actual frequency value is the input value.	User input with range from 0~255
AFE Configuration		
Differential Swing	Configure TX differential signal swing Vdiffpp, $V_{diffpp}=2*V_{diff}$	900mV,852mV,804mV,756mV,708mV,660mV,612mV,564mV,516mV,468mV,420mV,372mV,324mV,276mV,228mV,180mV
FFE Mode	Configure TX FFE mode ● Auto: Automatic mode ● Manual: Manual mode	Auto, Manual
Cm	Transmit FFE pre-cursor	User input with range of 0~19
C0	Transmit FFE main-cursor	Automatic calculation with range of 21~40
C1	Transmit FFE p-cursor	User input with range of 0~19
SD Threshold	Receive differential signal SD threshold	25mV,50mV,75mV,100mV,125mV,150mV,175mV,200mV
Equalization Mode	Receive Equalization ● Auto: Automatic mode ● Manual: Manual mode	Auto, Manual
ATT	Adjust the intermediate frequency amplification during reception. A smaller value indicates greater attenuation.	User input with range of 0~10
BOOST	Adjust the high-frequency amplification during reception. A larger value indicates greater gain.	User input with range of 0~15
BIAS	Configure the amplification parameters of the SerDes for RX signals. A higher value indicates stronger signal amplification.	User input with range of 0~15

Note!

The line rate and reference clock are subject to certain constraints. It is essential to ensure that the reference clock can generate the specified line rate. Alternatively, you can use the "Calculate" button to perform a check.

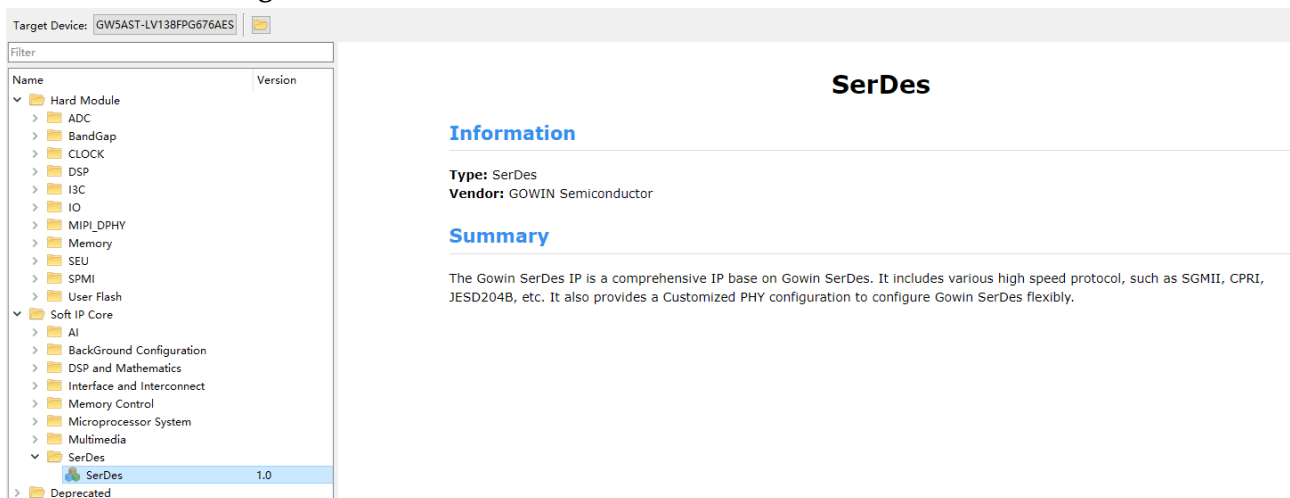
6 Interface Configuration

You can invoke and configure Gowin QSGMII IP using the IP Core Generator tool in the IDE. Taking MAC layer interface as an example, this section introduces the configuration interface, the configuration process, and the configuration options.

1. Open IP Core Generator

After creating the project, click the "Tools" tab in the upper left, click "IP Core Generator" to open Gowin IP Core Generator via the drop-down list, as shown in Figure 6-1.

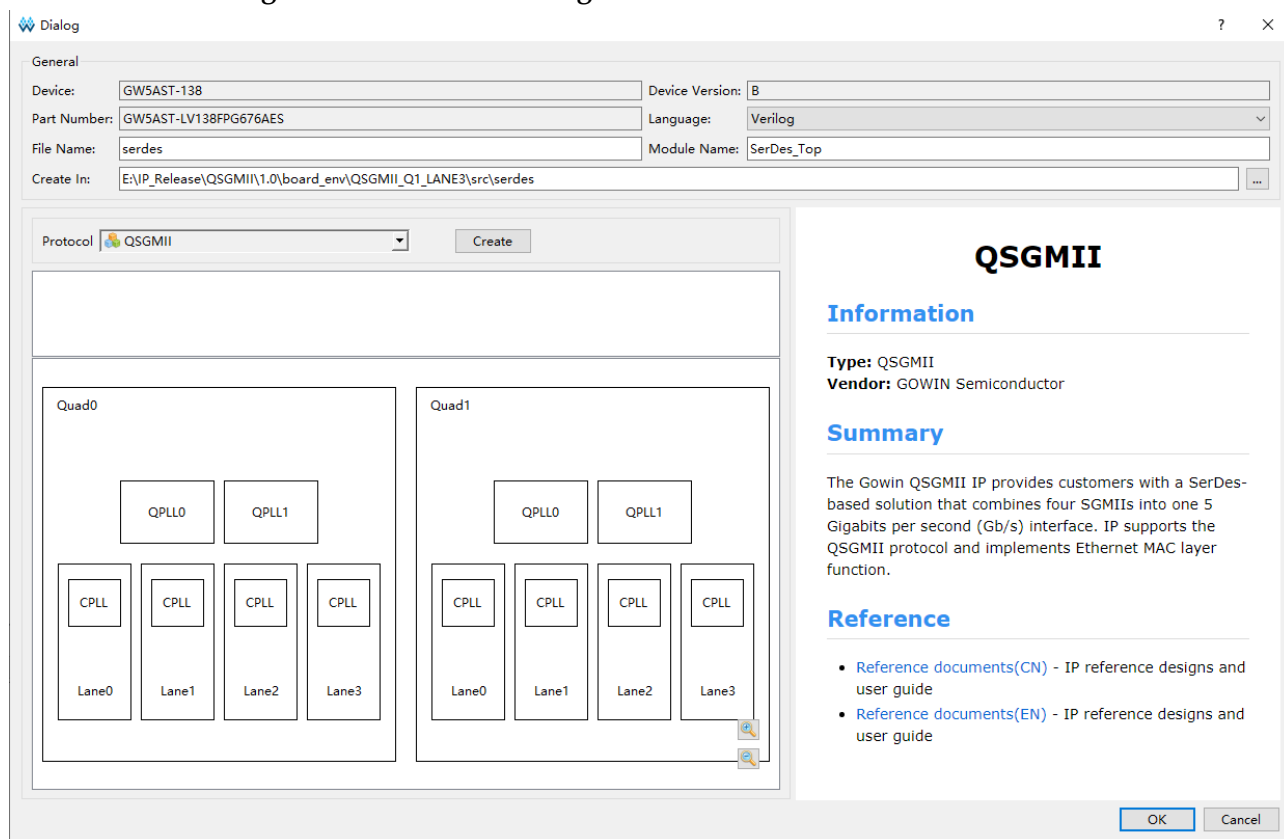
Figure 6-1 IP Core Generator



2. Open SerDes IP Configuration Interface

Select "SerDes" in IP Core Generator and open SerDes IP configuration interface, as shown in Figure 6-2.

Figure 6-2 SerDes IP Configuration Interface



First configure "General" tab in the SerDes IP interface.

- Device, Device Version, Part Number: Part number settings, determined by the current project, and the user can not set it.
- Language: Support Verilog and VHDL, choose the language as requirements, and the default is Verilog.
- File Name, Module Name, Create In: Display SerDes file name, module name and the generated file path settings.

You can select the protocol in "Protocol" option according to your needs. Click "Create" button on the right to open the protocol configuration, and it displays the current protocols supported by SerDes IP and the corresponding Quad, PLL and Lane usage; on the right side, it displays the information about the selected protocol, including "Information", "Summary" and "Reference".

3. Open QSGMII IP Configuration Interface

In the SerDes IP configuration interface, select "QSGMII" in the "Protocol" option, and click the "Create" button on the right to open the QSGMII IP configuration interface.

On the left side of the configuration interface displays the port diagram of QSGMII IP, and on the right side displays QSGMII IP configuration options, which include PHY Configuration, MAC Configuration, and AFE Configuration, as shown in Figure 6-3, Figure 6-4, and Figure 6-5

respectively, and the descriptions of parameters are shown in Table 5-1.

Figure 6-3 PHY Configuration

IP Customization

QSGMII

General

Device:GW5AST-138Device Version:B

Part Number:GW5AST-LV138FPG676AESLanguage:Verilog

File Name:qsgmiiModule Name:QSGMII_Top

Create In:II\1.1\ref_design\Gowin_QSGMII_IP_RefDesign\project\src\serdes\qsgmii

PHY ConfigurationMac ConfigurationAFE Configuration

Channel SelectionQ1 Lane3

Loopback Mode:OFF

Line Rate:5Gbps

Refclk Selection

Reference Clock Source:Q1 REFCLK0

Reference Clock Frequency:100MHz

PLL Selection:QPLL1

Calculate

OKCancel

Figure 6-4 MAC Configuration

IP Customization

QSGMII

General

Device: GW5AST-138 Device Version: B

Part Number: GW5AST-LV138FPG676AES Language: Verilog

File Name: qsgmii Module Name: QSGMII_Top

Create In: II\1.1\ref_design\Gowin_QSGMII_IP_RefDesign\project\src\serdes\qsgmii

PHY Configuration **Mac Configuration** **AFE Configuration**

☒ Enable MAC

☐ Enable PHY MIIM

MIIM Clock Divider: 20 (0~255)

OK Cancel

Figure 6-5 AFE Configuration

QSGMII

IP Customization

General

Device: GW5AST-138 Device Version: B

Part Number: GW5AST-LV138FPG676AES Language: Verilog

File Name: qsgmii Module Name: QSGMII_Top

Create In: II\1.1\ref_design\Gowin_QSGMII_IP_RefDesign\project\src\serdes\qsgmii

PHY Configuration **Mac Configuration** **AFE Configuration**

TX

Differential Swing: 900mV

FFE Mode

FFE Mode: Auto

Cm: 0 (0~19)

C0: 40 (21~40)

C1: 0 (0~19)

RX

SD Threshold: 100mV

Equalization

Equalization Mode: Auto

ATT: 7 (0~10)

BOOST: 9 (0~15)

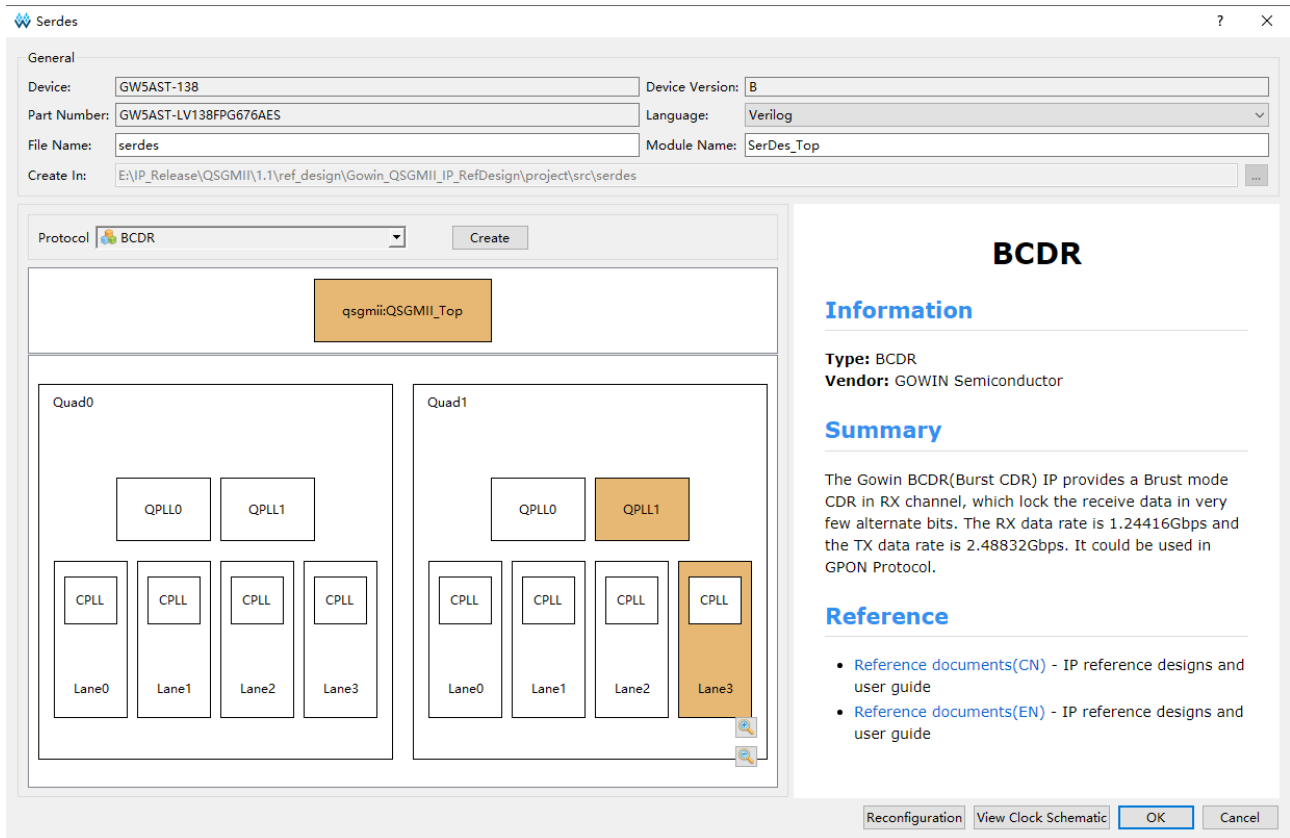
BIAS: 7 (0~15)

OK Cancel

4. IP Generation

After completing QSGMII IP configuration, click "OK" button at the bottom right corner of the interface to generate files of the QSGMII IP, and return to the SerDes IP configuration interface, and then the SerDes IP configuration interface displays the current generated IP and the corresponding Quad, PLL, and Lane usage, as shown in Figure 6-6.

Figure 6-6 QSGMII IP in SerDes IP Configuration Interface



Then, click "OK" button at the bottom right corner of the interface to generate SerDes IP files and complete the whole QSGMII IP generation.

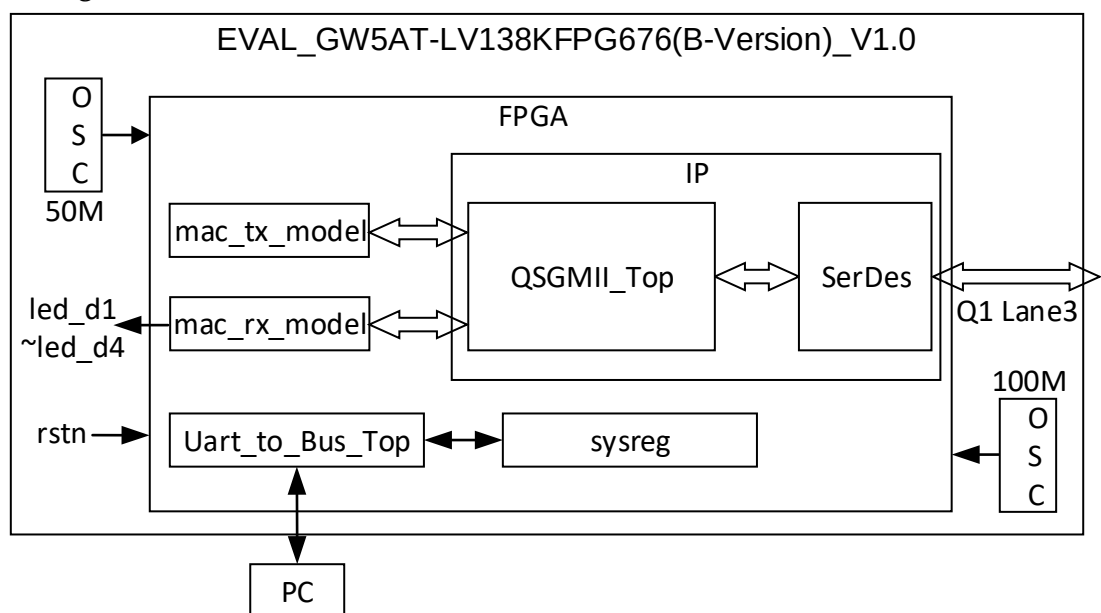
7 Reference Design

For more information, please see the QSGMII IP [reference design](#) at Gowin website.

7.1 Hardware Platform

The hardware platform is as shown in Figure 7-1.

Figure 7-1 Hardware Platform



One such reference example is implemented on a GW5AT board with the following hardware conditions.

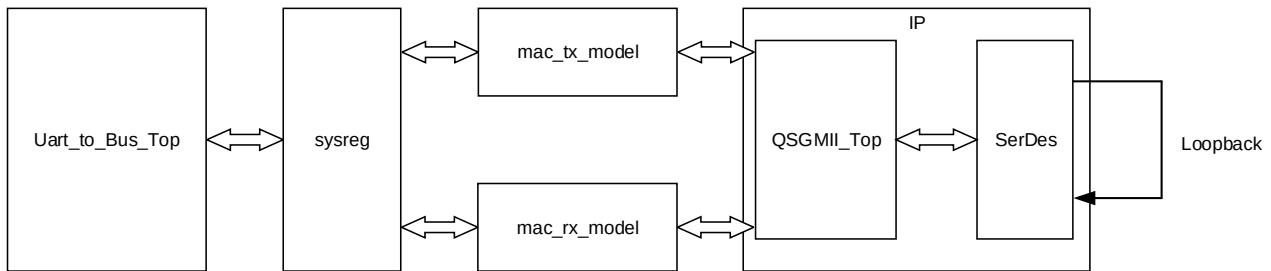
1. SerDes reference clock is generated from the on-board crystal oscillator with 100 MHz, located at Refclk0 of Quad1.
2. SerDes uses Lane3 of Quad1 for data transmission.
3. On-board 50MHz crystal oscillator serves as the input clock for the QSGMII IP.
4. SW1 is used as a reset signal rstn to perform a reset operation on the internal module, active-low.
5. LED D1 (led_d1) indicates the Link Up status of the IP, being constantly

on means that the IP links up, which can be used for data transmission.

6. LED D2 (led_d2) indicates the data transmission status of the IP, being constantly on means that the IP is continuously sending and receiving data.
7. LED D3 (led_d3) indicates the status of Ethernet frames received by the IP, being constantly on means that the IP receives abnormal Ethernet frames.
8. LED D4 (led_d4) indicates the status of Pause frames received by the IP, being constantly on means that the IP receives abnormal Pause frames.
9. The 50MHz on-board crystal oscillator goes through PLL to generate a 10MHz clock, used for communication between the PC-side serial port assistant and the FPGA, with a baud rate of 115200.

7.2 Implementation Diagram

Figure 7-2 Implementation Diagram of Reference Design



The `Uart_to_Bus_Top` module parses the custom bus protocol, then converts it into local system configuration registers using the `sysreg` module to configure and provide feedback on IP functions.

The `QSGMII_Top` module receives data from `mac_tx_model`, loops it back through the TX interface of `SerDes` to the RX interface, and finally, `QSGMII_Top` sends the looped-back data to `mac_rx_model`. The main modules are as follows:

- `Uart_to_Bus_Top` module: Serial-to-bus module that converts serial commands from the serial assistant or upper computer into bus control timing.
- `sysreg` module: Generates local system configuration registers.
- `mac_tx_model` module: Used to generate the IP transmission timing, transmits Ethernet frames and Pause frames.
- `mac_rx_model` module: Used to analyze received Ethernet frames and Pause frames from the IP, and provides feedback on abnormal detection.
- `QSGMII_Top` module: Configured according to the parameters in Figure 6-3, Figure 6-4, and Figure 6-5.

7.3 Bus Protocol and Address Planning

The core module of Gowin UART to Bus IP is an instruction parser that can be used to access the internal bus through UART interface. The read and write bus protocols are specified as follows:

Write bus "W AAAA BBBBBBBB"

Read bus "R AAAA"

The read bus will return the following command "G AAAA BBBBBBBB"

W means write, R means read, and G means read result return. They are separated by spaces, and you need to enter a carriage return at the end. AAAA means address, 16 bits; BBBBBBBBBB means data, 32 bits. For more details, you can see [IPUG1022, Gowin UART to Bus IP User Guide](#).

In this reference design, the UART to Bus IP parameters are configured as follows

Figure 7-3 UART to Bus IP Core Parameter Setting 1

Basic Slave Address

Bus Config

Bus Mode: ☐ APB ☒ Local

Address Width: 16 bits

Data Width: 32 bits

Timeout Value: 16 clocks

Uart Config

Clock Frequency: 10 (1.000~200.000)MHz

Baudrate Value: 115200

Generation Config

☒ Disable I/O Insertion

Figure 7-4 UART to Bus IP Core Parameter Setting 2

Basic Slave Address

Slave Config

Slave	Base Address	High Address
☒ slave0	0x0000	0x00FF
☐ slave1	0x0100	0x01FF
☐ slave2	0x0200	0x02FF
☐ slave3	0x0300	0x03FF
☐ slave4	0x0400	0x04FF
☐ slave5	0x0500	0x05FF
☐ slave6	0x0600	0x06FF
☐ slave7	0x0700	0x07FF
☐ slave8	0x0800	0x08FF
☐ slave9	0x0900	0x09FF

The detailed register address definitions in the reference project are as follows:

Table 7-1 Register Address Definition

Address (32bits)	Default	W/R	Description
0x0000	0x00000000	WR	[3:0]: Control the method of changing the data field length. The order from high to low corresponds to Port3, Port2, Port1, and Port0. 1: Keep the data field length for each frame as DATA_LENGTH_MAX. 0: Allow the data field length to vary between 0 and DATA_LENGTH_MAX, and the difference between adjacent frames is DATA_LENGTH_INCREASE.
0x0001	0x00000000	WR	[3:0]: Control whether to transmit one frame of Pause Frame, in order from high to low corresponding to Port3, Port2, Port1, and Port0 respectively. 1: Not transmit Pause Frame 0: Transmit Pause Frame
0x0002	0x00000000	WR	[3:0]: Clear detection results, in order from high to low corresponding to Port3, Port2, Port1, and Port0 respectively. 1: Clear abnormal results or transmitted frame count 0: Start re-detection
0x0010	0x00000000	WR	[3:0]: IP reset function (main_reset), in order from high to low corresponding to Port3, Port2, Port1, and Port0 respectively. 1: Reset 0: Release reset
0x0011	0x000000AA	WR	[7]/[5]/[3]/[1]: Auto-negotiation enable (an_enable), in order from high to low corresponding to Port3, Port2, Port1, and Port0 respectively. 1: Enable auto-negotiation 0: Disable auto-negotiation [6]/[4]/[2]/[0]: Restart auto-negotiation, in order from high to low corresponding to Port3, Port2, Port1, and Port0, respectively. 1->0: Restart auto-negotiation
0x0020	0x0006666F	WR	[18]/[14]/[10]/[6]: Duplex mode of SGMII, in order from high to low corresponding to Port3, Port2, Port1, and Port0, respectively. 1: Full duplex 0: Half duplex [17:16]/[13:12]/[9:8]/[5:4]: Rate of SGMII, in order from high to low corresponding to Port3, Port2, Port1, and Port0 respectively. 1x: 1000M 01: 100M 00: 10M [3:0]: Mode Selection, in order from high to low corresponding to Port3, Port2, Port1, and Port0 respectively. 0: System Mode for SGMII 1: Media Mode for SGMII
0x0021	0x00300030	WR	[24:16]: SGMII link time setting, and the default is 48 for Port1. [8:0]: SGMII link time setting, and the default is 48 for Port0.

Address (32bits)	Default	W/R	Description
0x0022	0x00300030	WR	[24:16]: SGMII link time setting, and the default is 48 for Port3. [8:0]: SGMII link time setting, and the default is 48 for Port2.
0x0030	0x00000001	WR	[11]/[9]/[7]/[5]: Data transmission continuous mode, equivalent to multiple bursts, in order from high to low corresponding to Port3, Port2, Port1, and Port0. 1: Execute data transmission 0: Stop data transmission [10]/[8]/[6]/[4]: Burst mode for data transmission, sending FRM_NUM_MAX Ethernet frames and one Pause frame in a single burst (controlled by 0x0001 to determine whether to send a Pause frame), in order from high to low corresponding to Port3, Port2, Port1, and Port0 respectively. 1->0: Execute a burst [0]: Reset all modules except Uart_to_Bus_Top and sysreg module 1: Release reset 0: Reset
0x0080	-	R	[31]/[23]/[15]/[7]: Self-negotiation complete flag, in order from high to low corresponding to Port3, Port2, Port1, and Port0 respectively. [26]/[18]/[10]/[2]: Received data exception, in order from high to low, corresponding to Port3, Port2, Port1, and Port0 respectively. [25]/[17]/[9]/[1]: Received Pause frame exception, in order from high to low corresponding to Port3, Port2, Port1, and Port0 respectively. [24]/[16]/[8]/[0]: Received Ethernet frame exception, in order from high to low corresponding to Port3, Port2, Port1, and Port0 respectively.
0x0081	-	R	[26]/[18]/[10]/[2]: The partner's duplex mode in SGMII, in order from high to low corresponding to Port3, Port2, Port1, and Port0 respectively. 1: Full duplex 0: Half duplex [25:24]/[17:16]/[9:8]/[1:0]: The partner's rate in SGMII, in order from high to low corresponding to Port3, Port2, Port1, and Port0 respectively. 10: 1000M 01: 100M 00: 10M
0x0090	-	R	[15:12]: IP Link Up status, in order from high to low corresponding to Port3, Port2, Port1, and Port0 respectively. [11]/[9]/[7]/[5]: Reset status of mac_rx_model module, in order from high to low corresponding to Port3, Port2, Port1, and Port0 respectively. [10]/[8]/[6]/[4]: Reset status of mac_tx_model module, in order from high to low corresponding to Port3, Port2, Port1, and Port0 respectively. [3]: Default 1. [2]: Reset status of IP.

Address (32bits)	Default	W/R	Description
			[1]: Reset status of Uart_to_Bus_Top and sysreg modules. [0]: Lock status of pll_uart.
0x0091	-	R	[7:4]: Frame count overflow flag for received Ethernet data, indicating exceeding the range, in order from high to low corresponding to Port3, Port2, Port1, and Port0 respectively. [3:0]: Frame count overflow flag for transmitted Ethernet data, indicating exceeding the range, in order from high to low corresponding to Port3, Port2, Port1, and Port0 respectively.
0x00A0	-	R	[31:0]: Frame count for transmitted Ethernet data, corresponding to Port0.
0x00A1	-	R	[31:0]: Frame count for transmitted Ethernet data, corresponding to Port1.
0x00A2	-	R	[31:0]: Frame count for transmitted Ethernet data, corresponding to Port2.
0x00A3	-	R	[31:0]: Frame count for transmitted Ethernet data, corresponding to Port3.
0x00B0	-	R	[31:0]: Frame count for received Ethernet data, corresponding to Port0.
0x00B1	-	R	[31:0]: Frame count for received Ethernet data, corresponding to Port1.
0x00B2	-	R	[31:0]: Frame count for received Ethernet data, corresponding to Port2.
0x00B3	-	R	[31:0]: Frame count for received Ethernet data, corresponding to Port3.

7.4 On-Board Testing

7.4.1 Operation Description

This example project has been tested on the EVAL_GW5AT-LV138KFPG676 (B-Version) V1.0 development board. If you don't have this development board but want to run this reference design, you will need to modify the QSGMII IP settings, including Channel Selection, Reference Clock Source, Reference Clock Frequency, and PLL Selection, based on the actual configuration of your board. Additionally, you should reconfigure the pll_uart according to the input clock and reallocate the clock input pins, reset pins, and LED pins for testing.

After the modification, the Bit file is generated, and download it to the FPGA to start testing.

7.4.2 Operating Flow

The steps are as follows:

1. Use RF cables to externally loop back TX and RX ends.
2. After the Bit file is downloaded to the FPGA, you first need to check if the serial command works.

Input: W 0003 F5A1490D

Input: R 0003

Return: G 0003 F5A1490D

Then the communication between PC and FPGA is OK, otherwise, you have to check the reason why they can't communicate first before proceeding to the next step.

3. Check the status of LED D1; if it is constantly on, it indicates that the QSGMII IP has completed negotiation in Media Mode at a rate of 1000Mbps and is ready for data transmission. Otherwise, you need to troubleshoot unsuccessful negotiation before proceeding.

4. Retrieve the current internal detection of the FPGA.

Input: R 0080

Return: G 0080 80808080

This indicates that all ports of the IP have negotiated successfully, and no abnormal reception or transmission data has been detected.

5. Set the Ethernet data transfer, with maximum payload for each frame and no Pause frames.

Input: W 0000 0000000F

Input: W 0001 0000000F

6. Execute data transfer (continuous mode) and observe that LED D2 is constantly on.

Input: W 0030 00000AA1

7. After a while, stop data transfer and observe that LED D2 is constantly off.

Input: W 0030 00000001

8. Observe that LED D3 and D4 is constantly off, indicating that the IP data transfer is normal.

9. Set the IP to Media Mode with rate 100M.

Input: W 0020 0005555F

10. Restart auto-negotiation

Input: W 0011 000000FF

Input: W 0011 000000AA

11. Repeat steps 3-8.

12. Set the IP to Media Mode with rate 10M.

Input: W 0020 0004444F

13. Restart auto-negotiation

Input: W 0011 000000FF

Input: W 0011 000000AA

14. Repeat steps 3-8.

15. Observe the indicator LED during the on-board testing to confirm that data transmission is normal.

8 File Delivery

The delivery files for the Gowin QSGMII IP includes the documents, the design source code, and the reference design.

8.1 Documentation

The folder mainly contains the user guide in PDF version.

Table 8-1 Document List

Name	Description
IPUG1087, Gowin QSGMII IP User Guide	Gowin QSGMII IP User Guide, namely this one

8.2 Design Source Code (Encryption)

The Encryption Code Folder contains the RTL encryption code of Gowin QSGMII IP used for the GUI, to generate the IP cores as needed.

Table 8-2 Gowin QSGMII IP Design Source Code List

Name	Description
ge_pcs_qsgmii_wrap.v	The top-level file of the IP core, which provides users with interface information, encrypted.
ge_pcs_qsgmii.v	IP core RTL design File, encrypted
ge_constants.v	Local static parameter configuration file, encrypted
static_macro_define.v	Local static parameter configuration file, not encrypted
define.vh	IP configuration file, generated form GUI
parameter.vh	IP configuration file, generated form GUI

8.3 Reference Design

The Gowin QSGMII IP RefDesign folder contains the netlist file for Gowin QSGMII IP, user reference design, constraints file, top-level file, and project file, etc.

Table 8-3 Gowin QSGMII IP RefDesign Folder Content List

Name	Description
top.v	The top module of reference design
fpga_project.cst	Project physical constraints file

Name	Description
fpga_project.sdc	Project timing constraints file
serdes	SerDes IP folder, including SerDes files and QSGMII files
mac_rx_model.v	MAC layer RX signal control module
mac_tx_model.v	MAC layer TX signal control module
uart_to_bus	UART to Bus IP folder, used to convert UART to internal configuration bus
sysreg.v	Local system configuration register module
button.v	Key jitter elimination module
pll_uart	PLL folder, and the onboard 50MHz clock is used to as a reference to generate a 10MHz clock for serial communication

