



Gowin RoraLink 64B66B IP User Guide

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Revision History

Date	Version	Description
02/23/2024	1.0E	Initial version published.
10/25/2025	1.1E	● "AFE" configuration option added. ● Descriptions of "Reference Clock Source" configuration option updated.

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1 About This Guide

1.1 Purpose

Gowin RoraLink 64B66B IP User Guide is to help you learn the features and usage of Gowin RoraLink 64B66B IP by providing descriptions of functions, GUI, and reference design, etc. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.10.03. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com.

- [SUG100, Gowin Software User Guide](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1104, GW5AST series of FPGA Products Data Sheet](#)

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
CB	Channel Bonding
CC	Clock Compensation
CRC	Cyclic Redundancy Code
FPGA	Field Programmable Gate Array
IP	Intellectual Property
NFC	Native Flow Control
PCS	Physical Coding Sublayer
PMA	Physical Medium Attachment
UFC	User Flow Control

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Function Overview

2.1 Overview

Gowin RoraLink 64B66B IP provides users with an extensible, lightweight, high-data-rate link layer transmission solution. It utilizes the 64B/66B encoding and decoding, offering user-friendly data interfaces and flow control interfaces.

Table 2-1 Gowin RoraLink 64B66B IP Overview

Gowin RoraLink 64B66B IP	
Logic Resource	See Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9.01 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features

- Supports 1~8 lanes
- Supports simplex or full-duplex transmission modes
- Supports 64B/66B encoding and decoding
- Supports serial data scrambling and descrambling
- Supports RX Channel Bonding (CB) alignment and clock adjustment
- Supports low-overhead transmission
- Supports automatic initialization and channel management
- Supports big-endian or little-endian
- Supports CRC32
- Provides user-friendly data interfaces and flow control interfaces

2.3 Resource Utilization

Gowin RoraLink 64B66B IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW5AT series of FPGA as an instance, the resource utilization of Gowin RoraLink 64B66B IP is as shown in Table 2-2.

Table 2-2 Gowin RoraLink 64B66B IP Resource Utilization

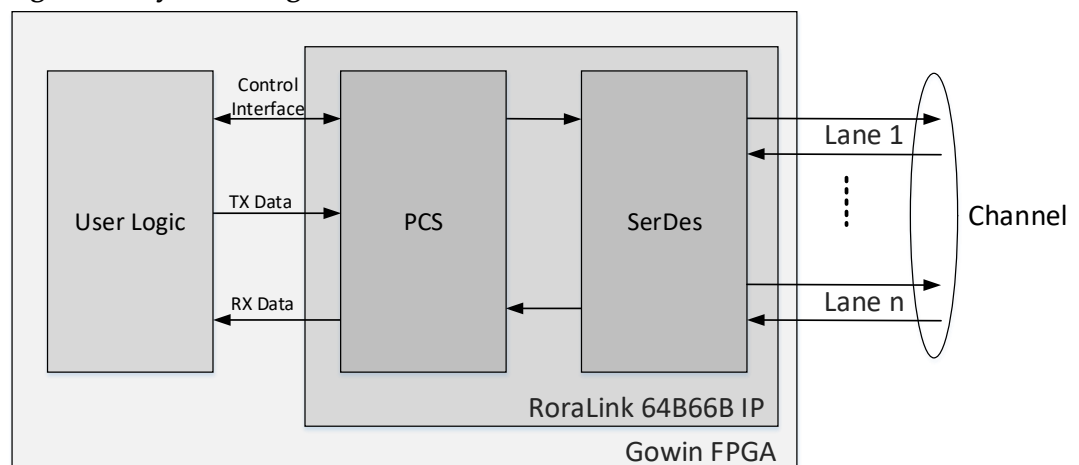
Lane Width	Dataflow Mode	Interface	Resource Utilization		
			REG	LUT	BSRAM
1	Duplex	Framing	4062	2946	2
		Streaming	3881	2767	2
	RX-only Simplex	Framing	2851	1612	2
		Streaming	2695	1497	2
	TX-only Simplex	Framing	1574	1443	0
		Streaming	1574	1447	0
	TX/RX Simplex	Framing	4242	3162	2
		Streaming	4059	2986	2
2	Duplex	Framing	7684	5679	4
		Streaming	7348	5376	4
	RX-only Simplex	Framing	5429	3147	4
		Streaming	5135	2933	4
	TX-only Simplex	Framing	2988	2820	0
		Streaming	2988	2826	0
	TX/RX Simplex	Framing	7915	5995	4
		Streaming	7576	5669	4
4	Duplex	Framing	14906	11126	8
		Streaming	14264	10555	8
	RX-only Simplex	Framing	10564	6171	8
		Streaming	9997	5773	8
	TX-only Simplex	Framing	5816	5568	0
		Streaming	5816	5587	0
	TX/RX Simplex	Framing	15239	11620	8
		Streaming	14592	11003	8

3 Functional Description

3.1 System Block Diagram

The system diagram of Gowin RoraLink 64B66B IP is shown in Figure 3-1. The IP comprises a SerDes module and a PCS module, invoking SerDes hard core as PMA for the protocol, while the IP can implement the PCS layer. The SerDes module transmits data encoded with 64B/66B, and users can connect with the counterpart device using 1~8 lanes, utilizing multiple lanes to transmit data for one channel. The PCS module can implement 64B/66B encoding/decoding, scrambling/descrambling, link initialization, and data transmission.

Figure 3-1 System Diagram



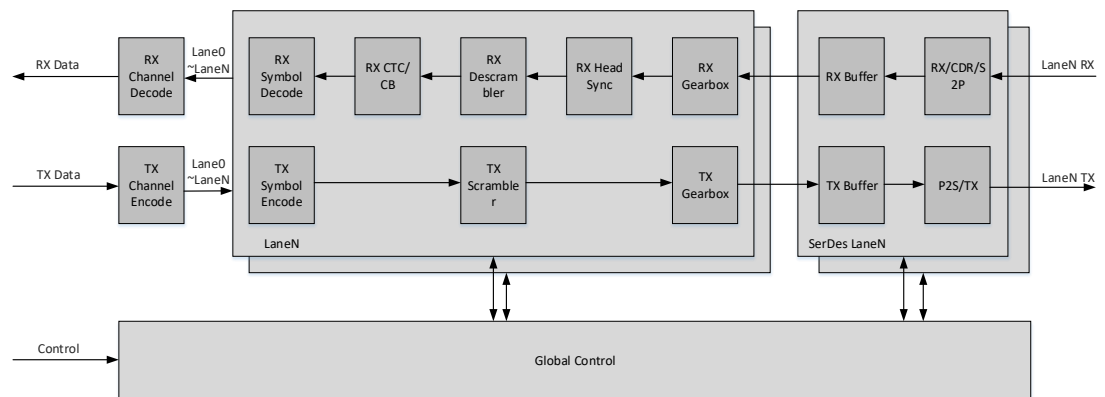
3.2 Operating Frequency

The operating frequency of Gowin RoraLink 64B66B IP is related to the SerDes line rate. When the SerDes width is 64 bits, and the operating clock frequency is calculated as the formula $\text{clock} = \text{line rate} / 64\text{bits}$. For example, if the line rate for a single Lane is 3.125 Gbps, then the operating clock frequency is calculated as follows: $\text{clock} = 3.125 \text{ Gbps} / 64 \text{ bits} = 48.828125 \text{ MHz}$.

3.3 Operating Principles

The structure diagram of Gowin RoraLink 64B66B IP is as shown in Figure 3-2. The functions of each module are described as follows:

- Global Control: Manages channel bonding alignment in the RX, IP initialization, link monitoring, reset, etc.
- TX Data: Users input data; the IP performs data processing and flow control, data scrambling, and gearbox processing, and then sends the data through SerDes.
 - TX Channel Encode: Processes user data, flow control data, user K-characters, etc. This includes interface conversion, flow control, endian conversion, adding CRC fields, etc. The CRC calculation uses the polynomial $G(X) = X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$.
 - TX Symbol Encode: The data outputted by the TX Channel Encode is correspondingly inputted to multiple lanes to add control symbols.
 - TX Scrambler: Scrambles data using the polynomial $G(x) = 1 + x^{39} + x^{58}$, excluding 2-bit sync headers.
 - TX Gearbox: Converts 64-bit and 2-bit sync headers into 64 bits for the SerDes interface.
- RX Data: The IP receives SerDes data, and sends it to users after operations of gearbox, block synchronization, descrambling, clock compensation, channel bonding alignment, and data decoding.
 - RX Gearbox: Converts SerDes-received 64-bit data to 66-bit data.
 - RX Head Sync: Receives and checks whether the 2-bit sync header is locked. If not locked, it collaborates with RX Gearbox to process data and eventually correctly recovers 64-bit data and 2-bit sync headers.
 - RX Descrambler: Reception descrambler module.
 - RX CTC/CB: RX clock adjustment and channel bonding alignment module.
 - RX Symbol Decode: Receives and processes control symbols.
 - RX Channel Decode: The received data is processed and sent to the user, including operations such as removing CRC fields, endian conversion, and interface conversion.

Figure 3-2 Structure Diagram

3.4 User Interface

The user interfaces provided by Gowin RoraLink 64B66B IP are described below:

- Clock Interface: Allows users to input the operating clock of IP Core.
- Reset Interface: Allows users to perform a reset operation on the IP Core, and simultaneously the IP outputs a reset signal to the user-side module.
- Transmit Data Interface: User interface for transmitting data.
- Receive Data Interface: User interface for receiving data.
- NFC Flow Control Interface: Interface for users to perform Native Flow Control (NFC), allowing the receiving party to request its channel partner to transmit idle instead of data.
- UFC Flow Control Interface: Interface for users to perform User Flow Control (UFC), allowing the transmission of short, high-priority control messages through the interface.
- User K-character Interface: User-defined interface for sending and receiving K-characters.
- Status Interface: Includes internal error status of the IP, lane linking status, channel linking status, and CRC verification status.
- SerDes-related interfaces: SerDes reset and SerDes status interfaces.

3.5 Port List

The I/O port diagram of Gowin RoraLink 64B66B IP is shown in Figure 3-3.

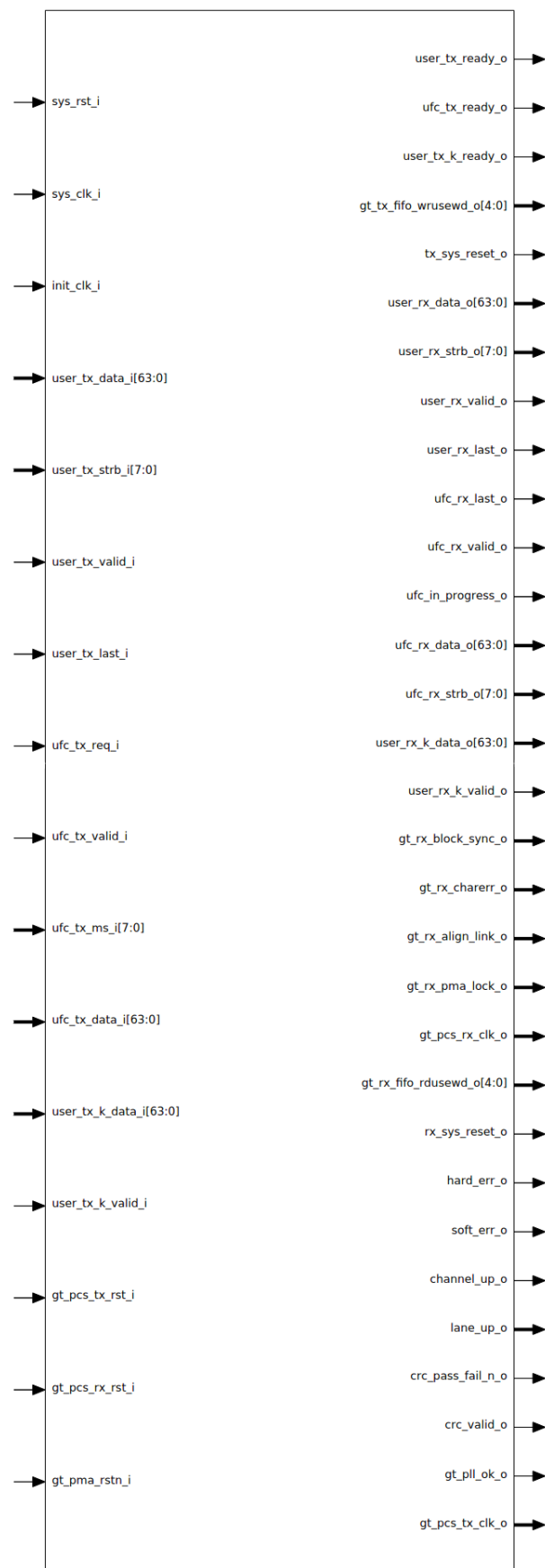
Figure 3-3 Gowin RoraLink 64B66B IP Port Diagram

Table 3-1 I/O List of Gowin RoraLink 64B66B IP

Port Name	I/O	Data Width	Description
Clock and Reset			
sys_rst_i	input	1	Reset signal, active-high.
sys_clk_i	input	1	Operating clock, and you can refer to the clock frequency details described in Section 3.2 Operating Frequency .
init_clk_i	input	1	Input the local crystal oscillator 50MHz clock
reset2fc_o ^[10]	output	1	For reference design only, reset the RX frame detection module, active-high.
reset2fg_o ^[9]	output	1	For reference design only, reset the TX frame generation module, active-high.
tx_sys_reset_o ^[2]	output	1	TX system reset signal, active-high.
rx_sys_reset_o ^[3]	output	1	RX system reset signal, active-high.
User Data Transmission Interface			
user_tx_data_i ^[2]	input	[(64n ^[1] -1):0] or [0:(64n ^[1] -1)]	Transmit user data
user_tx_valid_i ^[2]	input	1	Transmit user data valid indicator, active-high.
user_tx_ready_o ^[2]	output	1	Handshake signal for transmitting user data, and data on the bus is valid when both user_tx_ready_o and user_tx_valid_i are high.
user_tx_strb_i ^[2]	input	[(8n ^[1] -1):0] or [0:(8n ^[1] -1)]	Enable transmitting user data frame-tail byte valid. For example, if user_tx_strb_i is 8'h1f, it indicates that the user_tx_data_i [39:0] is valid, and user_tx_data_i [63:40] is invalid. This signal is only valid when user_tx_valid_i, user_tx_ready_o, and user_tx_last_i are high. Note! This port is only available when the Interface option on the GUI is set to "Framing".
user_tx_last_i ^[2]	input	1	Indicator for transmitting user data frame tail valid; when user_rx_valid_o and user_rx_last_o are high, it indicates the data on the bus is the last data of each frame. Note! This port is only available when the Interface option on the GUI is set to "Framing".
User Data Reception Interface			
user_rx_data_o ^[3]	output	[(64n ^[1] -1):0] or [0:(64n ^[1] -1)]	Receive user data
user_rx_valid_o ^[3]	output	1	Receive user data valid indicator; when it is high, the data on the bus is valid.
user_rx_strb_o ^[3]	output	[(8n ^[1] -1):0] or [0:(8n ^[1] -1)]	Enable receiving user data frame-tail byte valid. For example, if user_rx_strb_o is 8'h1f, it indicates that the user_rx_data_o [39:0] is valid, and user_rx_data_o [63:40] is invalid. This signal is only valid when both user_rx_valid_o and user_rx_last_o are high. Note! This port is only available when the Interface option on the GUI is set to "Framing".
user_rx_last_o ^[3]	output	1	Indicator for receiving user data frame tail valid;

Port Name	I/O	Data Width	Description
			when both user_rx_valid_o and user_rx_last_o are high, it indicates the data on the bus is the last data of each frame. Note! This port is only available when the Interface option on the GUI is set to "Framing".
Native Flow Control Interface			
nfc_valid_i ^[4]	input	1	NFC mode flow control data valid indicator, active-high.
nfc_data_i ^[4]	input	[15:0] or [0:15]	NFC mode flow control data
nfc_ready_o ^[4]	output	1	NFC mode flow control handshake signal; when nfc_ready_o and nfc_valid_i are high, the data on the bus is valid.
User Flow Control TX Interface			
ufc_tx_req_i ^{[2][5]}	input	1	Transmit UFC data request signal, active-high.
ufc_tx_ms_i ^{[2][5]}	input	[7:0] or [0:7]	Transmit UFC data byte count with the range of 0-255. For example, 3 indicates transmitting 4 bytes of UFC data.
ufc_tx_data_i ^{[2][5]}	input	[(64n ^[1] -1):0]or [0:(64n ^[1] -1)]	Transmit UFC data
ufc_tx_valid_i ^{[2][5]}	input	1	Transmit UFC data valid indicator, active-high.
ufc_tx_ready_o ^{[2][5]}	output	1	Transmit UFC data handshake signal; when ufc_tx_ready_o and ufc_tx_valid_i are high, it indicates ufc_tx_data_i on the bus is valid.
User Flow Control RX Interface			
ufc_rx_data_o ^{[3][5]}	output	[(64n ^[1] -1):0]or [0:(64n ^[1] -1)]	Receive UFC data
ufc_rx_strb_o ^{[3][5]}	output	[(8n ^[1] -1):0]or [0:(8n ^[1] -1)]	Enable receiving UFC frame-tail byte valid. For example, if ufc_rx_strb_o is 8'h1f, it indicates that the ufc_rx_data_o [39:0] is valid, and ufc_rx_data_o [63:40] is invalid. This signal is only valid when both ufc_rx_valid_o and ufc_rx_last_o are high.
ufc_rx_last_o ^{[3][5]}	output	1	Indicator for receiving user data frame tail valid; when both ufc_rx_valid_o and ufc_rx_last_o are high, it indicates the data on the bus is the last data of each frame.
ufc_rx_valid_o ^{[3][5]}	output	1	Receive UFC data valid indicator, active-high.
ufc_in_progress_o ^{[3][5]}	output	1	UFC transfer status; when it is low, it indicates that UFC data is currently being received.
User K-character TX Interface			
user_tx_k_data_i ^{[2][6]}	input	[(64n ^[1] -1):0]or [0:(64n ^[1] -1)]	Transmit user K-character data. ● If "Little Endian Support" option checked: user_tx_k_data_i = {{user_k_data[55:0], 4'h0, user_k_blk_no[3:0]}*n^[1]. ● If "Little Endian Support" option not checked, user_tx_k_data_i =

Port Name	I/O	Data Width	Description
			{{4'h0,user_k_blk_no[0:3],user_k_data[55:0]}*n ^[1] }.
user_tx_k_valid_i ^{[2][6]}	input	1	Indicator for transmitting user K-character valid, active-high.
user_tx_k_ready_o ^{[2][6]}	output	1	Handshake signal for transmitting user K-character, active-high; when both user_tx_k_valid_i and user_tx_k_ready_o are high, the data on the bus is valid.
User K-character RX Interface			
user_rx_k_data_o ^{[3][6]}	output	[(64n ^[1] -1):0]or [0:(64n ^[1] -1)]	Receive user K-character - If "Little Endian Support" option checked: user_tx_k_data_i = {{user_k_data[55:0],4'h0,user_k_blk_no[3:0]}*n^[1]}. - If "Little Endian Support" option not checked: user_tx_k_data_i = {{4'h0,user_k_blk_no[0:3],user_k_data[55:0]}*n^[1]}.
user_rx_k_valid_o ^{[3][6]}	output	1	Indicator for receiving user K-character valid, active-high; when user_rx_k_valid_o is high, the data on the bus is valid.
CRC Status Interface			
crc_pass_fail_n_o ^[7]	output	1	CRC check status; when crc_valid_o is high and crc_pass_fail_n_o is low, it indicates a current CRC error. When crc_valid_o and crc_pass_fail_n_o are high, it indicates a current successful CRC.
crc_valid_o ^[7]	output	1	CRC check status valid indicator, active-high.
Status Interface			
hard_err_o ^[8]	output	1	Hard error indicator; high indicates that a hard error has occurred in the link, and it sets to 1'b0 until the IP is reset.
soft_err_o ^[8]	output	1	Soft error indicator; high indicates that the current RX link has a soft error.
channel_up_o ^[8]	output	1	Channel linking status indicator; active-high; high indicates successful linking of the channel.
lane_up_o ^[9]	output	[(n ^[1] -1):0]	Lane linking status indicator, active-high; high indicates successful linking of the corresponding lane.
tx_hard_err_o ^[9]	output	1	TX hard error indicator; high indicates that a hard error has occurred in the link. It sets to 1'b0 until the IP is reset.
tx_soft_err_o ^[9]	output	1	TX soft error indicator; high indicates that the current RX link has a soft error.
tx_channel_up_o ^[9]	output	1	TX Channel linking status indicator, active-high; high indicates successful linking of the channel.
tx_lane_up_o ^[9]	output	[(n ^[1] -1):0]	TX lane linking status indicator, active-high; high indicates successful linking of the corresponding lane.
rx_hard_err_o ^[10]	output	1	RX Hard error indicator; high indicates that a hard

Port Name	I/O	Data Width	Description
			error has occurred in the link. It sets to 1'b0 until the IP is reset.
rx_soft_err_o ^[10]	output	1	RX soft error indicator; high indicates that the current RX link has a soft error.
rx_channel_up_o ^[10]	output	1	RX Channel linking status indicator, active-high; high indicates successful linking of the channel.
rx_lane_up_o ^[10]	output	[(n ^[1] -1):0]	RX lane linking status indicator, active-high; high indicates successful linking of the corresponding lane.
cfg_tx_init_counter_i ^[9]	Input	[23:0]	TX initialization counter statistics. During simulation, it can be set to 24'h3ff to accelerate simulation speed. For application, set it to 24'hffff.
User-side SerDes-related Control Interface			
gt_pma_rstn_i	input	1	SerDes channel reset signal, active-low; reset all lanes for the IP at the same time.
gt_pll_ok_o	output	1	SerDes PLL lock status; High indicates clock lock.
gt_pcs_tx_clk_o	output	[(n ^[1] -1):0]	SerDes PCS layer clock in the TX, with each lane corresponding to a 1-bit clock.
gt_pcs_tx_rst_i ^[2]	input	1	SerDes PCS layer TX reset, active-high; reset all lanes for the IP at the same time.
gt_tx_fifo_wrusewd_o ^[2]	output	[(5n ^[1] -1):0]	The difference in pointers between the read and write of the SerDes channel TX FIFO, with each lane corresponding to 5 bits of valid data.
gt_pcs_rx_rst_i ^[3]	input	1	SerDes PCS layer RX reset, active-high; reset all lanes for the IP at the same time.
gt_rx_align_link_o ^[3]	output	[(n ^[1] -1):0]	Alignment status of the SerDes channel, where high indicates normal link alignment, with each lane corresponding to 1 bit of valid data.
gt_rx_pma_lock_o ^[3]	output	[(n ^[1] -1):0]	RX PMA layer lock status of the SerDes channel, where high indicates normal link, with each lane corresponding to 1 bit of valid data.
gt_rx_fifo_rdusewd_o ^[3]	output	[(5n ^[1] -1):0]	Difference in pointers between the read and write of the SerDes channel RX FIFO, with each lane corresponding to 5 bits of valid data.
gt_pcs_rx_clk_o ^[3]	output	[(n ^[1] -1):0]	SerDes PCS layer clock in the RX, with each lane corresponding to a 1-bit clock.
gt_rx_block_sync_o ^[3]	output	[(n ^[1] -1):0]	SerDes RX block synchronization indicator; high indicates normal RX block synchronization, with each lane corresponding to 1 bit of valid data.
gt_rx_charerr_o ^[3]	output	[(n ^[1] -1):0]	SerDes RX error indicator; high indicates RX error, with each lane corresponding to 1 bit of valid data.
SerDes Hard-core Interface			
SerDes_*	—	—	The signal with the beginning of SerDes_ is the connection signal of RoraLink 64B66B IP with SerDes hardcore; users may not need to pay attention; Note! EDA tools will automatically complete the connections.

Note!

- ^[1] N in the table means the number of lanes.
- ^[2] When the GUI option "Dataflow Mode" is set to "RX-only Simplex", the IP does not have this port.
- ^[3] When the GUI option "Dataflow Mode" is set to "TX-only Simplex", the IP does not have this port.
- ^[4] When the GUI option "Flow Control" is set to "None" or "UFC", the IP does not have this port.
- ^[5] When the GUI option "Flow Control" is set to "None", "Immediate NFC" or "Completion NFC", the IP does not have this port.
- ^[6] When the GUI option "USER K" is not checked, the IP does not have this port.
- ^[7] When the GUI option "CRC" is not checked, the IP does not have this port.
- ^[8] When the GUI option "Dataflow Mode" is set to "Duplex", this port is valid for the IP.
- ^[9] When the GUI option "Dataflow Mode" is set to "TX-only Simplex" or "TX/RX Simplex", this port is valid for the IP.
- ^[10] When the GUI option "Dataflow Mode" is set to "RX-only Simplex" or "TX/RX Simplex", this port is valid for the IP.

3.6 User Interface Timing

3.6.1 User Data TX Interface Timing Diagram

Gowin RoraLink 64B66B IP provides a user data transmission interface for transmitting frame data or stream data.

For the frame data interface, the data blocks are separated by Separator Blocks, serving as the end of each data block. Data transmission occurs in blocks of 64 bits, and the data blocks in the TX are input by the user through the data transmission interface. Separator Blocks and Idle Blocks are inserted by the IP core. The frame data structure is illustrated in Figure 3-4, showing data transmission on a single Lane. When the last set of valid data in a data frame has a length of 1 to 6 bytes, the end of each frame data consists of 1 byte of SEP (0x1e), 1 byte of data count, 1 to 6 bytes of valid data, and padding data. And the data count ranges from 1 to 6, indicating the number of valid bytes in the last set of data. When the last set of valid data in a data frame is 8 bytes, the end of each frame data consists of 1 byte of SEP (0x1e), 1 byte of data count (0x0), and 6 bytes of padding data. When the last set of valid data in a data frame is 7 bytes, the end of each frame data consists of SEP-7 (0xe1) and 7 bytes of valid data.

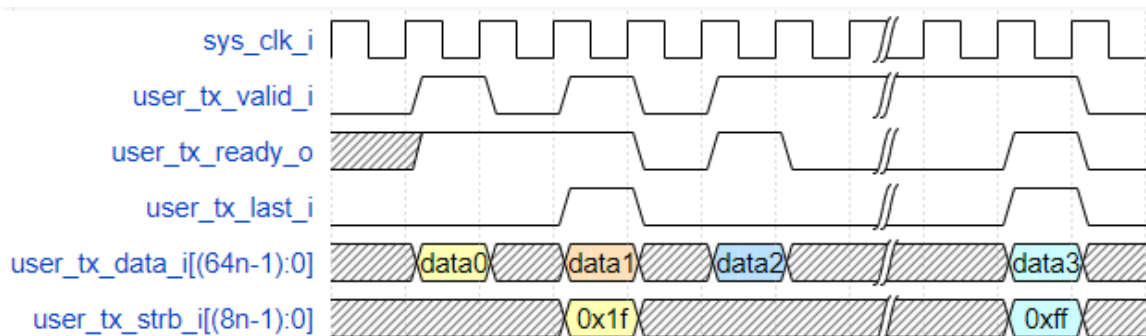
Figure 3-4 Frame Structure

Frame0 Data Byte7	Frame0 Data Byte6	Frame0 Data Byte5	Frame0 Data Byte4	Frame0 Data Byte3	Frame0 Data Byte2	Frame0 Data Byte1	Frame0 Data Byte0
SEP(0x1e)	Count(0x2)	---	---	---	---	Frame0 Data Byte9	Frame0 Data Byte8
IDLE(0x78)	CC/CB/NR/SA/---	---	---	---	---	---	---
SEP-7(0xe1)	Frame1 Data Byte6	Frame1 Data Byte5	Frame1 Data Byte4	Frame1 Data Byte3	Frame1 Data Byte2	Frame1 Data Byte1	Frame1 Data Byte0
Frame2 Data Byte8	Frame2 Data Byte7	Frame2 Data Byte6	Frame2 Data Byte5	Frame2 Data Byte4	Frame2 Data Byte3	Frame2 Data Byte1	Frame2 Data Byte0
Frame2 Data Byte16	Frame2 Data Byte15	Frame2 Data Byte14	Frame2 Data Byte13	Frame2 Data Byte12	Frame2 Data Byte11	Frame2 Data Byte10	Frame2 Data Byte9
SEP(0x1e)	Count(0x0)	---	---	---	---	---	---
IDLE(0x78)	CC/CB/NR/SA/---	---	---	---	---	---	---

Frame data TX interface timing is illustrated in Figure 3-5; user_tx_data_i is used to transmit data blocks. The data is valid when both user_tx_valid_i and user_tx_ready_o are high. The user_tx_last_i signal

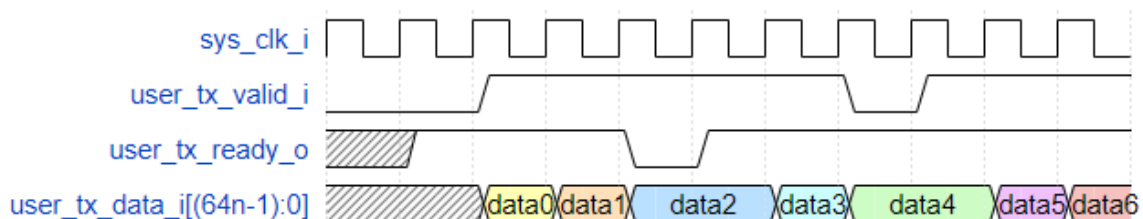
indicates the end of frame data, and `user_tx_strb_i` is only valid when `user_tx_last_i`, `user_tx_valid_i`, and `user_tx_ready_o` are all high. `user_tx_strb_i` represents the byte enable for the frame tail. Within the IP, Separator Blocks and Idle Blocks are inserted between frame data. If the CRC option is selected on the GUI, IP internally adds the CRC field to the end of the frame.

Figure 3-5 Frame Data TX Interface Timing Diagram



In the case of streaming data transmission, there is no frame delimiter, making the transmission simple and resource-efficient. The timing diagram for the data TX interface is illustrated in Figure 3-6. `user_tx_data_i` is used to transmit data blocks. Data is valid when both `user_tx_valid_i` and `user_tx_ready_o` are high.

Figure 3-6 Stream Data TX Interface Timing Diagram

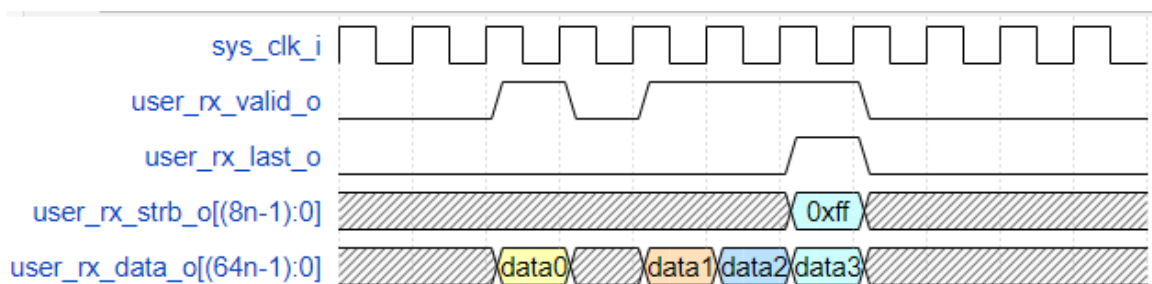


3.6.2 User Data RX Interface Timing Diagram

Gowin RoraLink 64B66B IP provides a user data RX interface for transmitting frame data or stream data. After receiving data, the IP processes control characters in the data and transmits the remaining data blocks to the user through the receive interface.

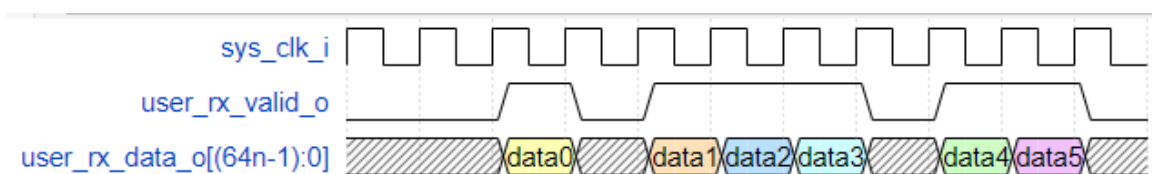
The timing diagram for the frame data RX interface is shown in Figure 3-7. `user_rx_data_o` is used to transmit data blocks. Data is valid when `user_rx_valid_o` is high. `user_rx_last_o` indicates the end of the frame data. `user_rx_strb_o` is valid only when both `user_rx_last_o` and `user_rx_valid_o` are high, and it represents the byte enable for the frame tail.

Figure 3-7 Frame Data RX Interface Timing Diagram



The timing diagram for the stream data RX interface is as shown in Figure 3-8. `user_rx_data_o` is used to transmit data blocks. Data is valid when `user_rx_valid_o` is high.

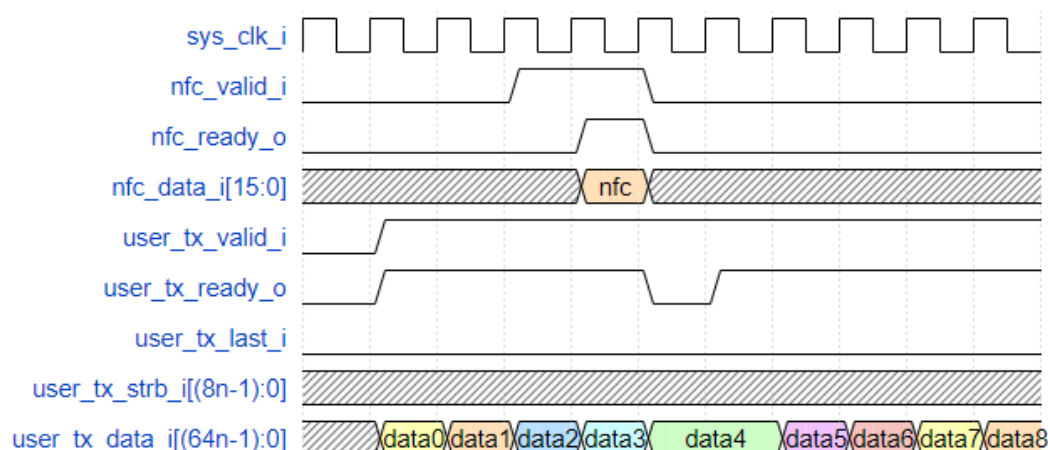
Figure 3-8 Stream Data RX Interface Timing Diagram



3.6.3 NFC Interface Timing Diagram

The NFC mode flow control interface provided by Gowin RoraLink 64B66B IP is used for sending NFC request messages from the local device to the remote end. NFC operates in two modes: immediate mode and completion mode. In immediate mode, the device must promptly process the NFC request it receives. In completion mode, the device must finish the previous frame data transmission before processing the NFC request.

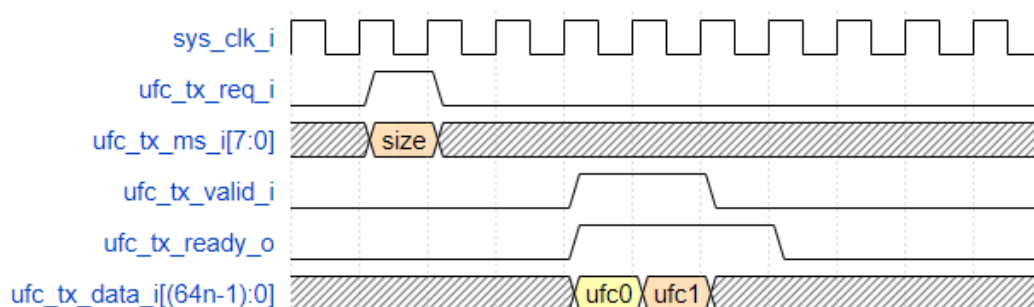
For NFC messages in big-endian mode, `nfc_data_i[0:6]` represents reserved fields. `nfc_data_i[7]` indicates the xoff mode indicator signal. `nfc_data_i[8:15]` represents the pause value. For NFC messages in little-endian mode, `nfc_data_i[15:9]` represents reserved fields. `nfc_data_i[8]` indicates the xoff mode indicator signal. `nfc_data_i[7:0]` represents the pause value. The pause value indicates the minimum number of cycles the device should pause to transmit data after receiving an NFC request message. For example, in big-endian mode, the number of cycles to pause to transmit data is equal to `nfc_data_i[8:15] + 1`. When the xoff mode indicator signal is high, it indicates that the device is currently in xoff mode, and the device should pause to transmit data until it receives a UFC request data with a low xoff mode indicator signal or until the IP is reset. If both the pause value and the xoff mode indicator signal are 0, it indicates that the device is currently in xon mode, and the device should immediately stop the NFC countdown counter upon receiving an xon mode message, resuming normal data transmission. The timing diagram for NFC interface is as shown in Figure 3-9. `user_rx_data_o` is used to transmit data blocks.

Figure 3-9 NFC Interface Timing Diagram

3.6.4 UFC Interface Timing Diagram

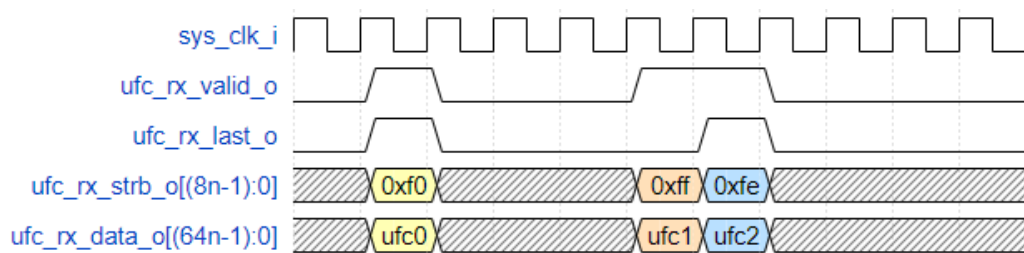
Gowin RoraLink 64B66B IP provides a UFC mode flow control interface, which includes TX and RX. UFC messages use a dedicated in-band channel to send control messages without waiting for the current data frame to finish transmission, and the maximum length of UFC messages is 256 bytes.

The timing diagram for the UFC TX interface is shown in Figure 3-10. The `ufc_tx_req_i` signal is pulled up to a high level for one clock cycle to initiate the UFC flow control transmission request. The `ufc_tx_ms_i` indicates the number of bytes in the UFC message and is valid when `ufc_tx_req_i` is high. For example, if `ufc_tx_ms_i` is 0xF, it means that the length of the UFC message to be transmitted is 16 bytes. The `ufc_tx_data_i` represents the UFC message to be transmitted, and the UFC message is valid when both `ufc_tx_ready_o` and `ufc_tx_valid_i` are high, under normal circumstances, the transmission of the UFC message is delayed by 2 clock cycles after the `ufc_tx_req_i` signal is asserted.

Figure 3-10 UFC TX Interface Timing Diagram

The timing diagram for the UFC RX interface is shown in Figure 3-11. When `ufc_rx_valid_o` is high, the `ufc_rx_data_o` data is valid. `ufc_rx_strb_o` corresponds to the byte enable of the data in `ufc_rx_data_o`, and `ufc_rx_last_o` being high indicates the end of the UFC data frame.

Figure 3-11 UFC RX Interface Timing Diagram



3.6.5 User K-character Interface Timing Diagram

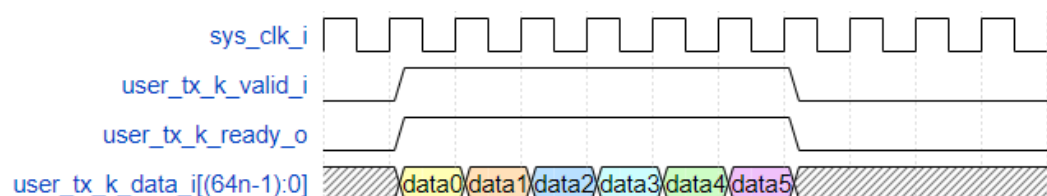
In Gowin RoraLink 64B66B IP, the User K-character interface is provided for both the TX and RX directions. The K-character is transmitted in 64-bit data blocks, consisting of 4-bit user_k_blk_no and 56-bit user_k_data. As shown in Table 3-2, the 4-bit user_k_blk_no ranges from 0 to 9, corresponding to 10 block types (Block Type Field, BTF). The user_k_data field is user-defined data.

Table 3-2 Correspondence between user_k_blk_no and BTF

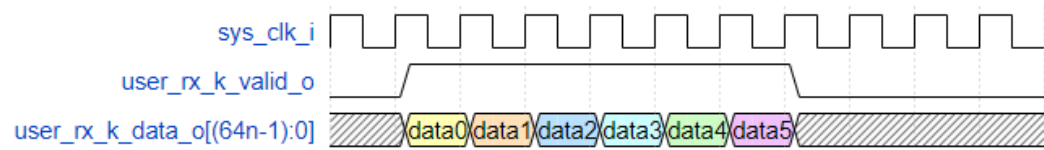
user_k_blk_no	Block Type Field(BTF)
USER-K Block 0	0xd2
USER-K Block 1	0x99
USER-K Block 2	0x55
USER-K Block 3	0xb4
USER-K Block 4	0xcc
USER-K Block 5	0x66
USER-K Block 6	0x33
USER-K Block 7	0x4b
USER-K Block 8	0x87

If the IP is configured in big-endian mode, user_tx_k_data_i [0:3] is filled with zeros; user_tx_k_data_i [4:7] represents user_k_blk_no; user_tx_k_data_i [8:63] represents user-defined data. If the IP is configured in little-endian mode, user_tx_k_data_i [63:8] represents user-defined data; user_tx_k_data_i [7:4] is filled with zeros; user_tx_k_data_i [3:0] represents user_k_blk_no. The timing diagram for the user K-character TX interface is illustrated in Figure 3-12.

Figure 3-12 User K-character TX Interface Timing Diagram

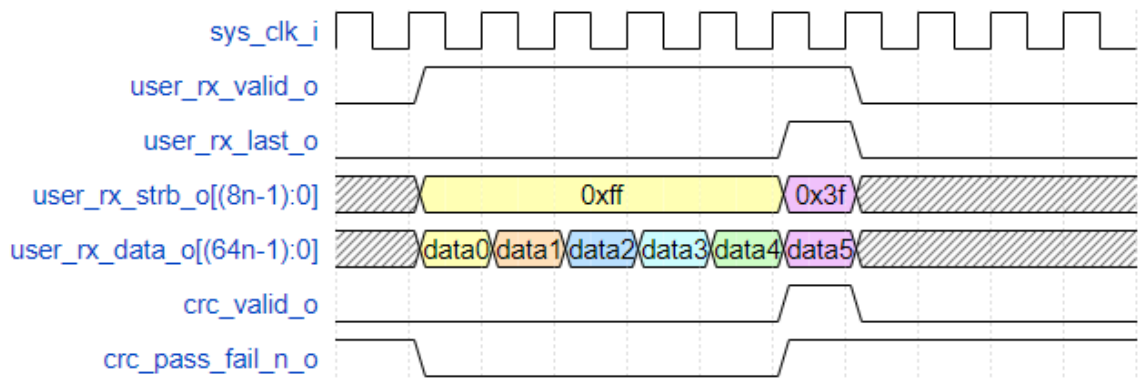


The timing diagram for the user K-character RX interface is illustrated in Figure 3-13.

Figure 3-13 User K-character RX Interface Timing Diagram

3.6.6 CRC Interface Timing Diagram

Gowin RoraLink 64B66B IP provides a CRC interface that indicates CRC check results. As shown in Figure 3-14, in the CRC check timing diagram, `crc_valid_o` is asserted high for one clock cycle at the end of the data frame. When `crc_valid_o` is high, the `crc_pass_fail_n_o` signal is valid. A high level on `crc_pass_fail_n_o` indicates a successful CRC check, while a low level indicates a CRC check error.

Figure 3-14 CRC Interface Timing

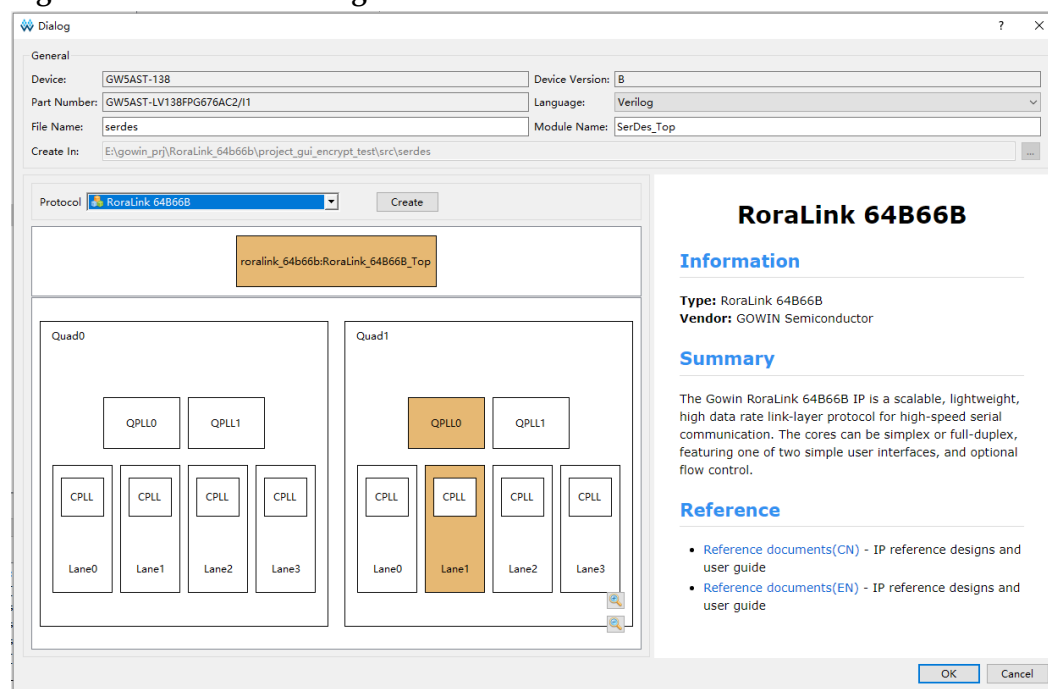
4 Interface Configuration

You can call and configure Gowin RoraLink 64B66B IP using the IP core generator tool in the IDE.

1. Open SerDes IP

After creating the project, click the "Tools" tab in the upper left interface, click "IP Core Generator" from the drop-down list to open Gowin IP Core Generator. Then find SerDes under the Soft IP Core directory, and double-click to open SerDes IP.

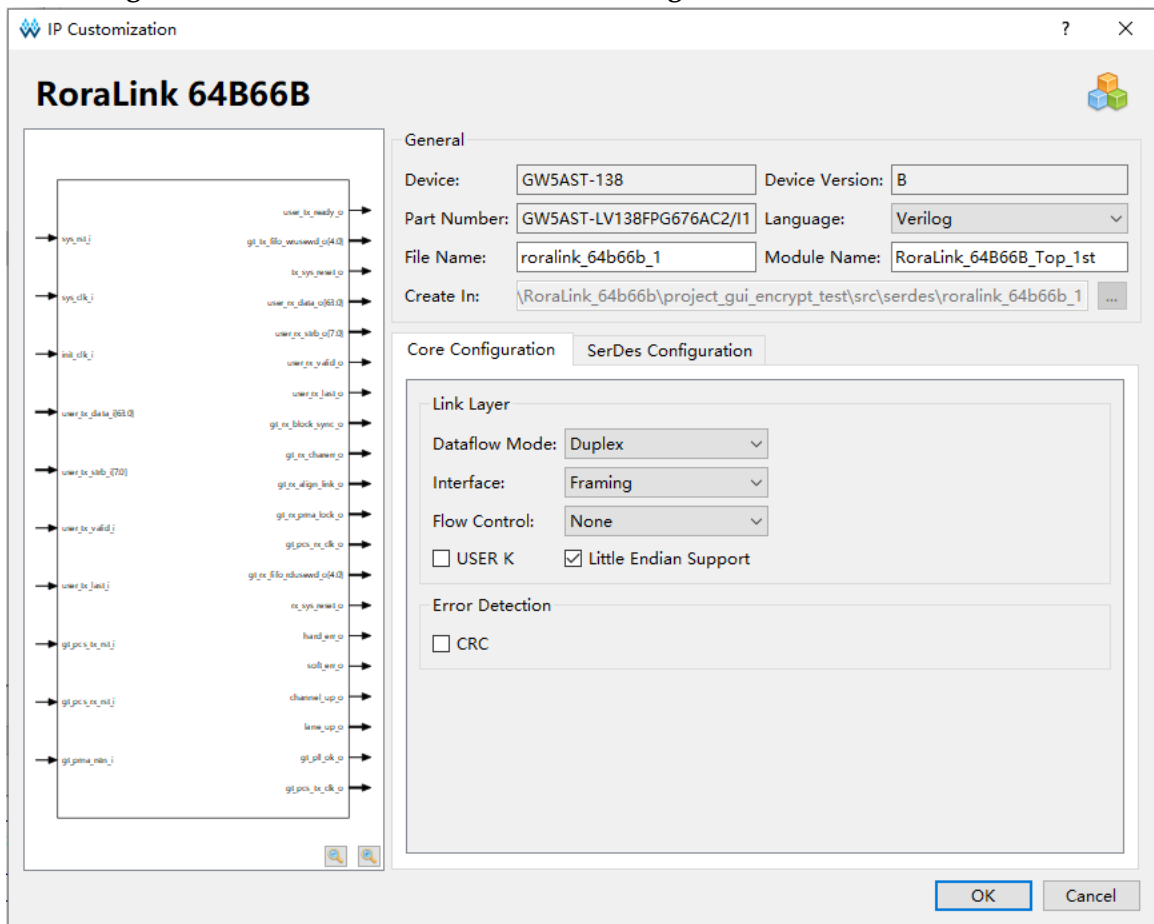
Figure 4-1 SerDes IP Configuration Interface



2. Open RoraLink 64B66B IP core

After opening SerDes IP, find "RoraLink 64B66B" in the "Protocol" drop-down list and click "Create" to open the RoraLink 64B66B IP protocol configuration interface.

Figure 4-2 Gowin RoraLink 64B66B IP Configuration Interface



3. Configure RoraLink 64B66B IP protocol

The RoraLink 64B66B IP configuration interface includes "Core Configuration", "SerDes Configuration", and "AFE", as shown in Figure 4-3, Figure 4-4, and Figure 4-5. Users can configure link-layer-related parameters on the "Core Configuration" page and SerDes-related parameters on the "SerDes Configuration" page. Users can select the SerDes analog parameters on the "AFE" page. The descriptions of parameters are shown in

Table 4-1. After configuring the RoraLink 64B66B IP parameters, click the "OK" button to generate the configuration for the RoraLink 64B66B IP protocol.

4. Complete SerDes IP configuration

On the SerDes IP interface, the user completes the configuration of all protocols and then clicks the "OK" button to generate the SerDes IP. In the SerDes IP top-level file, the signal with RoraLink_64B66B_Top_ prefix is the signal associated with RoraLink 64B66B IP.

Figure 4-3 IP Protocol Configuration

The image shows a configuration window titled "IP Protocol Configuration". It has two tabs: "Core Configuration" (selected) and "SerDes Configuration". The "Core Configuration" tab contains two sections: "Link Layer" and "Error Detection".

Link Layer

- Dataflow Mode: Duplex (dropdown menu)
- Interface: Framing (dropdown menu)
- Flow Control: None (dropdown menu)
- ☐ USER K
- ☒ Little Endian Support

Error Detection

- ☐ CRC

Figure 4-4 SerDes Configuration

Core Configuration

SerDes Configuration

Lane Width: 1

Channel Selection

Channel0 Selection: Q0 Lane0

Channel1 Selection: Q0 Lane1

Channel2 Selection: Q0 Lane2

Channel3 Selection: Q0 Lane3

Channel4 Selection: Q1 Lane0

Channel5 Selection: Q1 Lane1

Channel6 Selection: Q1 Lane2

Channel7 Selection: Q1 Lane3

Loopback Mode: OFF

Line Rate: 3.1250 [0.85-10.3125](Gbps)

Refclk Selection

Reference Clock Source: Q0 REFCLK0

Reference Clock Frequency: 125.000 MHz

PLL Selection: CPLL

Calculate

Figure 4-5 AFE Configuration

The screenshot shows the 'AFE' configuration window. It is divided into two columns: TX and RX. The TX column has a 'Differential Swing' dropdown set to 900mV, an 'FFE Mode' dropdown set to Auto, and three input fields for Cm (0), C0 (40), and C1 (0). The RX column has an 'SD Threshold' dropdown set to 100mV, an 'Equalization' dropdown set to Auto, and three input fields for ATT (7), BOOST (9), and BIAS (7). The window has 'OK' and 'Cancel' buttons at the bottom right.

Table 4-1 Gowin RoraLink 64B66B IP Parameters

Name	Range	Default	Description
Core Configuration			
Dataflow Mode	Duplex, RX-only Simplex, TX-only Simplex, TX/RX Simplex	Duplex	Select duplex mode or simplex mode
Interface	Framing, Streaming	Framing	Select frame data or stream data.
Flow Control	None, UFC, Immediate NFC, Completion NFC, UFC+Immediate NFC, UFC+Completion NFC	None	Select the flow control mode
USER K	Check/Uncheck	Uncheck	Whether to enable the User K-character interface. If selected, it means the User K-character interface is enabled; if not selected, it means the User K-character interface is disabled.
Little Endian Support	Check/Uncheck	Check	The interface is in little-endian mode or big-endian mode. If checked, it is in little-endian mode; if unchecked, it is in big-endian mode.
CRC	Check/Uncheck	Unchecked	Whether the IP performs CRC processing. CRC is added in the user data transmission direction and removed with

Name	Range	Default	Description
			CRC check in the user data reception direction. If checked, CRC is enabled; if unchecked, CRC is disabled.
PHY Configuration			
Lane Width	1,2,3,4,5,6,7,8	1	Select the number of lanes for the IP
Channel0 Selection	Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2, Q1 Lane3,	Q0 Lane0	Selection of the SerDes channel for the first Lane of the IP. Q0 and Q1 correspond to two Quads of SerDes Lane0, Lane1, Lane2, and Lane3 indicate the 4 Lane numbers for each Quad of SerDes. Note! The number of lanes available on the GUI is associated with the option "Lane Width".
Channel1 Selection	Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2, Q1 Lane3,	Q0 Lane1	Selection of the SerDes channel for the second Lane of the IP. Q0 and Q1 correspond to two Quads of SerDes. Lane0, Lane1, Lane2, and Lane3 indicate the 4 Lane numbers for each Quad of SerDes.
Channel2 Selection	Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2, Q1 Lane3,	Q0 Lane2	Selection of the SerDes channel for the third Lane of the IP. Q0 and Q1 correspond to two Quads of SerDes. Lane0, Lane1, Lane2, and Lane3 indicate the 4 Lane numbers for each Quad of SerDes.
Channel3 Selection	Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2, Q1 Lane3,	Q0 Lane3	Selection of the SerDes channel for the fourth Lane of the IP. Q0 and Q1 correspond to two Quads of SerDes. Lane0, Lane1, Lane2, and Lane3 indicate the 4 Lane numbers for each Quad of SerDes.
Channel4 Selection	Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2, Q1 Lane3,	Q1 Lane0	Selection of the SerDes channel for the fifth Lane of the IP. Q0 and Q1 correspond to two Quads of SerDes. Lane0, Lane1, Lane2, and Lane3 indicate the 4 Lane numbers for each Quad of SerDes.
Channel5 Selection	Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2, Q1 Lane3,	Q1 Lane1	Selection of the SerDes channel for the sixth Lane of the IP. Q0 and Q1 correspond to two Quads of SerDes. Lane0, Lane1, Lane2, and Lane3 indicate the 4 Lane numbers for each Quad of SerDes.
Channel6 Selection	Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2, Q1 Lane3,	Q1 Lane2	Selection of the SerDes channel for the seventh Lane of the IP. Q0 and Q1 correspond to two Quads of SerDes. Lane0, Lane1, Lane2, and Lane3 indicate the 4 Lane numbers for each Quad of SerDes.
Channel7 Selection	Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2, Q1 Lane3,	Q1 Lane3	Selection of the SerDes channel for the eighth Lane of the IP. Q0 and Q1 correspond to two Quads of SerDes. Lane0, Lane1, Lane2, and Lane3 indicate the 4 Lane numbers for each Quad of SerDes.

Name	Range	Default	Description
Loopback Mode	OFF, LB_NES, LB_FES, LB_ENC	OFF	SerDes Loopback Selection: ● OFF indicates Normal mode; SerDes data is transmitted and received normally. ● LB_NES (Loopback Near-End SerDes), SerDes internal loopback; data is looped back to from the near-end PMA to the near-end PMA. ● LB_ENC (Loopback Near-End PCS), SerDes internal loopback; data is looped back to the near-end PCS to the near-end PCS. ● LB_FES, SerDes external loopback; data is looped back to TX from RX of SerDes.
Line Rate	0.85~10.3125Gbps (QPLL0/CPLL), 0.95~10.3125G (QPLL1)	3.1250Gbps	User inputs the required SerDes line rate. When PLL is selected as QPLL0 or CPLL, the theoretical operating line rate range of SerDes is 0.85G~12.5G. When PLL is selected as QPLL1, the theoretical operating line rate range of SerDes is 0.95G~12.5G. However, the final achievable performance depends on the project timing. If CRC is selected, or if a larger number of lanes are chosen (larger data width), the maximum achievable speed may be reduced due to timing violation issues.
Reference Clock Source	● For devices GW5AST-138/GW5AT-138/GW5AT-75 Q0 REFCLK0, Q0 REFCLK1, Q1 REFCLK 0, Q1 REFCLK 1 ● For devices GW5AT-60 Q0 REFCLK0, Q0 REFCLK1, Q0 REFCLK2, Q0 REFCLK3, SERDES Q0CLKIN0, SERDES Q0CLKIN1, SERDES Q0CLKIN2, SERDES Q0CLKIN3	Q0 REFCLK0	● For devices GW5AST-138/GW5AT-138/GW5AT-75: The reference clock selection for high-speed transceivers is as follows: Q0/Q1 corresponds to the two Quads of SerDes. REFCLK0 and REFCLK1 correspond to the two input reference clocks for each SerDes Quad. Users can select the input reference clock according to their application needs. ● For devices GW5AT-60: The reference clock selection for high-speed transceivers is as follows: Q0REFCLK0, Q0REFCLK1, Q0REFCLK2, and Q0REFCLK3 correspond to the four input reference clocks for Quad0. SERDES Q0CLKIN0, SERDES Q0CLKIN1, SERDES Q0CLKIN2, and SERDES Q0CLKIN3 correspond to the input reference clocks for dedicated GPIO pins. The selectable input reference clocks vary depending on the chip package.
Reference Clock Frequency	User input	125M	The reference clock frequency for high-speed transceivers. The GUI interface

Name	Range	Default	Description
			will automatically calculate a set of recommended reference clock frequencies based on the input Line Rate in the dropdown list. Users can either customize the frequency or choose one of the frequencies generated by the GUI. Clicking the "Calculate" button allows users to confirm the correctness of the frequency.
PLL Selection	QPLL0, QPLL1, CPLL	CPLL	PLL selection
AFE			
Differential Swing	100mV~900mV	900mV	Configure TX differential signal swing Vdiffpp, Vdiffpp=2xVdiff
FFE Mode	Auto, Manual	Auto	Configure TX FFE mode Auto: Auto mode Manual: Manual mode
Cm	0~19	0	Transmit FFE pre-cursor
C0	21~40	40	Transmit FFE main-cursor
C1	0~19	0	Transmit FFE post-cursor
SD Threshold	25mV~200mV	100mV	Receive differential signal SD threshold
Equalization Mode	Auto, Manual	Auto	Configure RX equalization mode ● Auto: Auto mode ● Manual: Manual mode
ATT	0~10	7	Adjust RX intermediate-frequency attenuation, with smaller values indicating greater attenuation.
BOOST	0~15	9	Adjust RX high-frequency amplification, with larger values indicating larger gain.
BIAS	0~15	7	Configure SerDes amplification parameters for the RX signal. The higher the configuration, the stronger the amplification of the signal.

5 Reference Design

Please see the RoraLink 64B66B [reference design](#) for details at Gowinsemi website.

5.1 Applications

The data transmission of RoraLink 64B66B IP can be composed of a single Lane or multiple Lanes, with each Lane corresponding to a SerDes channel. Data transmission can be either duplex or simplex. As shown in Figure 5-1, it illustrates simplex data transmission with a single Lane. As shown in Figure 5-2, it illustrates simplex data transmission with multiple Lanes. As shown in Figure 5-3, it illustrates duplex data transmission with a single Lane. As shown in Figure 5-4, it illustrates duplex data transmission with multiple Lanes.

Figure 5-1 Simplex Data Transmission with a Single Lane

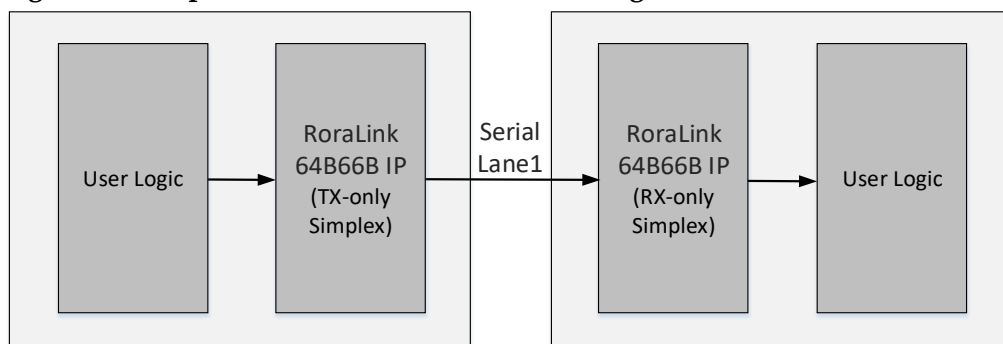


Figure 5-2 Simplex Data Transmission with Multiple Lanes

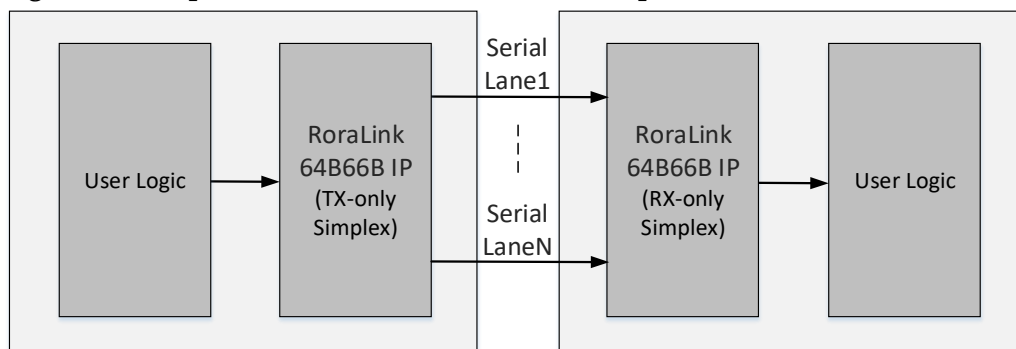
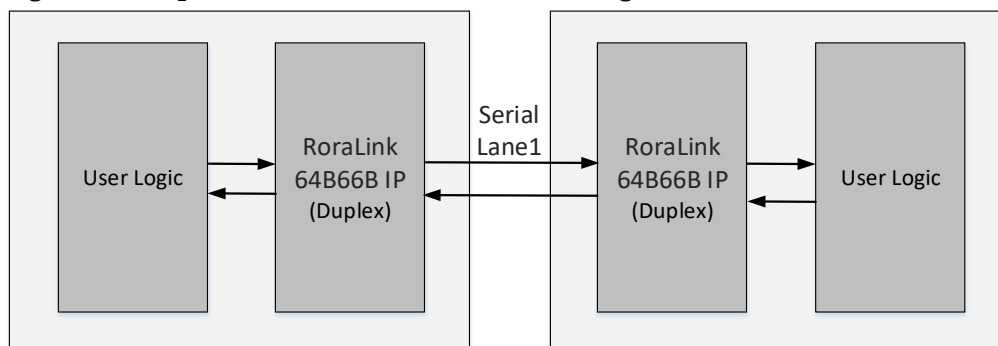
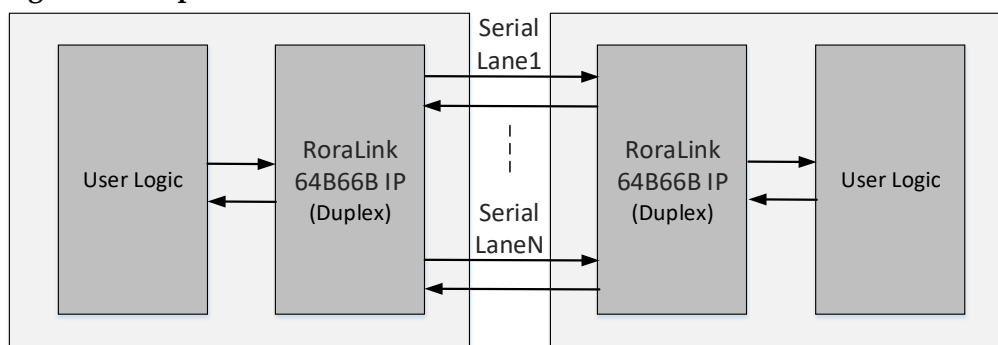


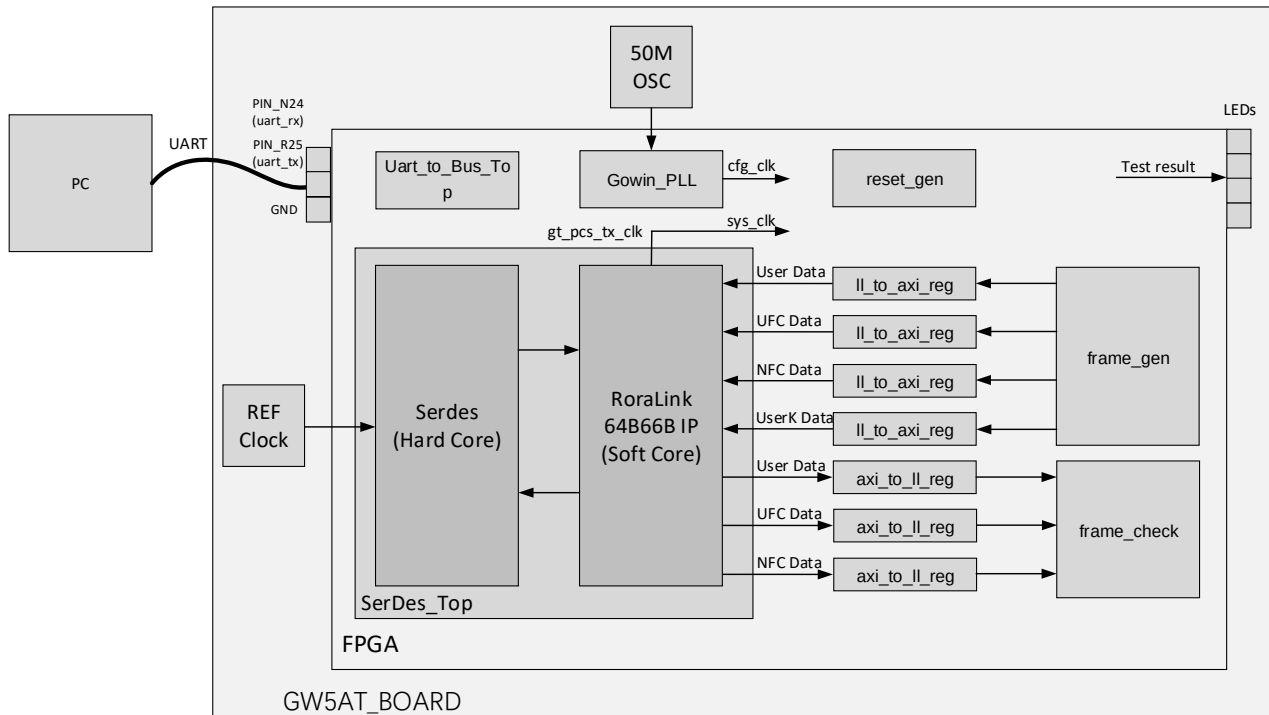
Figure 5-3 Duplex Data Transmission with a Single Lane**Figure 5-4 Duplex Data Transmission with Multi Lanes**

5.2 Gowin RoraLink 64B66B IP Reference Design Project

Gowin RoraLink 64B66B IP reference design contains the SerDes IP module (with the RoraLink 64B66B IP softcore), clock and reset, interface conversion module, frame generation module, frame detection module and debug module.

- `uart_to_bus_top`: Converts UART serial port to internal configuration bus interface in FPGA, easy to read/write registers, and easy to debug single board.
- `gowin_pll`: The on-board internal 50MHz crystal oscillator locks out the operating clock for the configuration module.
- `reset_gen`: Generates the system reset signal.
- `frame_gen`: Frame generation module.
- `frame_gen`: Frame detection module.
- `ll_to_axi_reg`: AXI interface conversion module.
- `axi_to_ll_reg`: AXI interface conversion module.
- `Serdes_Top`: Contains SerDes hard core and RoraLink 64B66B IP soft core; Gowin EDA tool will automatically complete the connection between SerDes hard core and RoraLink 64B66B IP; user only needs to pay attention to the interface of SerDes top layer after package.

Figure 5-5 Reference Design Instance Structure Diagram



5.3 Reference Design Board Test

Gowin currently offers a reference design for SerDes internal loopback testing of single RoraLink 64B66B IP, allowing users to quickly become familiar with the interface, timing, and function of RoraLink 64B66B IP without relying on a daughter card.

The steps for reference project board test are as follows:

- Download the project from the website and compile to generate fs file.
- The structure is as shown in Figure 5-5.
- Download fs to single board.
- To confirm the test results, there are two methods:

Method 1: Observe the LEDs

- LED0 (PIN_P20): Constantly ON indicates that Gowin_PLL is in a locked state.
- LED1 (PIN_R20): Constantly ON indicates that the internal PLL of SerDes is in a locked state.
- LED2 (PIN_N21): Constantly ON indicates that the IP Channel linking is established successfully.
- LED3 (PIN_N22): Constantly ON indicates that the data received by the IP has passed the verification.

Method 2: Read the register through the serial tool

PC can access the register addresses of the reference design through a serial port tool. When the environment is built, input "R 0" in the serial port tool and the register value is displayed as shown in Figure 5-6. If you

input "W 0 value", the register value corresponding to this value will be written to the register, and if you input "R 0" to reread the register, and the read register value should match the previously written value.

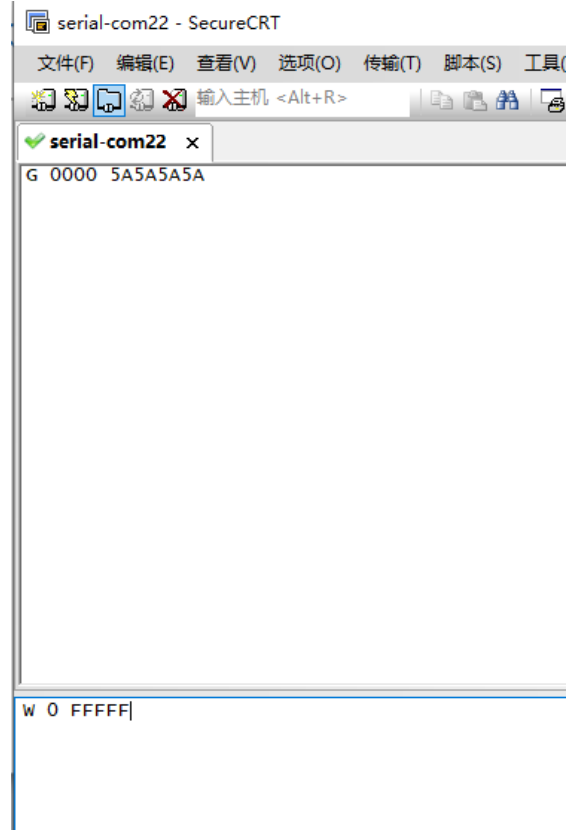
Table 5-1 Reference Design Register List

Address (Word)	Type	Data Width	Signal Name	Description
0x0	RW	[31:0]	test_reg	Test registers, and it can be written and read back, confirming the register read and write function.
0x1	RW	[31:4]	--	Reserved fields
	RW	[3]	reg_rst	IP system reset, active-high
	RW	[2]	gt_pcs_rx_rst	SerDes PCS reset in the RX, active-high
	RW	[1]	gt_pcs_tx_rst	SerDes PCS reset in the TX, active-high
	RW	[0]	gt_pma_rstn	SerDes PMA reset, active-high
0x2~0xf	RW	[31:0]	--	Reserved fields
0x10	RO	[31:5]	--	Reserved fields
	RO	[4]	lane_up	IP Lane linking status; high indicates successful link establishment
	RO	[3]	hard_err	IP Hard Error status; high indicates errors occur
	RO	[2]	channel_up	IP Channel linking status; high indicates successful link establishment
	RO	[1]	soft_err	IP Soft Error status; high indicates errors occur
	RO	[0]	gt_pll_ok	SerDes PLL lock status
0x11	RO	[31:9]	--	Reserved fields
	RO	8	gt_rx_align_link	SerDes receive alignment status; high indicates normal operation
	RO	[7:1]	--	Reserved fields
	RO	[0]	gt_rx_pma_lock	SerDes receive PMA lock status, high level indicates normal operation
0x12	RO	[31:24]	user_k_err_count	Receive USER-K message error statistics
	RO	[23:16]	ufc_err_count	Receive UFC message error statistics
	RO	[15:8]	crc_err_count	Receive CRC check error statistics
	RO	[7:0]	data_err_count	Receive data check error statistics
0x13	RO	[31:24]	soft_err_cnt	IP soft error statistics
	RO	[23:16]	hard_err_cnt	IP hard error statistics
	RO	[15:8]	channel_resync_cnt	IP channel re-linking statistics
	RO	[7:0]	lane_resync_cnt	IP lane re-linking statistics
0x15	RO	[31:17]	--	Reserved fields
	RO	[16]	gt_rx_block_sync	IP RX block synchronization status
	RO	[15:8]	gt_block_resync_cnt	IP RX block resynchronization statistics
	RO	[7:0]	gt_err_cnt	SerDes error statistics

Note!

Register read/write definition:

- RO indicates read-only
- RW indicates read-write

Figure 5-6 Serial Port Tool

6 File Delivery

The delivery file for Gowin RoraLink 64B66B IP includes documentation, design source code, and reference design.

6.1 Documentation

The folder mainly contains the user guide in PDF version.

Table 6-1 Document List

Name	Description
IPUG1085, Gowin RoraLink 64B66B IP User Guide	Gowin RoraLink 64B66B IP User Guide, namely this one

6.2 Design Source Code (Encryption)

The encrypted code file contains Gowin RoraLink 64B66B IP RTL encrypted code which is used for GUI in order to cooperate with Gowin software to generate the IP core required by users.

Table 6-2 Design Source Code List of Gowin RoraLink 64B66B IP

Name	Description
roralink_64b66b.v	The top-level file of the IP core, which provides users with interface information, encrypted.

6.3 Reference Design

The Ref. Design folder contains the netlist file, the user reference design, the constraints file, the top file, and the project folder, etc.

Table 6-3 Gowin RoraLink 64B66B IP RefDesign Folder Content List

Name	Description
top.v	The top module of reference design
top.cst	Project physical constraints file
top.sdc	Project timing constraints file
top.gsc	Project synthesis constraints file
top.gao	Project debugging file
reset_gen.v	Reset generation module
local2reg.v	Bus to Register module

Name	Description
apb2local.v	Configure the Bus to Register module
ll_to_axi_reg.v	AXI bus conversion module
axi_to_ll_reg.v	AXI bus conversion module
axi_register_slice.v	AXI bus conversion module
frame_gen.v	Data generation module
frame_check.v	Data check module
SerDes	SerDes IP folder, including SerDes related files and roralink_64b66b folder generated by EDA tool
uart_to_bus	Generated UART to Bus IP files, used to convert UART to internal configuration bus
gowin_pll	PLL IP folder, using an external input 50MHz clock as the reference clock, locking out the internal configuration clock

