



Gowin EDP RX Desteer IP User Guide

IPUG1083-2.2E, 06/26/2026

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Revision History

Date	Version	Description
02/23/2024	1.0E	Initial version published.
03/29/2024	1.1E	Descriptions of "Double Pixels Per Lane" parameter added.
06/07/2024	2.0E	● Synchronization Type parameter added. ● O_vcnt_strmclk and O_hcnt_strmclk debug ports added.
09/12/2025	2.1E	● "Frame Synchronization Without Line Complete" removed from "Synchronization Type" option. ● 1:80 clock ratio added. ● "Bits Per Pixel Coefficient" option added with selectable values of 1 and 2.
06/26/2026	2.2E	● Added 18 and 30 as selectable values for the "Bits Per Pixel" option. The available values are 18/24/30. ● Added 4 as a selectable value for the "BPP Coefficient"06/26 option. The available values are 1/2/4.

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1 About This Guide

1.1 Purpose

The purpose of Gowin EDP RX Desteer IP is to help you learn the features and usage of Gowin EDP RX Desteer IP by providing the descriptions of features, functions, ports, timing, GUI and reference design, etc. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.12.03 (64-bit). As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at www.gowinsemi.com:

- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1111, GW5AT series of FPGA Products \(Automotive\) Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1113, GW5A series of FPGA Products \(Automotive\) Data Sheet](#)
- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1118, GW5ART series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
DE	Data Enable
Desteer	De-steer

Terminology and Abbreviations	Meaning
DP	DisplayPort
EDP	Embedded DisplayPort
FPGA	Field Programmable Gate Array
HS	Horizontal Sync
IP	Intellectual Property
MSA	Main Stream Attribute
RGB	R(Red) G(Green) B(Blue)
SerDes	Serializer/Deserializer
VESA	Video Electronics Standards Association
VS	Vertical Sync

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Overview

DisplayPort (DP) is a digital video interface standard developed by the PC and chip manufacturing industry in collaboration with the Video Electronics Standards Association (VESA). This interface is free from certification and licensing fees. It is primarily used for connecting video sources to display devices and supports carrying audio, USB, and other forms of data.

The Embedded DisplayPort (eDP) protocol is an extension of the DP protocol specifically designed for embedded systems. eDP is fully compatible with the DP protocol. It is frequently utilized as the interface for liquid crystal displays (LCDs) in tablets and laptop computers.

Gowin EDP RX Desteer IP is used to receive EDP decoded data and convert it into video data for output.

Table 2-1 Gowin EDP RX Desteer IP

Gowin EDP RX Desteer IP	
Logic Resource	Please refer to Table 2-2
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9.01(64-bit) and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features

- Supports 1/2/4 lanes
- Supports 18-bit pixel input data widths of 18, 36, and 72 bits.
- Supports 24-bit pixel input data widths of 24, 48, and 96 bits.

- Supports 30-bit pixel input data widths of 30, 60, and 120 bits.
- Supports line buffer depths of 1024, 2048, 4096, 8192, and 16384.

2.3 Resource Utilization

Gowin EDP RX Desteer IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW5AST series of FPGA as an instance, the resource utilization of EDP RX Desteer IP is as shown in Table 2-2.

Table 2-2 EDP Encode Resource Utilization

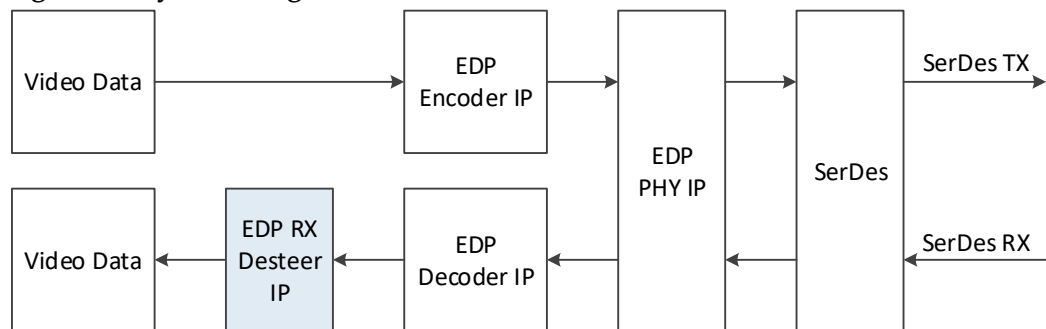
Device	Speed Grade	Name	Resource Utilization	Note
GW5AST-138	-C1/I0	LUT	1307	4 lanes, User Clock Ratio1:20, Line buffer depth 4096
		REG	591	
		BSRAM	24	

3 Functional Description

3.1 System Block Diagram

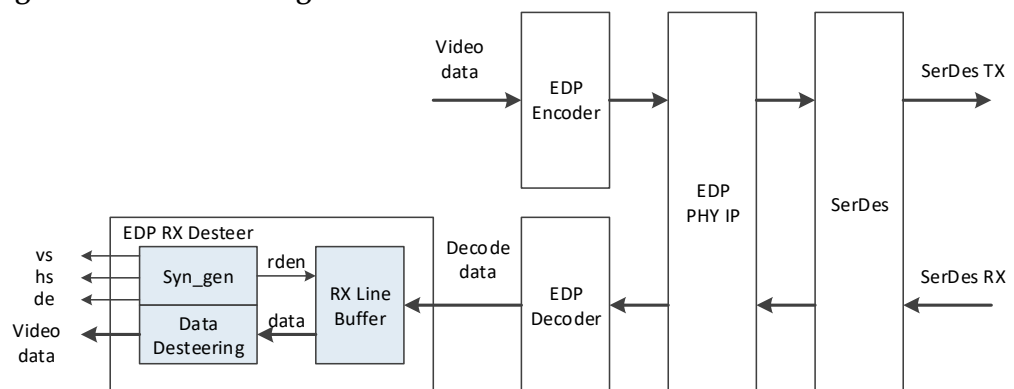
The system diagram of Gowin EDP RX Desteer IP is shown in Figure 3-1.

Figure 3-1 System Diagram



3.2 Structure Diagram

Figure 3-2 Structure Diagram



Gowin EDP RX Desteer IP primarily includes line buffer module, synchronization generation module, and data desteeing module.

3.3 Working Principle

According to the DP protocol, the main link can support 1, 2, or 4 lanes. Regardless of the color space and pixel bit depth of the video stream, pixel is steered according to Table 3-1.

Table 3-1 Pixel Steering

# of Lanes	Pixel Steering
One	All pixels to Lane 0
Two	Pixel 2N to Lane 0 Pixel 2N+1 to Lane 1
Four	Pixel 4N to Lane 0 Pixel 4N+1 to Lane 1 Pixel 4N+2 to Lane 2 Pixel 4N+3 to Lane 3

3.3.1 Line Buffer Module

The line buffer module is used to receive data output from the EDP decoding IP and buffer it using FIFOs. Each lane corresponds to an independent FIFO, and the FIFO depth can be set to 1024, 2048, 4096, 8192, 16384.

The input data width of the line buffer module varies based on the User Clock Ratio parameter. When the User Clock Ratio is 1:20, the input data width per lane is 24. When the User Clock Ratio is 1:40, the input data width per lane is 48. When the User Clock Ratio is 1:80, the input data width per lane is 96.

When Bits Per Pixel is set to 24, and the Bits Per Pixel Coefficient is set to 1, the output data width per lane is 24 bits. When the Bits Per Pixel Coefficient is set to 2, the output data width per lane is 48 bits. When the Bits Per Pixel Coefficient is set to 4, the output data width per lane is 96 bits.

When Bits Per Pixel is set to 18 or 30, the calculation method is the same as the calculation method when Bits Per Pixel is set to 24.

3.3.2 Synchronization Generation Module

The synchronization generation module generates horizontal sync (HS), vertical sync (VS), data enable (DE), and FIFO read enable signals based on the video stream parameter output from the EDP decoding IP.

3.3.3 Data Desteering Module

The data desteering module reads data from the line buffer module and outputs it according to the VESA video timing. This IP generates different pixel modes based on the number of lanes. For a main link with 1 lane, the video output data is 24 bits in single-pixel mode, meaning one pixel is transmitted per pixel clock. For a main link with 2 lanes, the video output data is 48 bits in dual-pixel mode, meaning two pixels are transmitted per pixel clock. For a main link with 4 lanes, the video output data is 96 bits in quad-pixel mode, meaning four pixels are transmitted per

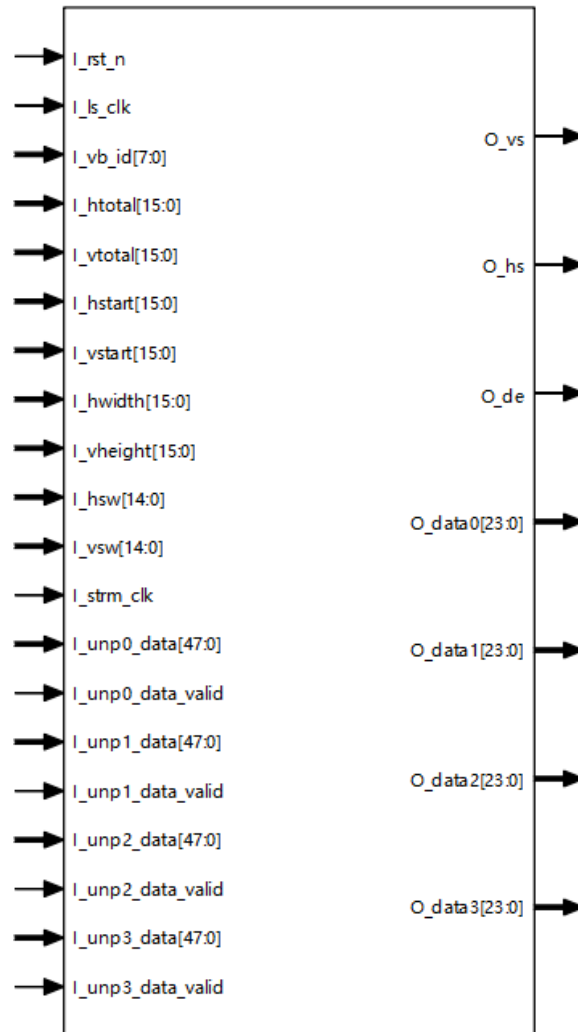
pixel clock.

When the Bits Per Pixel Coefficient is set to 2, the number of output pixels is doubled.

3.4 Port List

The I/O ports of Gowin EDP RX Desteer IP are as shown in Figure 3-3.

Figure 3-3 Gowin EDP RX Desteer IO Port Diagram



The IO ports vary slightly depending on the parameters.

The details of IO port of Gowin EDP RX Desteer IP are shown in Table 3-2.

Table 3-2 I/O List of Gowin EDP RX Desteer IP

No.	Signal Name	I/O	Description	Note
1	I_rst_n	I	Reset signal, active-low	The I/O of all the signals take EDP RX Desteer IP as a reference.
2	I_ls_clk	I	Input link clock	
3	I_vb_id	I	VB-ID parameter	
4	I_htotal	I	Parameter of horizontal total pixels in MSA	
5	I_vtotal	I	Parameter of vertical total lines in MSA	

No.	Signal Name	I/O	Description	Note
6	I_hstart	I	Parameter of horizontal active start in MSA, measured in pixel count	
7	I_vstart	I	Parameter of vertical active start in MSA, measured in line count	
8	I_hwidth	I	Parameter of horizontal active in MSA, measured in pixel count	
9	I_vheight	I	Parameter of vertical active in MSA, measured in line count	
10	I_hsw	I	Parameter of horizontal sync signal width in MSA	
11	I_vsw	I	Parameter of vertical sync signal width in MSA	
12	I_unp0_data_valid	I	Input lane0 data valid signal	
13	I_unp0_data	I	Input lane0 link data If "Bit Per Pixel" is set to 18: - When User Clock Ratio is 1:20 and the bit width is 18 bits, the format is {B,G,R}. - When User Clock Ratio is 1:40 and the bit width is 36 bits, the format is { B₁,G₁,R₁,B₀,G₀,R₀}. - When the User Clock Ratio is 1:80 and the bit width is 72 bits, the format is {B₃,G₃,R₃,B₂,G₂,R₂, B₁,G₁,R₁,B₀,G₀,R₀}. If "Bit Per Pixel" is set to 24: - When User Clock Ratio is 1:20 and the bit width is 24 bits, the format is {B,G,R}. - When User Clock Ratio is 1:40 and the bit width is 48 bits, the format is {B₁,G₁,R₁,B₀,G₀,R₀}. - When the User Clock Ratio is 1:80 and the bit width is 96 bits, the format is {B₃,G₃,R₃,B₂,G₂,R₂, B₁,G₁,R₁,B₀,G₀,R₀}. If "Bit Per Pixel" is set to 30: - When User Clock Ratio is 1:20 and the bit width is 30 bits, the format is {B,G,R}. - When User Clock Ratio is 1:40 and the bit width is 60 bits, the format is {B₁,G₁,R₁,B₀,G₀,R₀}. - When the User Clock Ratio is 1:80 and the bit width is 120 bits, the format is {B₃,G₃,R₃,B₂,G₂,R₂, B₁,G₁,R₁,B₀,G₀,R₀}.	
14	I_unp1_data_valid	I	Input lane1 data valid signal	
15	I_unp1_data	I	Input lane1 link data; Its functional definition is the same as	

No.	Signal Name	I/O	Description	Note
			I_unp0_data. For detailed information, refer to the I_unp0_data signal description.	
16	I_unp2_data_valid	TX video data enable	Input lane2 data valid signal	
17	I_unp2_data	I	Input lane2 link data; Its functional definition is the same as I_unp0_data. For detailed information, refer to the I_unp0_data signal description.	
18	I_unp3_data_valid	I	Input lane3 data valid signal	
19	I_unp3_data	I	Input lane3 link data Its functional definition is the same as I_unp0_data. For detailed information, refer to the I_unp0_data signal description.	
20	I_strm_clk	I	Input video stream clock	
21	O_vcnt_strmclk	I	Debug port, vertical count in video stream clock domain	
22	O_hcnt_strmclk	I	Debug port, horizontal count in video stream clock domain	
23	O_vs	O	Output vertical sync signal	
24	O_hs	O	Output horizontal sync signal	
25	O_de	O	Output data valid signal	
26	O_data0	O	Output lane0 data If "Bit Per Pixel" is set to 18: - When the Bits Per Pixel Coefficient is 1 and the data width is 18 bits, the format is {B, G, R}. - When the Bits Per Pixel Coefficient is 2 and the data width is 36 bits, the format is {B₁,G₁,R₁,B₀,G₀,R₀}. - When the Bits Per Pixel Coefficient is 4 and the data width is 72 bits, the format is {B₃,G₃,R₃,B₂,G₂,R₂, B₁,G₁,R₁,B₀,G₀,R₀}. If "Bit Per Pixel" is set to 24: - When the Bits Per Pixel Coefficient is 1 and the data width is 24 bits, the format is {B, G, R}. - When the Bits Per Pixel Coefficient is 2 and the data width is 48 bits, the format is {B₁,G₁,R₁,B₀,G₀,R₀}. - When the Bits Per Pixel Coefficient is 4 and the data width is 96 bits, the format is {B₃,G₃,R₃,B₂,G₂,R₂, B₁,G₁,R₁,B₀,G₀,R₀}. If "Bit Per Pixel" is set to 30: - When the Bits Per Pixel Coefficient is 1 and the data width is 30 bits, the format is {B, G, R}. - When the Bits Per Pixel Coefficient is	

No.	Signal Name	I/O	Description	Note
			2 and the data width is 60 bits, the format is {B ₁ ,G ₁ ,R ₁ ,B ₀ ,G ₀ ,R ₀ }. When the Bits Per Pixel Coefficient is 4 and the data width is 120 bits, the format is {B₃,G₃,R₃,B₂,G₂,R₂,B₁,G₁,R₁,B₀,G₀,R₀}.	
27	O_data1	O	Output lane1 data; Its functional definition is the same as O_data0. For detailed information, refer to the O_data0 signal description.	
28	O_data2	O	Output lane2 data; Its functional definition is the same as O_data0. For detailed information, refer to the O_data0 signal description.	
29	O_data3	O	Output lane3 data; Its functional definition is the same as O_data0. For detailed information, refer to the O_data0 signal description.	

3.5 Parameter Configuration

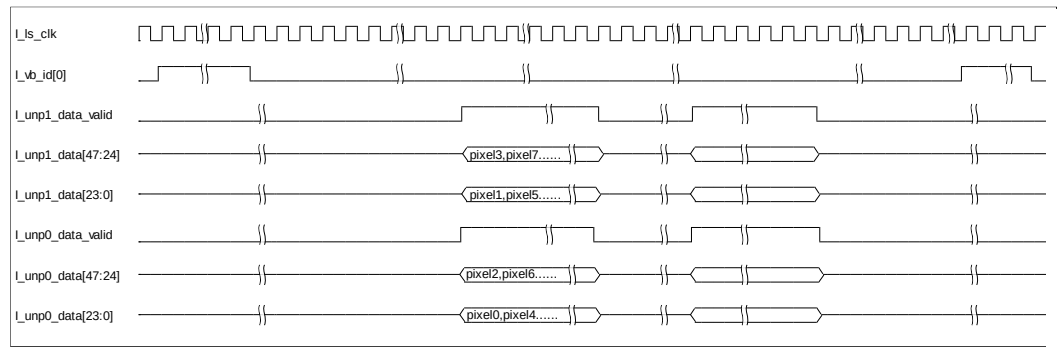
Table 3-3 EDP RX Desteer Parameters

No.	Name	Range	Default	Description
1	User Clock Ratio	1:20/1:40/1:80	1:20	Ratio of user clock to serial clock
2	Lanes Number	1, 2, 4	1	Number of lanes for main link
3	Bits Per Pixel	18/24/30	24	Bits per pixel
4	Line Buffer Depth	1024/2048/4096/8192/16384	4096	Data line buffer depth
5	Synchronization Type	Frame Synchronization With Line Complete/Line Synchronization	Frame Synchronization With Line Complete	Synchronization Type; for the details, you can see 3.7 Synchronization Type .
6	Generated VS Delay Lines	0~7	3	Generate VS delay lines
7	Bits Per Pixel Coefficient	1/2/4	1	Bits per pixel coefficient

3.6 Timing Description

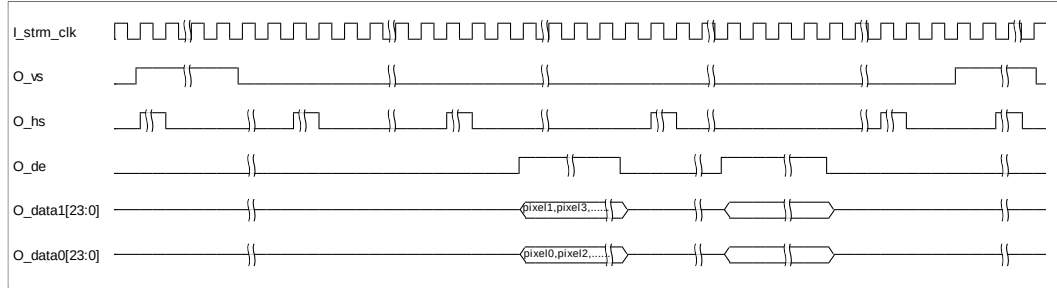
This section describes the timing of Gowin EDP RX Desteer IP.

The EDP RX Desteer input interface timing (2 lanes) with the data width 48 bits is as shown in Figure 3-4.

Figure 3-4 EDP RX Desteer Input Interface Timing Diagram (2 Lanes)**Note!**

When the User Clock Ratio is 1:40 and the Channel Number is 2 or 4 lanes, 48 bits of pixel data per lane are output non-sequentially in the order, as shown in above figure.

The EDP RX Desteer output interface timing (2 lanes) with the data width 24 bits is as shown in Figure 3-5.

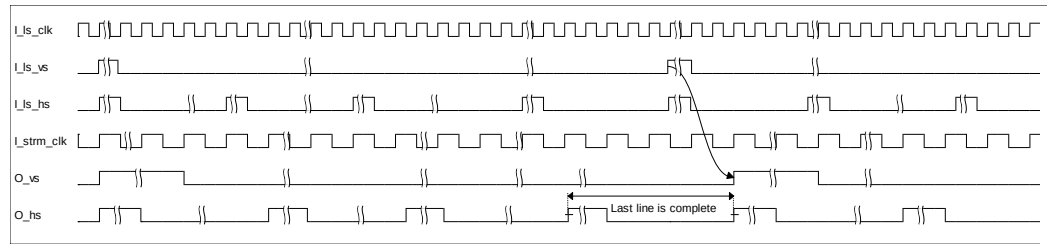
Figure 3-5 EDP RX Desteer Output Interface Timing Diagram (2 Lanes)

3.7 Synchronization Type

The data decoded by EDP Decoder IP remains in the `ls_clk` clock domain, while the EDP RX Desteer output is in the `strm_clk` clock domain. If the frequencies of `ls_clk` and `strm_clk` are not perfectly matched, there will be synchronization issues. In video processing, there are three synchronization modes

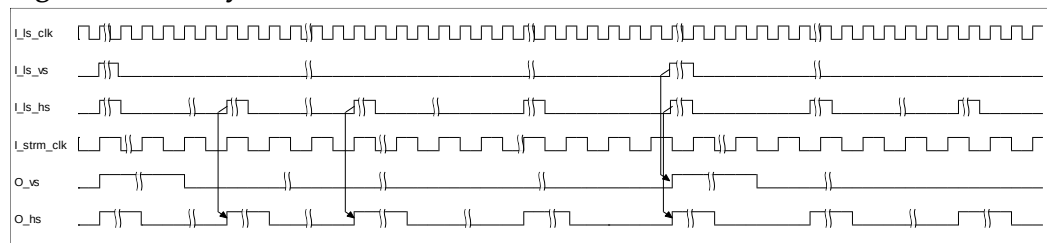
1. Frame Synchronization with Line Complete

When the `ls_vs` frame synchronization pulse arrives, if the last line in the `strm_clk` clock domain has not yet finished, the `O_vs` signal will not be immediately output. Instead, it waits until the horizontal count of the last line is completed before outputting. This ensures that each line output in the `strm_clk` clock domain is complete. However, this can cause an issue where the total number of lines in a frame will have a deviation of one line every so often.

Figure 3-6 Frame Synchronization with Line Complete

2. Line Synchronization

When the `I_ls_hs` line synchronization pulse arrives, the `O_hs` signal is immediately output. Similarly, when the `I_ls_vs` frame synchronization pulse arrives, the `O_vs` signal is also immediately output. This results in the horizontal count for each line in the `stm_clk` clock domain being slightly different, with at least a one-clock deviation.

Figure 3-7 Line Synchronization

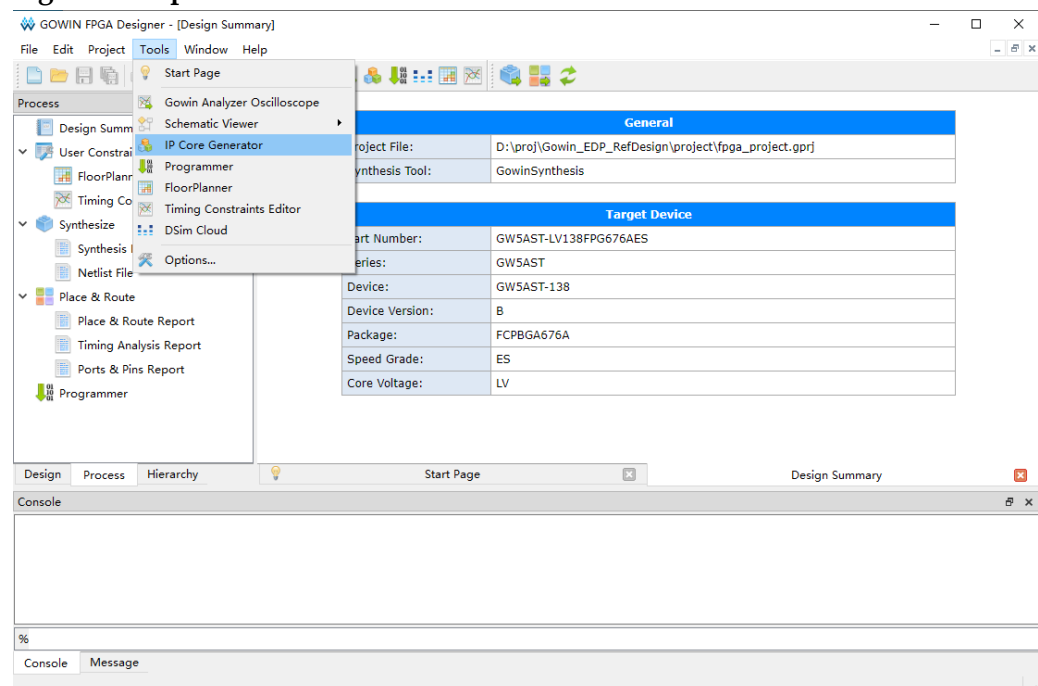
4 Interface Configuration

You can use IP core generator tool in Gowin Software to call and configure Gowin EDP RX Desteer IP.

1. Open IP Core Generator

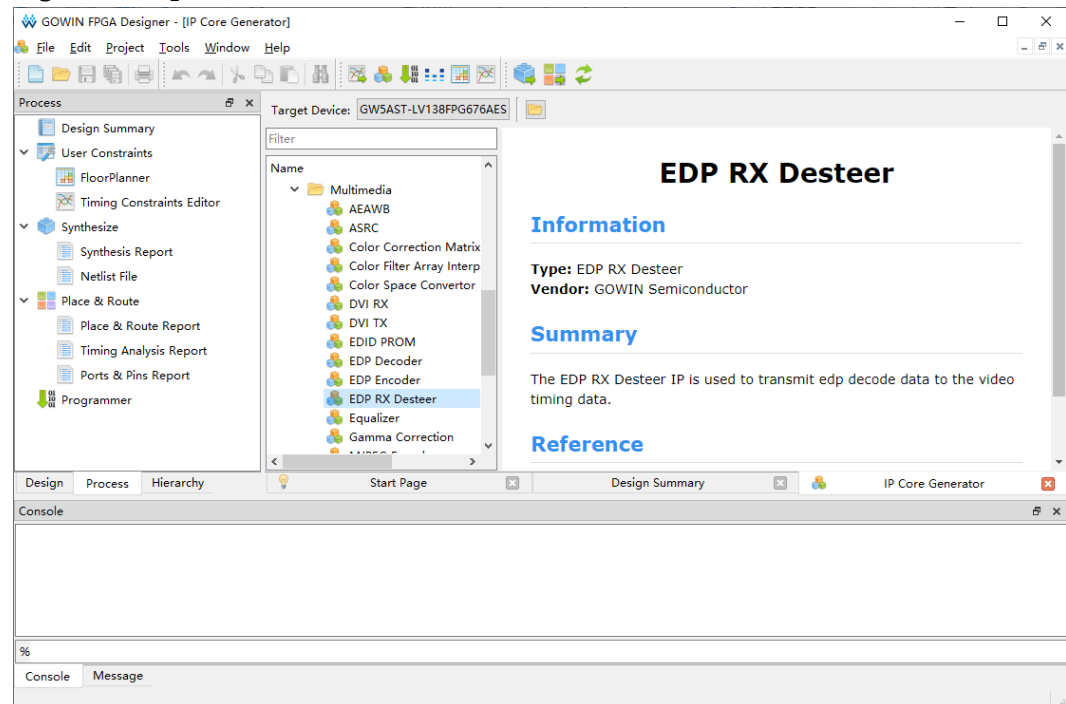
After creating the project, click the "Tools" tab in the upper left, click "IP Core Generator" from the drop-down list to open Gowin IP Core Generator, as shown in Figure 4-1.

Figure 4-1 Open IP Core Generator



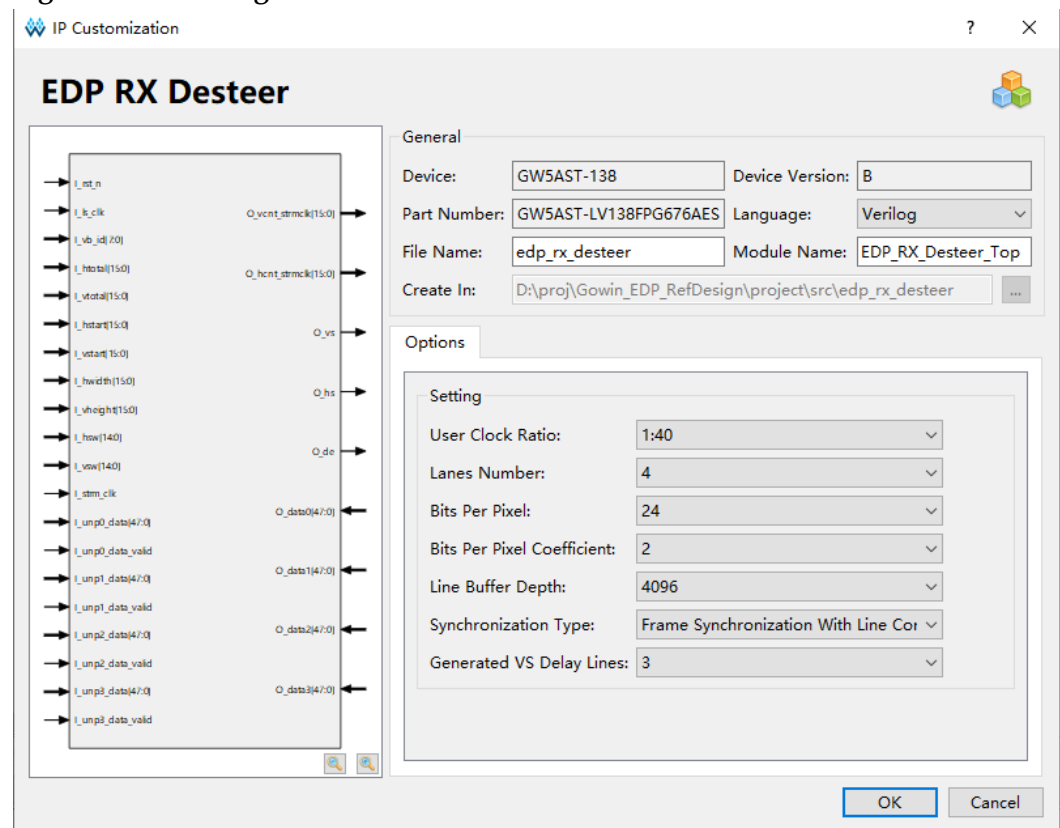
2. Open EDP RX Desteer IP Core

Click "Multimedia" and double click "EDP RX Desteer" to open the configuration interface, as shown in Figure 4-2 .

Figure 4-2 Open EDP RX Desteer IP core

3. EDP RX Desteer IP Core Port Interface

On the left of the configuration interface is the port diagram of EDP RX Desteer IP core, as shown in Figure 4-3.

Figure 4-3 Port Diagram of EDP RX Desteer IP

4. Configure General Information

See the project general information in the upper part of the configuration interface. Take GW5AST-138 FPG676A package as an example. The "Module Name" displays the top-level file name of the generated project, and the default is "EDP_RX_Desteer_Top"; and you can modify the name. The "File Name" displays the folder generated by the IP core, which contains the files required by EDP RX Desteer IP core, and the default is "edp_rx_desteer", and you can modify the path. "Create In" displays the path of IP core folder, and the default is "\project\src\edp_rx_desteer"; you can modify the path.

Figure 4-4 General Tab

General			
Device:	GW5AST-138	Device Version:	B
Part Number:	GW5AST-LV138FPG676AES	Language:	Verilog
File Name:	edp_rx_desteer	Module Name:	EDP_RX_Desteer_Top
Create In:	D:\proj\Gowin_EDP_RefDesign\project\src\edp_rx_desteer ...		

5. Options Tab

In this tab, you need to configure EDP RX Desteer parameters.

Figure 4-5 Options Tab

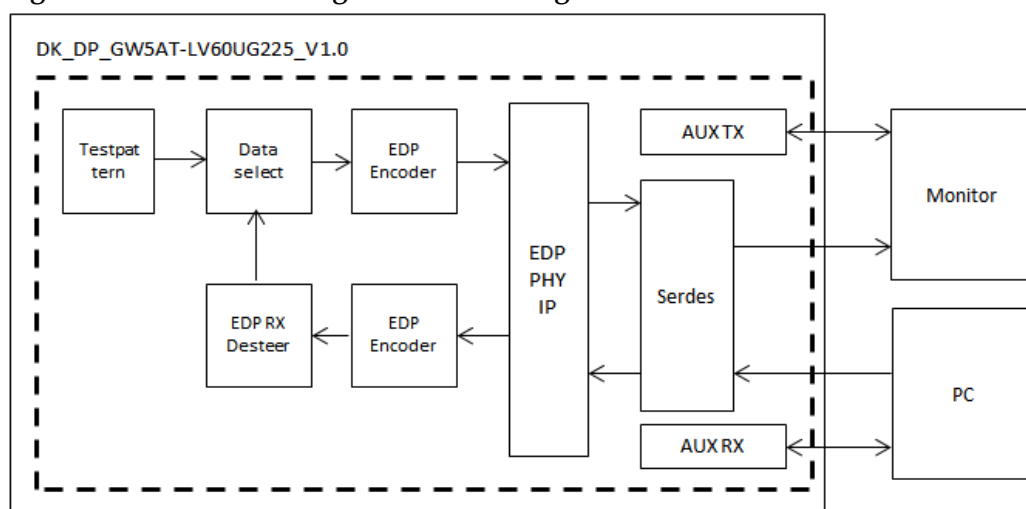
Options	
Setting	
User Clock Ratio:	1:40
Lanes Number:	4
Bits Per Pixel:	24
Bits Per Pixel Coefficient:	2
Line Buffer Depth:	4096
Synchronization Type:	Frame Synchronization With Line Cor
Generated VS Delay Lines:	3

5 Reference Design

This chapter is intended to introduce the usage and structure of the reference design of EDP RX Desteer IP. Please see the [reference design](#) for details at Gowinsemi website.

Take DK_DP_GW5AT-LV60UG225_V1.0 development board as an example, the diagram is as shown in Figure 5-1. For more information about the development boards, see the details at Gowinsemi website.

Figure 5-1 Reference Design Instance 1 Diagram



In the reference design, there are DP TX and DP RX. The DP TX generates test pattern video signals through Testpattern module; then encode them through EDP Encoder module, input them to EDP PHY IP to convert them into serial signals, and output them to DP display. If no data is received, the DP RX continuously displays the test pattern. For the DP RX, PC outputs DP signals; then convert them to parallel signals through EDP PHY IP, decode them through the EDP Decoder module, convert the format through the EDP RX Desteer module, and then output them to the data selection module before displaying them on the monitor.

6 File Delivery

The file delivery for Gowin EDP RX Desteer IP includes the documentation, the design source code, and the reference design.

6.1 Documentation

The folder mainly contains the user guide in PDF version.

Table 6-1 Document List

Name	Description
IPUG1083, Gowin EDP RX Desteer IP User Guide	Gowin EDP RX Desteer IP User Guide, namely this one.

6.2 Design Source Code (Encryption)

The encryption code folder contains the RTL encryption code of Gowin EDP RX Desteer IP used for the GUI, to generate the IP core as needed.

Table 6-2 Design Source Code List of EDP RX Desteer

Name	Description
edp_rx_desteer.v	The top-level file of the IP core, which provides users with interface information, encrypted.

6.3 Reference Design

Gowin EDP RefDesign folder contains the netlist file, user reference design, constraints file, top-level file and the project file for Gowin EDP RX Desteer IP.

Table 6-3 Gowin EDP RefDesign Folder Content List

Name	Description
test_top.v	The top module of reference design
fpga_project.cst	Project physical constraints file
fpga_project.sdc	Project timing constraints file
key_debounce.v	Debounce module file
pll_init.v	PLL initialization module file
rst_gen.v	Reset generation module file
serdes	EDP PHY IP folder
testpattern.v	Test pattern generation module

Name	Description
auxlink	Auxiliary channel (AUX) communication folder
gowin_pll	PLL IP folder
edp_decoder	EDP receive module folder
edp_encoder	EDP transmit module folder
edp_rx_desteer	EDP RX desteer module folder

