



# Gowin 10G Ethernet MAC IP User Guide

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**Revision History**

| Date       | Version | Description                                                                                                                                                                                                                                   |
|------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 02/02/2024 | 1.0E    | Initial version published.                                                                                                                                                                                                                    |
| 03/09/2026 | 1.1E    | <ul style="list-style-type: none"><li>● The CRC processing framework optimized.</li><li>● FCS Forward: The tx_fcs_fwd_ena_i and rx_fcs_fwd_ena_i control signals have been removed; configuration is now performed through the GUI.</li></ul> |

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# 1 About This Guide

## 1.1 Purpose

Gowin 10G Ethernet MAC IP user guide aims to help users quickly learn the features, functions and usage of Gowin 10G Ethernet MAC IP. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.12.02 (64-bit). As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

## 1.2 Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at [www.gowinsemi.com](http://www.gowinsemi.com):

- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1104, GW5AST series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

## 1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

| Terminology and Abbreviations | Meaning               |
|-------------------------------|-----------------------|
| DDR                           | Double Data Rate      |
| IP                            | Intellectual Property |

| Terminology and Abbreviations | Meaning              |
|-------------------------------|----------------------|
| IFG                           | Inter-Frame Gap      |
| LUT                           | Look-up Table        |
| MAC                           | Media Access Control |
| SDR                           | Single Data Rate     |

## 1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: [www.gowinsemi.com](http://www.gowinsemi.com)

E-mail: [support@gowinsemi.com](mailto:support@gowinsemi.com)

# 2 Overview

This manual describes 10G Ethernet MAC IP, which realized the function description of the 10G-rate Ethernet MAC layer in the IEEE 802.3 protocol. Gowin 10G Ethernet MAC IP provides users with a generic access interface that can be integrated into devices requiring a 10G-rate Ethernet MAC. This type of connection is commonly used in communication applications.

**Table 2-1 Gowin 10G Ethernet MAC IP**

| Gowin 10G Ethernet MAC IP |                                      |
|---------------------------|--------------------------------------|
| Logic Resource            | See Table 2-2.                       |
| Delivered Doc.            |                                      |
| Design Files              | Verilog (encryption)                 |
| Reference Design          | Verilog                              |
| TestBench                 | Verilog                              |
| Test and Design Flow      |                                      |
| Synthesis Software        | GowinSynthesis                       |
| Application Software      | Gowin Software (V1.9.9.01 and above) |

**Note!**

For the devices supported, you can click [here](#) to get the information.

## 2.1 Features and Performance

## 2.2 Features

- Supports 32-bit and 64-bit XGMII interfaces
- Complies with IEEE 802.3 clause 46
- Supports rate 10G
- Supports full-duplex
- Allows users to choose whether to automatically add and check CRC
- Supports automatic addition of padding
- Supports Ethernet frame error statistics
- Supports configurable IFG

- Supports Jumbo mode

## 2.3 Operating Frequency

Gowin 10G Ethernet MAC IP operates at 156.25MHz.

## 2.4 Resource Utilization

Table 2-2 shows the resource utilization. For the resource utilization of other devices, please refer to later release information.

**Table 2-2 Resource Utilization**

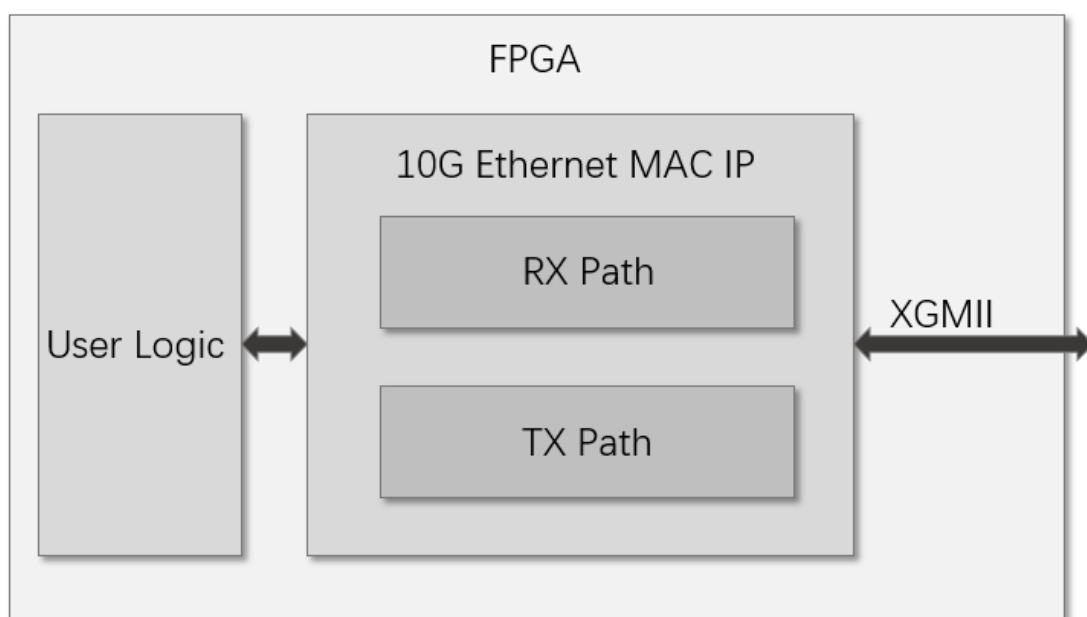
| TX FCS Forward | RX FCS Forward | LUTs | REGs | Device Series | Speed Level |
|----------------|----------------|------|------|---------------|-------------|
| Disable        | Disable        | 3007 | 3630 | GW5AST-138    | C2          |
| Disable        | Enable         | 3015 | 3620 |               |             |
| Enable         | Disable        | 1922 | 2877 |               |             |
| Enable         | Enable         | 1896 | 2867 |               |             |

# 3 Functional Description

## 3.1 Structure

As shown in Figure 3-1, Gowin 10G Ethernet MAC IP mainly includes modules such as RX Path, TX Path, etc. The User Logic in Figure 3-1 represents the user design within the FPGA.

Figure 3-1 Block Diagram of Gowin 10G Ethernet MAC IP



- The RX Path module performs the conversion from XGMII data format to user data format and implements functions such as CRC, PAD, frame statistics, etc.
- The TX Path module performs the conversion from user data format to XGMII data format and implements functions such as CRC, IFG configuration, frame statistics, error indication, etc.

## 3.2 Function and Interface Description

### 3.2.1 Reset

The IP supports asynchronous resets for the receive and transmit directions separately. Refer to Table 4-1 for the reset signal descriptions.

### 3.2.2 XGMII

The IP supports two XGMII interface modes: SDR mode and DDR mode.

#### SDR Mode

When the "Interface" option is set to SDR, the IP operates in SDR mode. This mode uses single-edge data format. And this mode should be configured when the IP needs to connect to the internal XGMII interface of the FPGA (e.g., connecting to the 10G Serial Ethernet IP). You can see Table 4-1 for SDR mode signals.

#### DDR Mode

When the "Interface" option is set to DDR, the IP operates in DDR mode. This mode uses the double-edge data format and encoding defined in IEEE802.3 clause 46. And this mode should be configured when the FPGA needs to interface with an external XGMII chip. You can see Table 4-1 for DDR mode signals.

### 3.2.3 Configuration Function

The IP supports various configuration modes, allowing users to customize the IP based on their requirements.

#### FCS Forward Reception

When the user disables the FCS Forward reception function, the FCS field will not be output to the user side. The IP automatically verifies the FCS field and its results will be output to the corresponding field of rx\_statistics\_vector. When the user enables the FCS Forward reception function, the FCS field will be output to the user side. The IP still automatically verifies the FCS field and its results will be output to the corresponding field of rx\_statistics\_vector.

#### FCS Forward Transmit

When the user disables the FCS Forward transmit function, the user does not need to calculate and transmit the FCS field. The IP calculates the FCS field and adds it to the Ethernet frame automatically. When the user enables the FCS Forward transmit function, the user calculates the FCS field and transmits it to the IP on the user side.

#### Jumbo Reception Function

The IP supports the Jumbo reception function. When the user disables Jumbo function, the IP judges that the normal Ethernet frame length is 64 bytes to 1518 bytes (non-VLAN frames) or 64 bytes to 1522 bytes (VLAN frames). If the Ethernet frames received are not within the

above range, rx\_mac\_error will indicate that there are some errors on this frame and RX Length Error is 1 in rx\_statistics\_vector. When the user enables Jumbo function, the IP judges there is an error only if the Ethernet frames received are smaller than 64 bytes.

### Link Fault Transmit Configuration

Users can configure whether the XGMII interface of the IP sends the corresponding Link Fault frame when it receives a Link Fault frame according to the protocol.

When users configure the IP to enable Link Fault transmit, the XGMII transmission follows the following rules: when the XGMII interface of IP receives a Local Fault frame, its XGMII interface sends a Remote Fault frame; when the XGMII interface of IP receives a Remote Fault frame, its XGMII interface sends an Idle frame; when the XGMII interface of IP does not receive any Fault frame, its XGMII interface sends user data.

When users configure the IP to disable Link Fault transmit, the XGMII interface sends user data regardless of whether the XGMII interface of IP receives Link Fault frames.

### Inter-Frame Gap Transmit Configuration

Users can configure the minimum transmit Inter-Frame Gap. The minimum inter-frame gap can be configured from 12 bytes to 60 bytes in steps of 4 bytes.

### Configuration Interface

Users can set the above configurations through the configuration interface, and can see Table 4-1 for details on the configuration interface.

## 3.2.4 Ethernet Data

### Receive Data

Users can receive Ethernet data through the user-side interface provided by the IP, and the IP can convert XGMII-formatted data into user-side Ethernet data.

Figure 3-2 shows the reception timing when the Receive FCS Forward is disabled. When rx\_mac\_valid\_o transitions from 0 to 1, it indicates that the user is ready to receive data. Users need to determine which bytes of rx\_mac\_data\_o are valid based on rx\_mac\_valid\_o and rx\_mac\_byte\_o. In this mode, only the data field is forwarded to the user side, and the FCS field is not forwarded. When users detect rx\_mac\_last\_o as 1, it indicates the last clock cycle of Ethernet data is received. Users need to judge the valid bytes of the last clock cycle based on rx\_mac\_byte\_o. If there are errors in the received Ethernet data, rx\_mac\_error\_o and rx\_mac\_last\_o will be asserted simultaneously. Information on received data statistics and errors can be viewed through rx\_statistics\_vector\_o. rx\_statistics\_vector\_o indicates the status of received data, and it is valid when rx\_statistics\_valid\_o is 1.

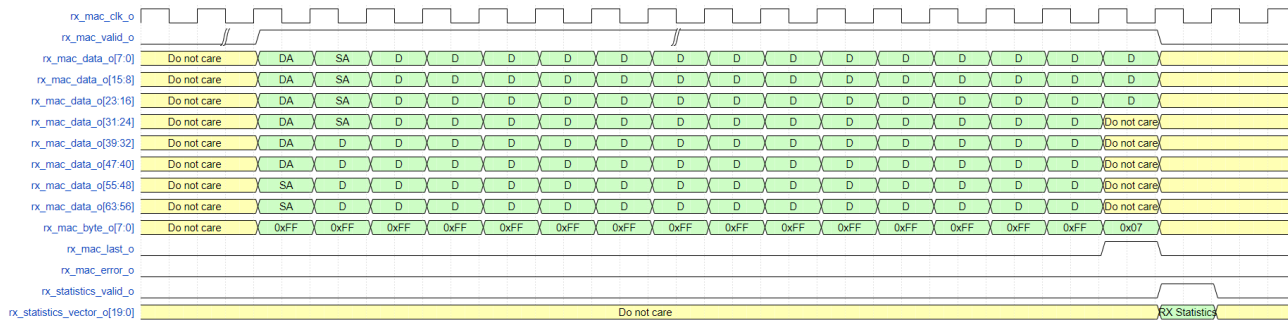
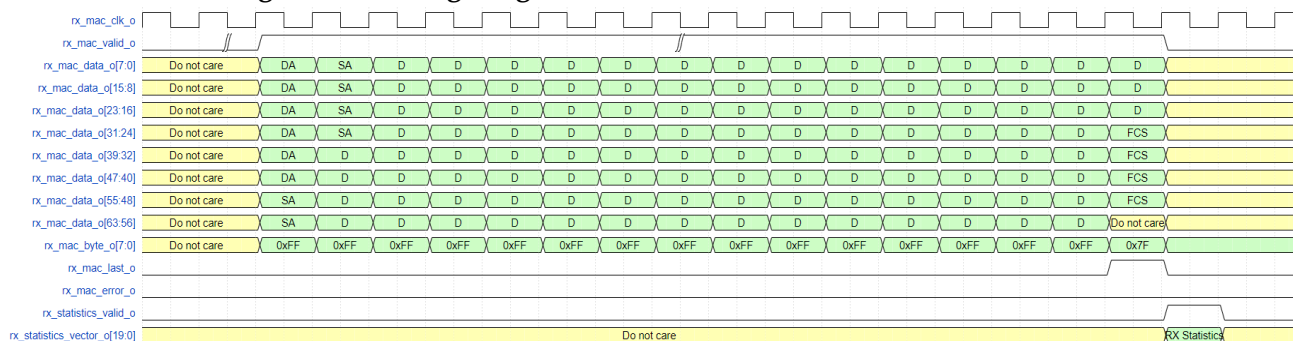
**Figure 3-2 Timing Diagram When Receive FCS Forward Disabled**

Figure 3-3 shows the reception timing when the Receive FCS Forward is enabled. Note that during the reception of data in the last clock cycle, the IP provides the FCS field, and simultaneously, rx\_mac\_byte\_o indicates the presence of the FCS field, and you can see Table 4-1 for the user-side interface description of receiving Ethernet data.

**Figure 3-3 Timing Diagram When Receive FCS Forward Enabled**

## Transmit Data

Users can transmit Ethernet data through the user-side interface provided by the IP, and the IP can convert user-side Ethernet data into XGMII data.

Figure 3-4 shows the transmission timing when the Transmit FCS Forward is disabled. When the user asserts tx\_mac\_valid\_i, it indicates it is ready to transmit data. Users need to continuously update the data to be transmitted, tx\_mac\_data\_i, based on tx\_mac\_ready\_o. In this mode, users only need to transmit data without transmitting the FCS field; the IP will automatically calculate the FCS and add it after transmitting the last data. When transmitting the last data, users need to assert tx\_mac\_last\_i for one clock cycle, indicating that the data for this cycle is the last data to be transmitted. Simultaneously, users need to use tx\_mac\_byte\_i to indicate which bytes of the last data need to be transmitted. If users need to send Transmit error propagation during the data transmission, they should assert tx\_mac\_error\_i for one clock cycle at the corresponding position. Information on transmit data statistics and errors can be viewed through tx\_statistics\_vector\_o. tx\_statistics\_vector\_o indicates the status of transmit data and is valid when tx\_statistics\_valid\_o is 1.

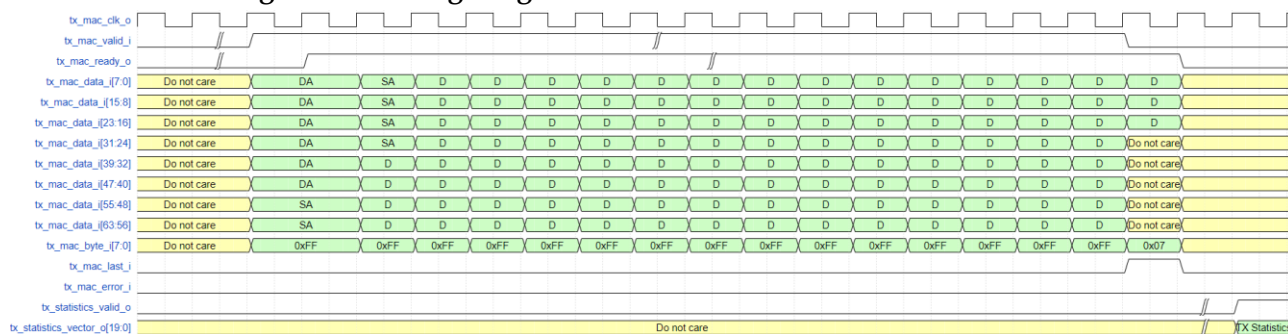
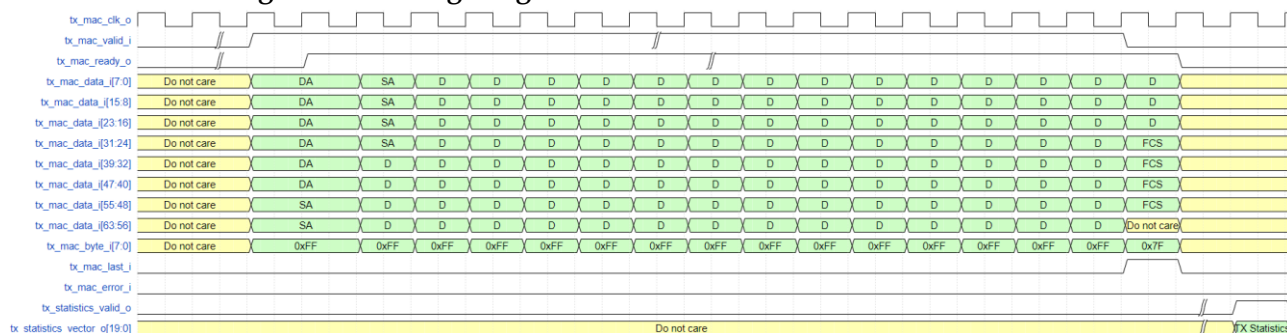
**Figure 3-4 Timing Diagram When Transmit FCS Forward Disabled**

Figure 3-5 shows the transmission timing when the Transmit FCS Forward is enabled. Note that when transmitting data in the last clock cycle, users need to transmit the FCS field. Simultaneously, tx\_mac\_byte\_i indicates the presence of the FCS field, and you can see Table 4-1 for the user-side interface description of transmitting Ethernet data.

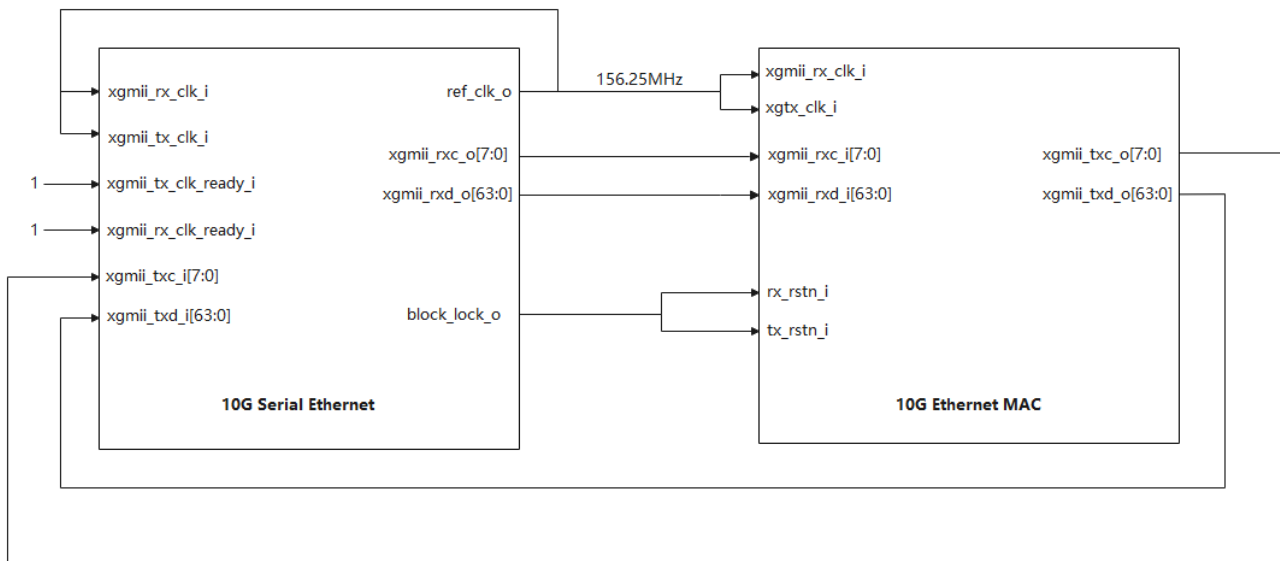
**Figure 3-5 Timing Diagram When Transmit FCS Forward Enabled**

## 3.2.5 Recommended Connection

### SDR Mode

Taking the connection to Gowin 10G Serial Ethernet IP as an example, as shown in Figure 3-6, where the 10G Ethernet MAC IP is configured in SDR mode. The connection between the two IPs is established as follows:

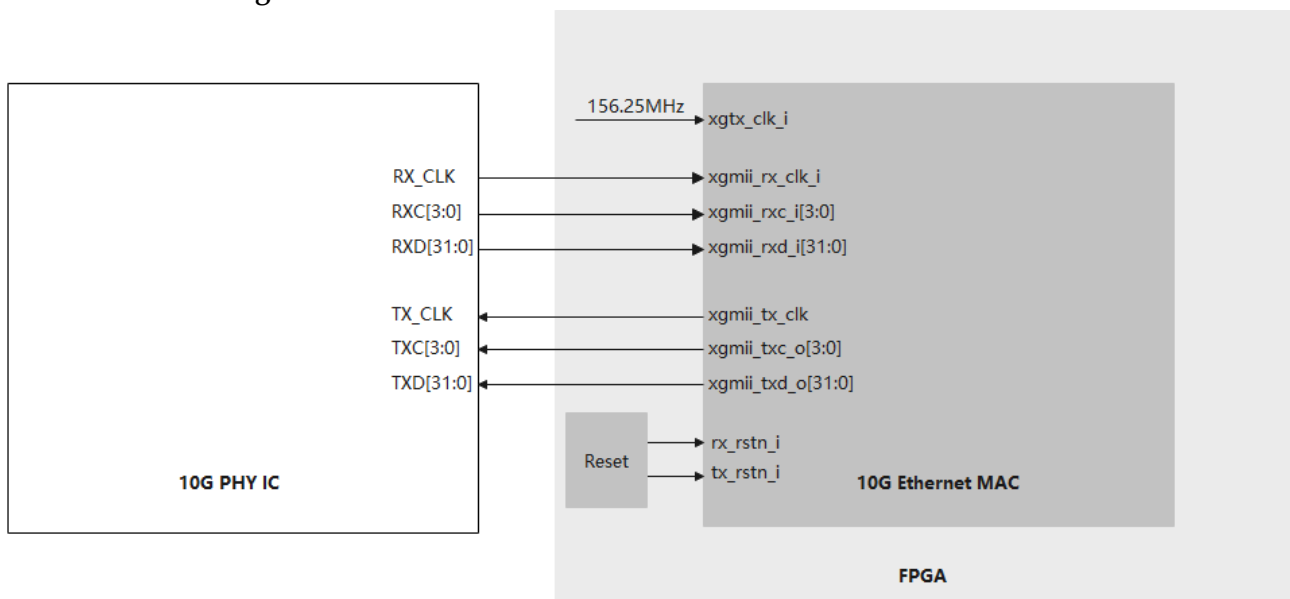
1. The XGMII interfaces of the two IPs are interconnected.
2. The 156.25MHz clock output from the 10G Serial Ethernet IP (ref\_clk\_o) serves as the clock for receiving and transmitting XGMII. It is connected to xgmii\_rx\_clk\_i and xgmii\_tx\_clk\_i of the 10G Serial Ethernet IP, and xgmii\_rx\_clk\_i and xgtx\_clk\_i of the 10G Ethernet MAC IP. This connection ensures that the XGMII receive and transmit clocks of both IPs are in sync in terms of frequency and phase.
3. The block\_lock\_o from the 10G Serial Ethernet IP is connected to rx\_rstn\_i and tx\_rstn\_i of the 10G Ethernet MAC IP. This connection ensures that the release of TX/RX reset in the 10G Ethernet MAC IP occurs after the block in the 10G Serial Ethernet IP is synchronized.
4. For the clocking of the 10G Serial Ethernet IP, you can see [IPUG1178, Gowin 10G Serial Ethernet IP User Guide](#).

**Figure 3-6 Connection in SDR Mode**

### DDR Mode

Taking the connection to a PHY IC as an example, as shown in Figure 3-7, where the 10G Ethernet MAC IP is configured in DDR mode. The connection between PHY IC and the IP is established as follows:

1. The XGMII interface of the PHY IC is connected to the XGMII interface of the IP.
2. The IP's `xgtx_clk_i` receives a clock signal of 156.25MHz.
3. The `rx_rstn_i` of the IP is controlled by the user and can be released once `xgmii_rx_clk_i` is stable.
4. The `tx_rstn_i` of the IP is controlled by the user and can be released once `xgtx_clk_i` is stable.

**Figure 3-7 Connection in DDR Mode**

# 4 Port List

The I/O port of Gowin 10G Ethernet MAC IP is shown in Figure 4-1; for the descriptions, you can see Table 4-1.

**Figure 4-1 I/O Port Diagram of Gowin 10G Ethernet MAC IP**

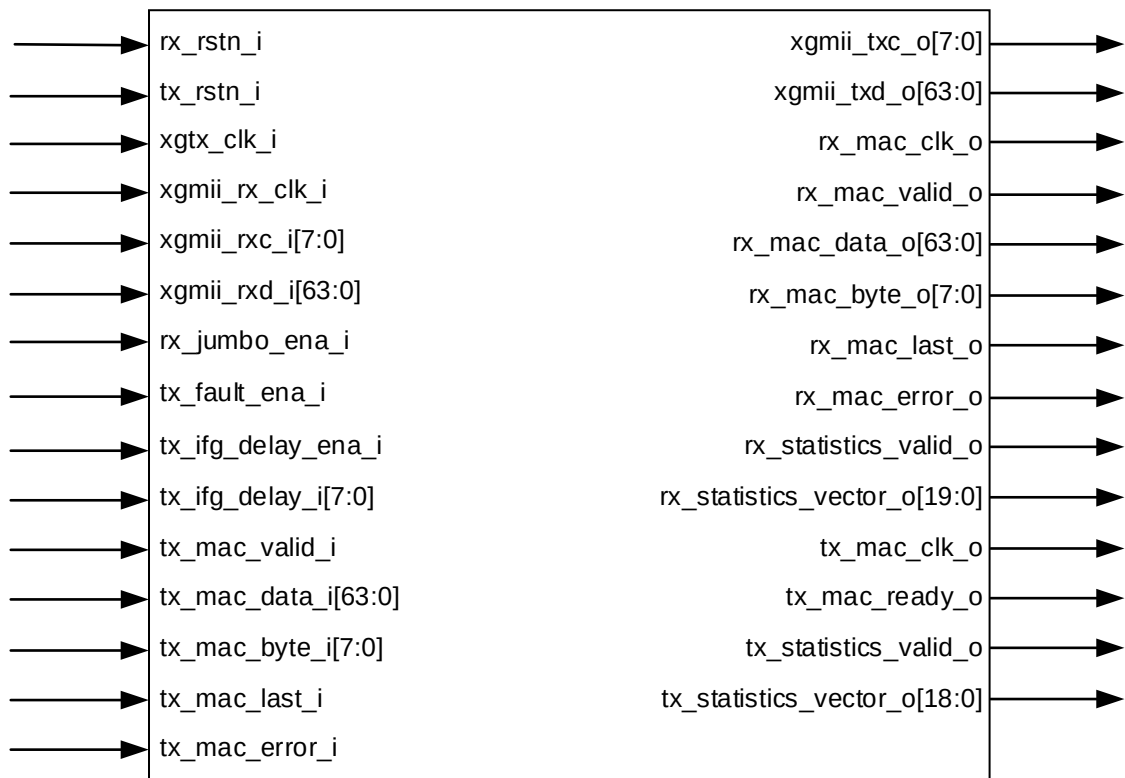


**Table 4-1 IO Port List of Gowin 10G Ethernet MAC IP**

| Signal                          | I/O    | Data Width | Description                                                        |
|---------------------------------|--------|------------|--------------------------------------------------------------------|
| <b>Reset</b>                    |        |            |                                                                    |
| rx_rstn_i                       | input  | 1          | Asynchronous reset input for RX, active-low                        |
| tx_rstn_i                       | input  | 1          | Asynchronous reset input for TX, active-low                        |
| <b>XGMII Interface-SDR Mode</b> |        |            |                                                                    |
| xgtx_clk_i                      | input  | 1          | XGMII TX clock input with a frequency of 156.25MHz                 |
| xgmii_txc_o                     | output | 8          | The output of XGMII transmitting TxC, synchronized with xgtx_clk_i |

| Signal                          | I/O    | Data Width | Description                                                                                                                                                                                                                                                                                                                                             |
|---------------------------------|--------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| xgmii_txd_o                     | output | 64         | The output of XGMII transmitting TXD, synchronized with xgtx_clk_i                                                                                                                                                                                                                                                                                      |
| xgmii_rx_clk_i                  | input  | 1          | The input of XGMII receiving RX_CLK with a frequency of 156.25MHz                                                                                                                                                                                                                                                                                       |
| xgmii_rxc_i                     | input  | 8          | The input of XGMII receiving RXC, synchronized with xgmii_rx_clk_i                                                                                                                                                                                                                                                                                      |
| xgmii_rxd_i                     | input  | 64         | The input of XGMII receiving RXD, synchronized with xgmii_rx_clk_i                                                                                                                                                                                                                                                                                      |
| <b>XGMII Interface-DDR Mode</b> |        |            |                                                                                                                                                                                                                                                                                                                                                         |
| xgtx_clk_i                      | input  | 1          | XGMII TX clock reference input with a frequency of 156.25MHz                                                                                                                                                                                                                                                                                            |
| xgmii_tx_clk_o                  | output | 1          | XGMII transmits TX_CLK                                                                                                                                                                                                                                                                                                                                  |
| xgmii_txc_o                     | output | 4          | XGMII transmits TXC                                                                                                                                                                                                                                                                                                                                     |
| xgmii_txd_o                     | output | 32         | XGMII transmits TXD                                                                                                                                                                                                                                                                                                                                     |
| xgmii_rx_clk_i                  | input  | 1          | XGMII receives RX_CLK                                                                                                                                                                                                                                                                                                                                   |
| xgmii_rxc_i                     | input  | 4          | XGMII receives RXC                                                                                                                                                                                                                                                                                                                                      |
| xgmii_rxd_i                     | input  | 32         | XGMII receives RXD                                                                                                                                                                                                                                                                                                                                      |
| <b>Configuration Interface</b>  |        |            |                                                                                                                                                                                                                                                                                                                                                         |
| rx_jumbo_ena_i                  | input  | 1          | Receive Jumbo<br>1: Enable receiving Jumbo<br>0: Disable receiving Jumbo                                                                                                                                                                                                                                                                                |
| tx_fault_ena_i                  | input  | 1          | Transmit Link Fault<br>1: Enable transmitting Link Fault<br>0: Disable transmitting Link Fault                                                                                                                                                                                                                                                          |
| tx_ifg_delay_ena_i              | input  | 1          | Transmit the minimum IFG configuration enable<br>1: Enable the minimum IFG configuration<br>0: Disable minimum IFG configuration, and the default minimum IFG is 12 bytes                                                                                                                                                                               |
| tx_ifg_delay_i                  | input  | 8          | Transmit minimum IFG<br>When tx_ifg_delay_ena_i is 1, the minimum IFG transmitted by IP is determined by tx_ifg_delay_i; when tx_ifg_delay_i is less than 3, the minimum IFG is 12 bytes; when tx_ifg_delay_i is greater than or equal to 3, the minimum IFG is the user-set value * 4 bytes.<br>When tx_ifg_delay_ena_i is 0, this setting is invalid. |
| <b>User Interface</b>           |        |            |                                                                                                                                                                                                                                                                                                                                                         |
| rx_mac_clk_o                    | output | 1          | User-side RX clock with the frequency of 156.25MHz                                                                                                                                                                                                                                                                                                      |
| rx_mac_valid_o                  | output | 1          | User-side receive enable, synchronized with rx_mac_clk_o                                                                                                                                                                                                                                                                                                |
| rx_mac_data_o                   | output | 64         | User-side receive data, synchronized with rx_mac_clk_o                                                                                                                                                                                                                                                                                                  |
| rx_mac_byte_o                   | output | 8          | User-side receive data valid byte indicator; each bit indicates the validity of 1 byte in rx_mac_data_o, synchronized with rx_mac_clk_o.<br>0: invalid<br>1: valid<br>[0]: Indicates rx_mac_data_o[7:0]<br>[1]: Indicates rx_mac_data_o[15:8]                                                                                                           |

| Signal                 | I/O    | Data Width | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------------------------|--------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                        |        |            | [2]: Indicates rx_mac_data_o[23:16]<br>[3]: Indicates rx_mac_data_o[31:24]<br>[4]: Indicates rx_mac_data_o[39:32]<br>[5]: Indicates rx_mac_data_o[47:40]<br>[6]: Indicates rx_mac_data_o[55:48]<br>[7]: Indicates rx_mac_data_o[63:56]                                                                                                                                                                                                                                                                                         |
| rx_mac_last_o          | output | 1          | Indicator for receiving last data on user-side, synchronized with rx_mac_clk_o                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| rx_mac_error_o         | output | 1          | Indicator for receiving Error frame on user-side, synchronized with rx_mac_clk_o                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| rx_statistics_valid_o  | output | 1          | Indicator for receiving statistics valid on user-side, synchronized with rx_mac_clk_o                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| rx_statistics_vector_o | output | 20         | Receive statistics information, synchronized with rx_mac_clk_o.<br>[15:0]: Receive data length, including the FCS field<br>[16]: Receive data length error<br>0: Correct<br>1: Error<br>[17]: Receive "Receive error" code during data reception<br>0: "Receive error" not received<br>1: "Receive error" received<br>[18]: Receive data CRC error<br>0: No error<br>1: Error occurred<br>[19]: Receive "control characters" during data reception<br>0: "control characters" not received<br>1: "control characters" received |
| tx_mac_clk_o           | output | 1          | User-side TX clock with frequency of 156.25MHz, synchronized with xgtx_clk_i                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| tx_mac_valid_i         | input  | 1          | User-side transmit enable, synchronized with tx_mac_clk_o                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| tx_mac_ready_o         | output | 1          | User-side transmit handshake signal, synchronized with tx_mac_clk_o. A value of 1 indicates that tx_mac_data_i has been received                                                                                                                                                                                                                                                                                                                                                                                               |
| tx_mac_data_i          | input  | 64         | User-side transmit data, synchronized with tx_mac_clk_o                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| tx_mac_byte_i          | input  | 8          | Indicator for valid bytes in transmit data on user-side; each bit indicates the validity of 1 byte in tx_mac_data_i, synchronized with tx_mac_clk_o.<br>0: invalid<br>1: valid<br>[0]: Indicates tx_mac_data_i[7:0]<br>[1]: Indicates tx_mac_data_i[15:8]<br>[2]: Indicates tx_mac_data_i[23:16]<br>[3]: Indicates tx_mac_data_i[31:24]<br>[4]: Indicates tx_mac_data_i[39:32]<br>[5]: Indicates tx_mac_data_i[47:40]<br>[6]: Indicates tx_mac_data_i[55:48]<br>[7]: Indicates tx_mac_data_i[63:56]                            |

| Signal                     | I/O    | Data Width | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------------------------|--------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| tx_mac_last_i              | input  | 1          | Indicator for transmitting last data on user-side, synchronized with tx_mac_clk_o                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| tx_mac_error_i             | input  | 1          | Transmit "Transmit error propagation enable" on user-side, synchronized with tx_mac_clk_o                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| tx_statistics_vali<br>d_o  | output | 1          | Indicator for TX statistics valid on user-side, synchronized with tx_mac_clk_o                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| tx_statistics_vect<br>or_o | output | 19         | <p>Transmit statistics information on user-side, synchronized with tx_mac_clk_o</p> <p>[15:0]: Length of transmit data, including FCS field</p> <p>[16]: Indicates that during the transmission of this frame; an Idle code was sent due to Remote Fault, indicating that this frame data was not sent successfully.</p> <p>0: Success</p> <p>1: Failure</p> <p>[17]: Indicates that during the transmission of this frame; a Remote Fault code was sent due to Local Fault, indicating that this frame data was not sent successfully.</p> <p>0: Success</p> <p>1: Failure</p> <p>[18]: Indicates the transmission of "Transmit error propagation" code during the transmission of data.</p> <p>0: "Transmit error propagation" not transmitted</p> <p>1: "Transmit error propagation" transmitted</p> |

# 5 Parameter Configuration

You can configure the static parameters and timing parameters of Gowin 10G Serial Ethernet MAC IP according to the design requirements, and you can refer to Table 5-1.

**Table 5-1 Static Parameters of Gowin 10G Ethernet MAC IP**

| Name                  | Description           | Option                                                                                |
|-----------------------|-----------------------|---------------------------------------------------------------------------------------|
| Interface             | Interface Mode        | SDR/DDR<br>SDR: XGMII in single data rate mode<br>DDR: XGMII in double data rate mode |
| Enable TX FCS Forward | Enable TX FCS Forward | Checked/Unchecked                                                                     |
| Enable RX FCS Forward | Enable RX FCS Forward | Checked/Unchecked                                                                     |

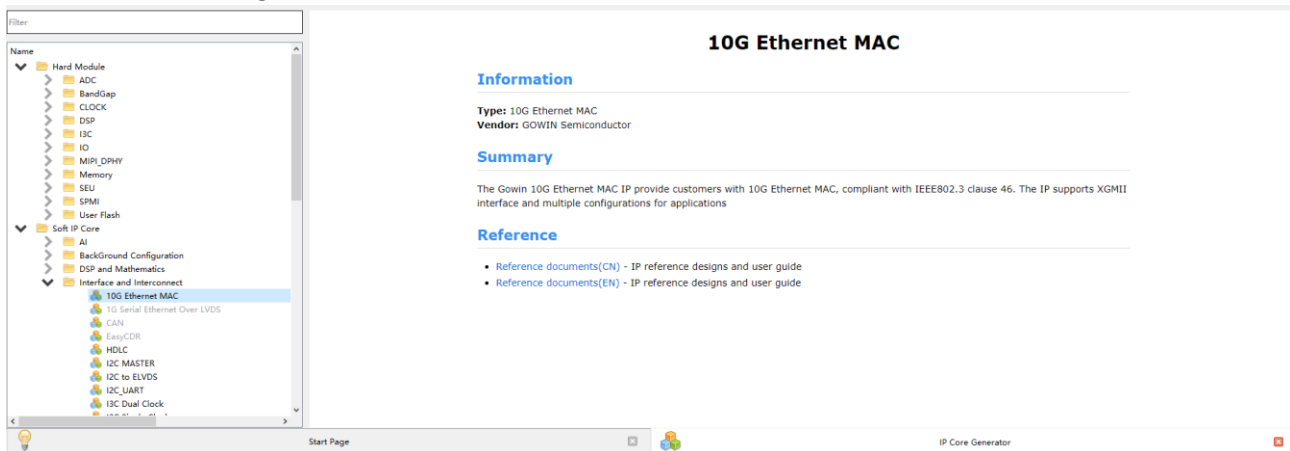
# 6 Interface Configuration

You can invoke and configure Gowin 10G Ethernet MAC IP using the IP Core Generator tool in the IDE. Taking SDR mode as an example, this section will introduce the configuration interface, configuration process, and configuration options.

## 1. Open IP Core Generator

After creating a project, you can click the "Tools" tab in the upper left, open the IP Core Generator via the drop-down list and select "10G Ethernet MAC", as shown in Figure 6-1.

Figure 6-1 IP Core Generator



## 2. 10G Ethernet MAC Ports

On the left of the configuration interface, it is the 10G Ethernet MAC IP ports diagram, and on the right, it is the IP options, as shown in Figure 6-2.

Figure 6-2 Gowin 10G Ethernet MAC IP Configuration Interface

IP Customization

## 10G Ethernet MAC

The diagram shows a central block with numerous input and output ports. Inputs on the left include rx\_nbi\_i, tx\_nbi\_i, rxpbi\_rx\_clk\_i, rxpbi\_clk\_i, rxpbi\_rx\_7Q, rxpbi\_rx\_6B0, rx\_jumbo\_wna\_i, tx\_fault\_wna\_i, tx\_1q\_delay\_wna\_i, tx\_1q\_delay\_17Q, tx\_mac\_valid\_i, tx\_mac\_data\_1B3Q, tx\_mac\_byte\_1Q\_0, tx\_mac\_lani\_i, and tx\_mac\_wncr\_i. Outputs on the right include rxpbi\_tx\_7Q, rxpbi\_tx\_6B3Q, rx\_mac\_clk\_o, rx\_mac\_valid\_o, rx\_mac\_data\_6B3Q, rx\_mac\_byte\_7Q, rx\_mac\_lani\_o, rx\_mac\_wncr\_o, rx\_statistics\_valid\_o, rx\_statistics\_vector\_19Q, tx\_mac\_clk\_o, tx\_mac\_ready\_o, tx\_statistics\_valid\_o, tx\_statistics\_vector\_1BQ, local\_fault\_o, and remote\_fault\_o.

**General**

Device:  Device Version:

Part Number:  Language:

File Name:  Module Name:

Create In:  ...

**Options**

Interface:

☐ Enable TX FCS Forward

☐ Enable RX FCS Forward

OK Cancel

# 7 Reference Design

See 10G Ethernet MAC [reference design](#) for details at Gowinsemi website.

