



Gowin SLVS-EC RX IP

User Guide

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Revision History

Date	Version	Description
12/08/2023	1.0E	Initial version published.
09/26/2025	1.1E	● o_pixel[16:31] ports added. ● Single-lane rate 4.752 Gbps supported. ● Bus Width configuration parameter added. ● Timing description added.
05/18/2026	1.1.1E	Added a development board note to chapter 5 Reference Design.

Contents

Contents	i
List of Figures	ii
List of Tables	iii
1 About This Guide	1
1.1 Purpose	1
1.2 Related Documents	1
1.3 Terminology and Abbreviations	1
1.4 Support and Feedback	2
2 Overview	3
2.1 Overview	3
2.2 Features	3
2.3 Resource Utilization	4
3 Functional Description	5
3.1 System Block Diagram	5
3.2 Function Modules	5
3.2.1 Structure Diagram	5
3.2.2 SerDes Clock	6
3.2.3 SerDes Data	6
3.3 Port List	7
3.4 Parameter Configuration	10
3.5 Timing Description	10
4 Interface Configuration	12
5 Reference Design	18
6 File Delivery	20
6.1 Documentation	20
6.2 Design Source Code (Encryption)	20
6.3 Reference Design	20

List of Figures

Figure 3-1 Gowin SLVS-EC RX IP System Diagram	5
Figure 3-2 Structure Diagram of Gowin SLVS-EC RX IP	6
Figure 3-3 Gowin SLVS-EC RX IP Port Diagram	7
Figure 3-4 Timing Diagram of Video Interface	11
Figure 4-1 Open IP Core Generator	12
Figure 4-2 Open SerDes IP Configuration Interface.....	13
Figure 4-3 Open SLVS-EC RX Configuration Interface.....	14
Figure 4-4 SLVS-EC RX Configuration Interface.....	15
Figure 4-5 General Information Configuration Interface.....	15
Figure 4-6 PHY Configuration.....	16
Figure 4-7 Channel Bonding	16
Figure 4-8 SLVS-EC RX IP in SerDes IP Configuration Interface.....	17
Figure 5-1 Block Diagram of Reference Design	18

List of Tables

Table 1-1 Terminology and Abbreviations	1
Table 2-1 Gowin SLVS-EC RX IP Overview	3
Table 2-2 Gowin SLVS-EC RX IP Resource Utilization	4
Table 3-1 Port List of Gowin SLVS-EC RX IP	8
Table 3-2 Gowin SLVS-EC RX IP Parameter	10
Table 6-1 Document List	20
Table 6-2 Gowin SLVS-EC RX IP File List.....	20
Table 6-3 Gowin SLVS-EC RX RefDesign Folder Content List.....	20

1 About This Guide

1.1 Purpose

The purpose of Gowin SLVS-EC RX IP is to help you learn the features and usage of Gowin SLVS-EC RX IP by providing the descriptions of features, functions, ports, timing, GUI and reference design, etc. The software screenshots and the supported products listed in this manual are based on Gowin Software V1.9.11. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

You can find the related documents at www.gowinsemi.com:

- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1118, GW5ART series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
CDR	Clock Data Recovery
CRC	Cyclic Redundancy Check
DC	Digital Camera
DE	Data Enable
ECC	Error Correction Code
FPGA	Field Programmable Gate Array

Terminology and Abbreviations	Meaning
HS	Horizontal Sync
IP	Intellectual Property
SerDes	Serializer/Deserializer
SLVS-EC	Scalable Low Voltage Signaling Embedded Clock
VICAP	Video Capture
VS	Vertical Sync

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Overview

Gowin SLVS-EC RX IP implements the functions described by Sony's SLVS-EC interface standard. It provides users with a universal access interface for high-frame-rate and high-resolution image capture. It is capable of converting high-speed serial data into DC (Digital Camera) timing and then transmitting it to the next-level module VICAP (Video Capture).

Gowin SLVS-EC RX IP is compliant with SLVS-EC Specification Version 1.2/2.0 and supports ECC/CRC. Gowin SLVS-EC RX IP provides users with a SerDes physical layer access interface, enabling users to easily implement the connection between the SLVS-EC protocol layer and the physical layer.

Table 2-1 Gowin SLVS-EC RX IP Overview

Gowin SLVS-EC RX IP	
Logic Resource	Please refer to Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features

- Supports 1, 2, 4, 6, 8 lanes configuration
- Single-line rate supports 1.188 – 4.752 Gbps
- Supports ECC/CRC

2.3 Resource Utilization

Gowin SLVS-EC RX IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW5AST series of FPGA as an instance, the resource utilization of Gowin SLVS-EC RX IP is as shown in Table 2-2.

Table 2-2 Gowin SLVS-EC RX IP Resource Utilization

Device	GW5AST-138
Register	1297
LUT	3859

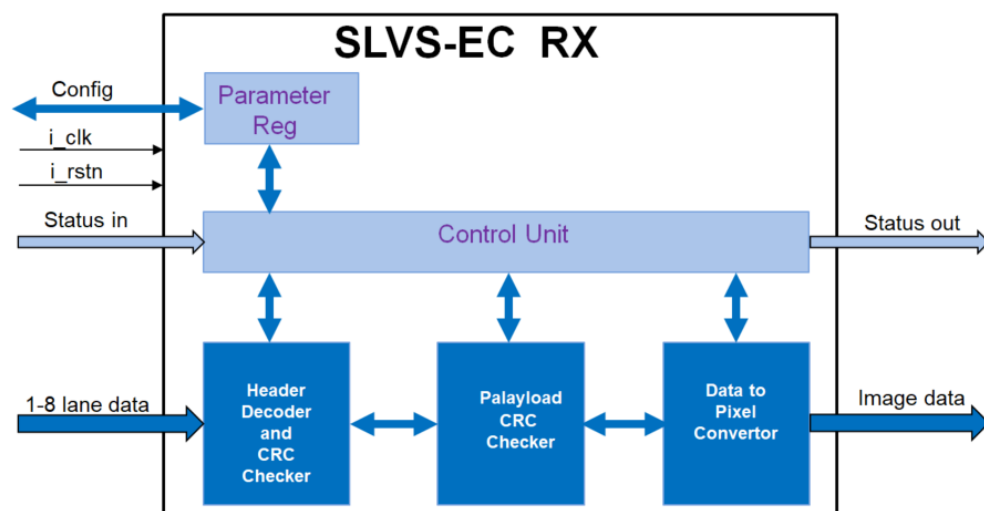
3 Functional Description

3.1 System Block Diagram

Gowin SLVS-EC RX IP can be capable of converting high-speed serial data into DC timing and then transmitting it to the next-level module VICAP.

The system diagram of Gowin SLVS-EC RX IP is shown in Figure 3-1.

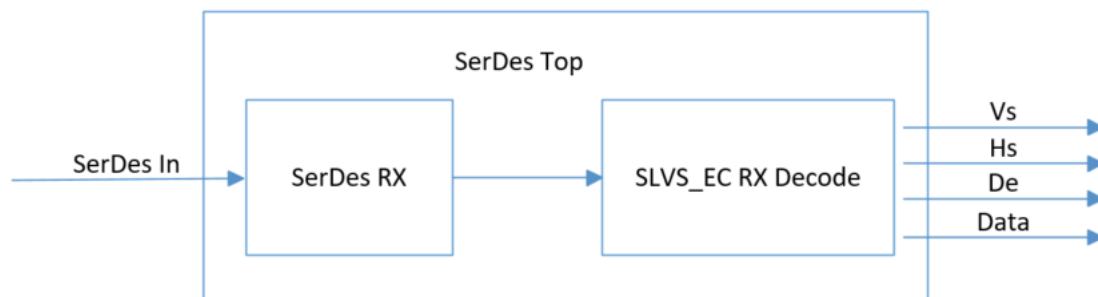
Figure 3-1 Gowin SLVS-EC RX IP System Diagram



3.2 Function Modules

3.2.1 Structure Diagram

The structure diagram of Gowin SLVS-EC RX IP is shown in Figure 3-2.

Figure 3-2 Structure Diagram of Gowin SLVS-EC RX IP

As shown above, the RX consists of the following 2 modules:

- SerDes RX: Receives serial data and outputs it in parallel
- SLVS-EC RX Decode: Decodes the parallel data provided by the SerDes

3.2.2 SerDes Clock

SerDes transmit clock is generated by CPLL/QPLL. When configuring a lane, the user needs to configure the rate of the lane, the PLL (CPLL/QPLL) used, as well as the reference clock source and its frequency. Based on the above configuration, the IP configures SerDes PLL to generate a high-speed clock for data transmission. At the same time, SerDes divides the high-speed clock based on user configuration and outputs it as a fabric transmit clock.

The SerDes receive clock is recovered by CDR (Clock Data Recovery), and the CDR outputs the recovered serial data clock for the receive module. At the same time, SerDes divides the serial data clock according to the user configuration and outputs it as a fabric receive clock.

When the user configures the data rate to 1.188 Gbps with Bus Width set to 16, the parallel data width is 20 bits, and the Fabric receive clock is $1.188 \text{ Gbps}/20 = 59.4 \text{ MHz}$.

When the user configures the data rate to 4.752 Gbps with Bus Width set to 32, the parallel data width is 40 bits, and the Fabric receive clock is $4.752 \text{ Gbps}/40 = 118.8 \text{ MHz}$.

3.2.3 SerDes Data

Gowin SLVS-EC RX IP SerDes data is fixed at 20 or 40 bits. SerDes TX data transmission order: The least significant bit of txdata is transmitted first. SerDes RX data transmission order: The least significant bit of rxdata is received first.

3.3 Port List

The IO port of Gowin SLVS-EC RX IP is shown in Figure 3-3.

Figure 3-3 Gowin SLVS-EC RX IP Port Diagram



The IO ports vary slightly depending on the parameters, and the details of IO port of Gowin SLVS-EC RX IP are shown in Table 3-1.

Table 3-1 Port List of Gowin SLVS-EC RX IP

Signal Name	I/O	Data Width	Description	Note
i_clk	input	1	SerDes receive clock input	- The input/output directions are all referenced to the SLVS-EC RX IP. - The values of sync code, deskew code, standby code, and idle code should match the corresponding register configuration values of the connected image sensor. - When Bus Width is set to 16, o_pixel16 to o_pixel31 are not visible. - The valid output bit width of o_pixel0 to o_pixel31 is equal to the input value of i_pixel_bit.
o_clk	output	1	Fabric receive clock; this clock is output to the user logic and is equal to i_clk.	
i_rst_n	input	1	Reset signal, active-low	
i_sync_symbol	input	[7:0]	sync code value	
i_deskew_symbol	input	[7:0]	deskew code value	
i_standby_symbol	input	[7:0]	standby code value	
i_idle_code_k	input	[3:0]	idle_code K character	
i_idle_code	input	[31:0]	idle code value	
i_lane_num	input	[7:0]	The number of lanes: 1, 2, 4, 6, 8	
i_line_length	input	[15:0]	The length of one line of image data	
i_pixel_bit	input	[7:0]	Pixel bit width: 8, 10, 12, 14, 16	
i_ecc_option	input	[1:0]	ECC selected 0: Disable 1: Enable (parity 2 byte) 2: Enable (parity 4 byte)	
i_crc_option	input	1	CRC selected 0: Disable 1: Enable	
i_baud_grade	input	[3:0]	Reserved parameter, fixed to 0.	
i_config	input	1	Reserved parameter for configuration setting, fixed to 1.	
i_standby	input	1	Reserved parameter for status setting, fixed to 0.	
i_setup	input	1	Reserved parameter for configuration setting, fixed to 1.	
i_phy_sync	input	1	Reserved parameter for receiving sync data signal, fixed to 1.	
i_lane0_data	input	[87:0]	SerDes RX data input port 1	
i_lane1_data	input	[87:0]	SerDes RX data input port 2	
i_lane2_data	input	[87:0]	SerDes RX data input port 3	
i_lane3_data	input	[87:0]	SerDes RX data input port 4	
i_lane4_data	input	[87:0]	SerDes RX data input port 5	
i_lane5_data	input	[87:0]	SerDes RX data input port 6	
i_lane6_data	input	[87:0]	SerDes RX data input port 7	
i_lane7_data	input	[87:0]	SerDes RX data input port 8	

Signal Name	I/O	Data Width	Description	Note
o_pixel0	output	[15:0]	Image data output port 0	
o_pixel1	output	[15:0]	Image data output port 1	
o_pixel2	output	[15:0]	Image data output port 2	
o_pixel3	output	[15:0]	Image data output port 3	
o_pixel4	output	[15:0]	Image data output port 4	
o_pixel5	output	[15:0]	Image data output port 5	
o_pixel6	output	[15:0]	Image data output port 6	
o_pixel7	output	[15:0]	Image data output port 7	
o_pixel8	output	[15:0]	Image data output port 8	
o_pixel9	output	[15:0]	Image data output port 9	
o_pixel10	output	[15:0]	Image data output port 10	
o_pixel11	output	[15:0]	Image data output port 11	
o_pixel12	output	[15:0]	Image data output port 12	
o_pixel13	output	[15:0]	Image data output port 13	
o_pixel14	output	[15:0]	Image data output port 14	
o_pixel15	output	[15:0]	Image data output port 15	
o_pixel16	output	[15:0]	Image data output port 16	
o_pixel17	output	[15:0]	Image data output port 17	
o_pixel18	output	[15:0]	Image data output port 18	
o_pixel19	output	[15:0]	Image data output port 19	
o_pixel20	output	[15:0]	Image data output port 20	
o_pixel21	output	[15:0]	Image data output port 21	
o_pixel22	output	[15:0]	Image data output port 22	
o_pixel23	output	[15:0]	Image data output port 23	
o_pixel24	output	[15:0]	Image data output port 24	
o_pixel25	output	[15:0]	Image data output port 25	
o_pixel26	output	[15:0]	Image data output port 26	
o_pixel27	output	[15:0]	Image data output port 27	
o_pixel28	output	[15:0]	Image data output port 28	
o_pixel29	output	[15:0]	Image data output port 29	
o_pixel30	output	[15:0]	Image data output port 30	
o_pixel31	output	[15:0]	Image data output port 31	
o_v_sync	output	1	vs output of image data	
o_h_sync	output	1	hs output of image data	
o_d_sync	output	1	de output of image data	
o_link_state	output	1	Operating state output; a rising edge indicates that the data parsing state has been entered.	
o_crc_state	output	1	CRC state output 0: Correct 1: Error	

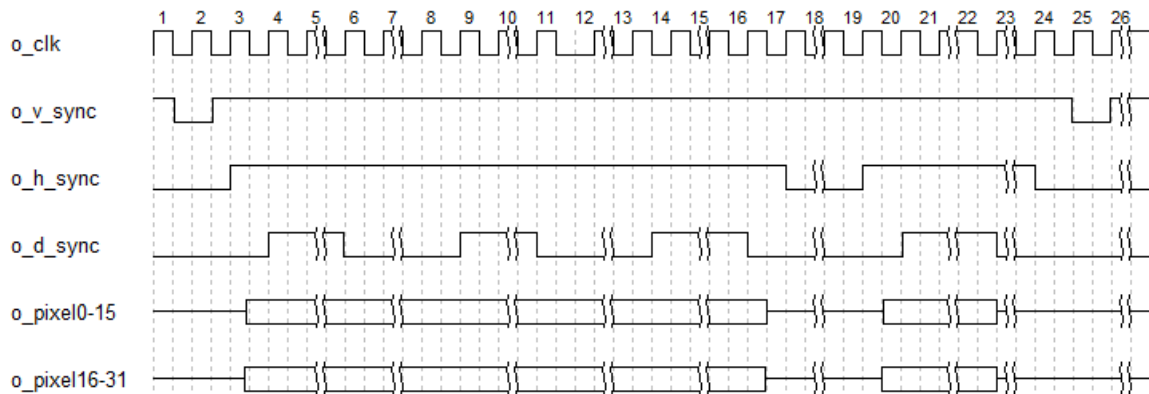
3.4 Parameter Configuration

Table 3-2 Gowin SLVS-EC RX IP Parameter

Name	Range	Default	Description
Bus Width	16/32	32	The parallel data output width of the SerDes. It is recommended to set this value to 32.
Err Correction	Q0/Q1	CRC	Err correction selection
Channel Selection	Q0 Lane0 Q0 Lane1 Q0 Lane2 Q0 Lane3 Q1 Lane0 Q1 Lane1 Q1 Lane2 Q1 Lane3	Q0 Lane0	SerDes lane selection
Loopback Mode	OFF LB_NES LB_FES LB_ENC	OFF	OFF: No Loopback, normal operating mode LB_NES: Loopback Near-End Side LB_FES: Loopback Far-End Side LB_ENC: Loopback Encoder
Line Rate	1.188 – 4.752 Gbps	1.188	Configure transmit data rate
Reference Clock Source	Q0 REFCLK0 Q0 REFCLK1 Q1 REFCLK0 Q1 REFCLK1	Q0 REFCLK0	Reference clock source selection
Reference Clock Frequency	50-500MHz	148.5	Configure reference clock source
PLL Selection	CPLL QPLL0 QPLL1	CPLL	Select PLL

3.5 Timing Description

This section describes the timing of Gowin SLVS-EC RX IP. The timing diagram of Gowin SLVS-EC RX video interface is shown in Figure 3-4.

Figure 3-4 Timing Diagram of Video Interface

The image data is received through the timing control signals and data ports described above. Note that on each rising edge of o_clk, when o_d_sync is high, image data is output through the ports o_pixel0 – o_pixel31. The duration of the high level of o_d_sync, as well as the low-level interval between two o_d_sync signals, is not fixed. As the number of lanes increases or the value of i_pixel_bit increases, the data volume input to Gowin SLVS-EC RX increases. To match the data rate, the duration of the o_d_sync high level will increase, and low-level interval between two o_d_sync signals will decrease accordingly. Conversely, when the data volume input to Gowin SLVS-EC RX IP decreases, the changes are in the opposite manner.

When the Bus Width is set to 16, the output on o_pixel16 – o_pixel31 is invalid.

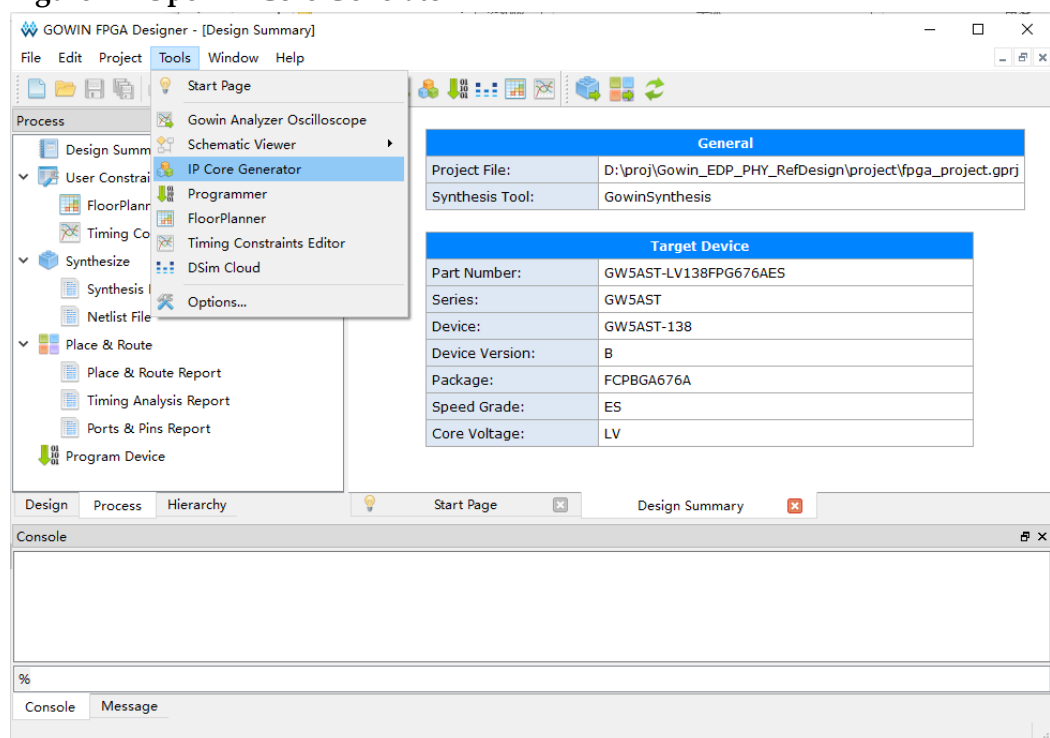
4 Interface Configuration

You can use IP core generator tool in Gowin Software to call and configure SLVS-EC RX IP.

1. Open IP Core Generator.

After creating the project, click the "Tools" tab in the upper left, click "IP Core Generator" from the drop-down list to open Gowin IP Core Generator, as shown in Figure 4-1.

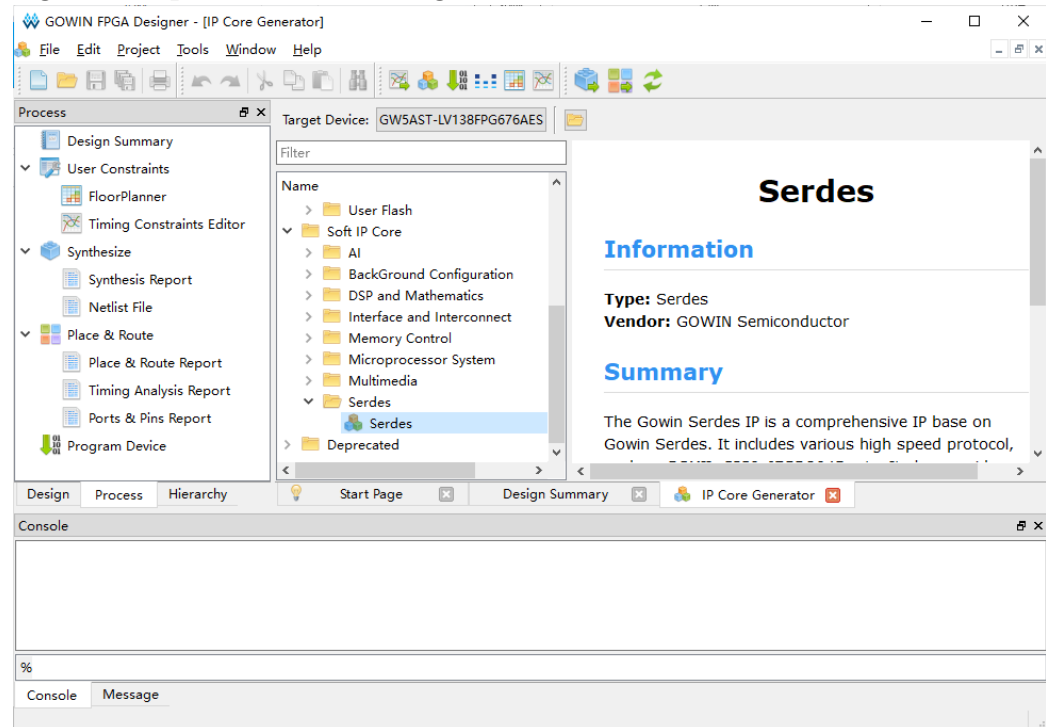
Figure 4-1 Open IP Core Generator



2. Open SerDes IP Configuration Interface

Double click "Serdes" to open the configuration interface, as shown in Figure 4-2.

Figure 4-2 Open SerDes IP Configuration Interface

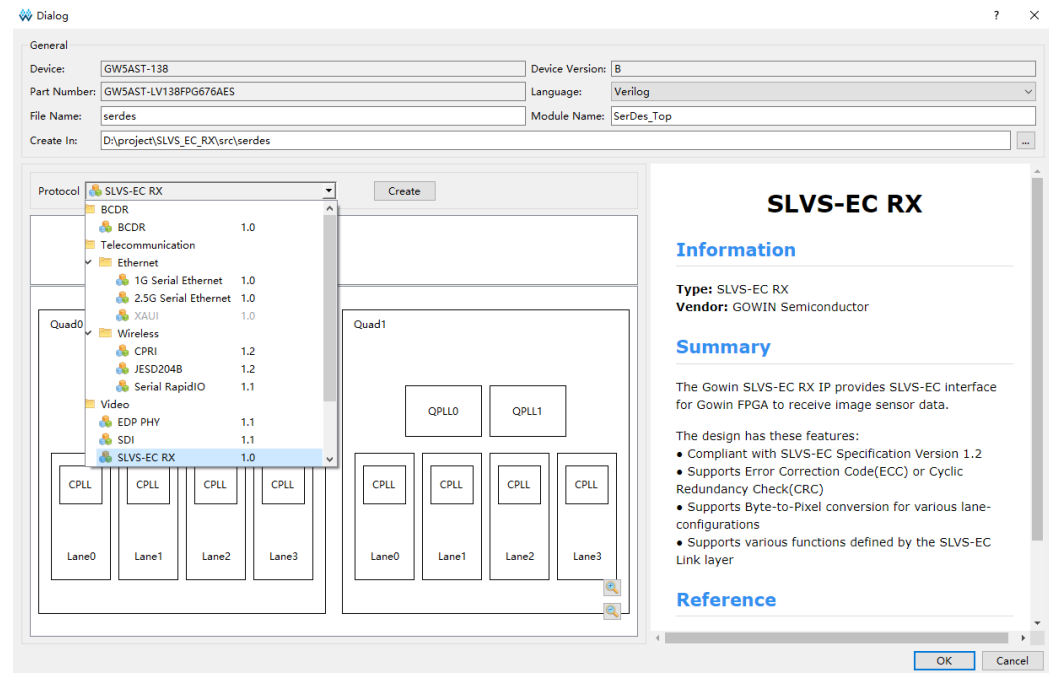


3. Open SLVS-EC RX configuration interface

First configure "General" tab in the SerDes IP interface.

- Device, Device Version, Part Number options: Part number settings, determined by the current project, and the user can not set.
- Language options: Support Verilog and VHDL, and choose the language as requirements, and the default is Verilog.
- File Name, Module Name, Create In options: SerDes file name, module name and the generated file path settings.

Then select the "SLVS-EC RX" in the "Protocol" on the SerDes IP configuration interface and click the "Create" button, as shown in Figure 4-3.

Figure 4-3 Open SLVS-EC RX Configuration Interface

4. Open SLVS-EC RX configuration interface

The configuration interface of SLVS-EC RX is shown in Figure 4-4. The port diagram is on the left, and the parameter configuration options are on the right.

Figure 4-4 SLVS-EC RX Configuration Interface

SLVS-EC RX

IP Customization

General

Device: GW5AST-138 Device Version: B

Part Number: GW5AST-LV138FPG676AES Language: Verilog

File Name: slvs_ec_rx Module Name: SLVS_EC_RX_Top

Create In: .376G_32bit\Gowin_SLVS_EC_RX_RefDesign\project\src\serdes\slvs_ec_rx

Basic Configuration PHY Configuration Channel Bonding

Bus Width: 32

Lane Num: 1

Pixel Bit: 8

Line Length: 1920 (4-8192)

Err Correction: ☒ CRC 1 ☐ ECC 0

OK Cancel

The general information configuration is as shown in Figure 4-5. See the project general information in the upper section of the configuration interface. The "Module Name" displays the top-level module name of the generated project, and the default is "xxx_Top"; you can modify the name. The "File Name" displays the folder generated by the IP, which contains the files required by the IP, and the default is "slvs_ec_rx", and you can modify the path.

Figure 4-5 General Information Configuration Interface

General

Device: GW5AST-138 Device Version: B

Part Number: GW5AST-LV138FPG676AES Language: Verilog

File Name: slvs_ec_rx Module Name: SLVS_EC_RX_Top

Create In: D:\project\SLVS_EC_RX\src\serdes\slvs_ec_rx

The "PHY Configuration" tab is as shown in Figure 4-6. There is a limitation between the line rate and the reference clock; make sure that the reference clock can generate the above line rate, which can also be detected through clicking "Calculate" button.

Figure 4-6 PHY Configuration

The figure shows the 'PHY Configuration' tab of a configuration window. It contains several sections:

- Channel Selection:** Eight dropdown menus for SLVS_EC_LANE0 through SLVS_EC_LANE7. The values are: Q1 Lane3, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2, and Q1 Lane3.
- RX Line Rate:** A text box containing '1.188' and a unit '(Gbps)'.
- Loopback Mode:** A dropdown menu set to 'OFF'.
- Refclk Selection:**
 - Reference Clock Source:** A dropdown menu set to 'Q1 REFCLK1'.
 - Reference Clock Frequency:** A text box containing '148.5' and a unit '(MHz)'.
- PLL Selection:**
 - PLL Selection Q0:** A dropdown menu set to 'NONE'.
 - PLL Selection Q1:** A dropdown menu set to 'QPLL1'.

A 'Calculate' button is located at the bottom right of the configuration area.

The "Channel Bonding" tab is as shown in Figure 4-7. If you are using two or more channels, "Channel Bonding" must be configured; select one lane as the Master Channel, and select the K character and its number.

Figure 4-7 Channel Bonding

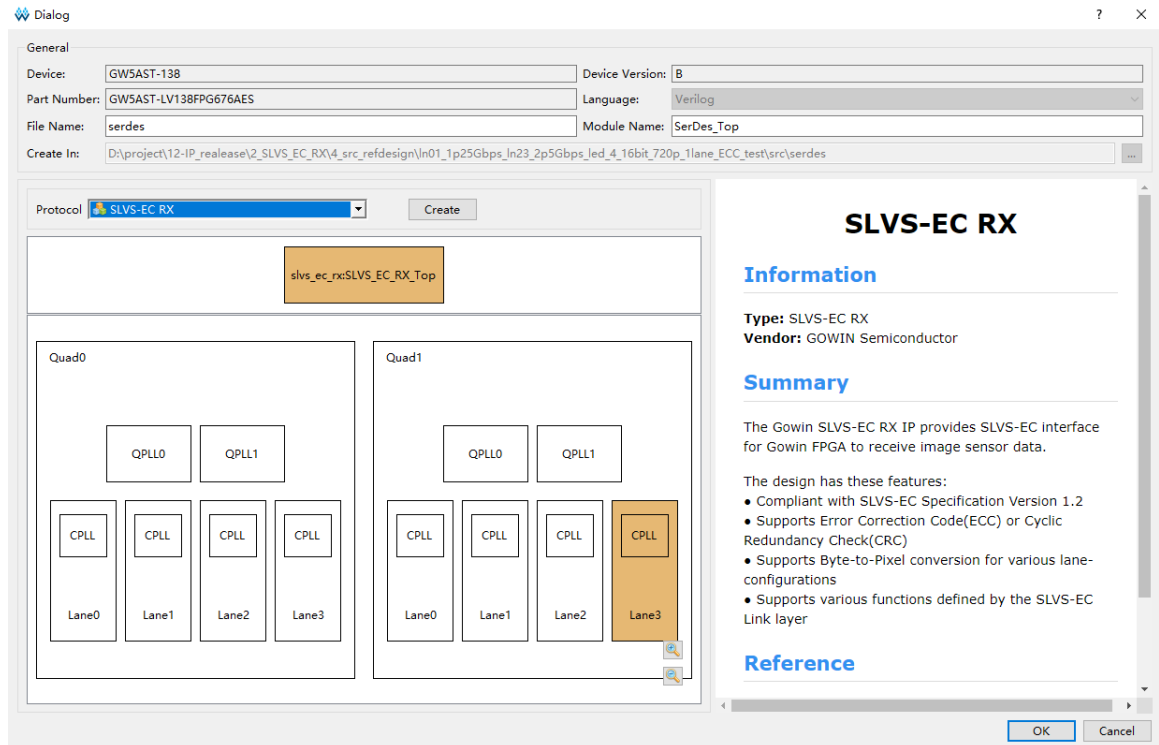
The figure shows the 'Channel Bonding' tab of the configuration window. It contains the following settings:

- RX Channel Bonding:**
 - Channel Bonding:** A dropdown menu set to 'Four Words'.
 - Master Channel Selection:** A dropdown menu set to 'Q1 Lane3'.
 - Pattern 0:** A text box containing 'BC'. A note to the right says 'Pattern 0 must be K Character'.
 - Pattern 1:** A text box containing 'FB' with a checked checkbox labeled 'K Character'.
 - Pattern 2:** A text box containing '5C' with a checked checkbox labeled 'K Character'.
 - Pattern 3:** A text box containing 'FB' with a checked checkbox labeled 'K Character'.
 - Max Skew:** A dropdown menu set to '8'.
 - Read Start Depth:** A dropdown menu set to '16'.

5. IP Generation

After completing SLVS-EC RX IP configuration, click "OK" button at the bottom right corner of the interface to generate files of the SLVS-EC RX IP, and return to the SerDes IP configuration interface, and then the SerDes IP configuration interface displays the current generated IP and the corresponding Quad, PLL, and Lane usage, as shown in Figure 4-8.

Figure 4-8 SLVS-EC RX IP in SerDes IP Configuration Interface



Then, click "OK" button at the bottom right corner of the interface to generate SerDes IP files and complete the whole IP generation.

5 Reference Design

This chapter is intended to introduce the usage and structure of the reference design for SLVS-EC RX IP. Please see the SLVS-EC RX IP [reference design](#) for details at Gowinsemi website.

This reference design uses the following development board^[1]:

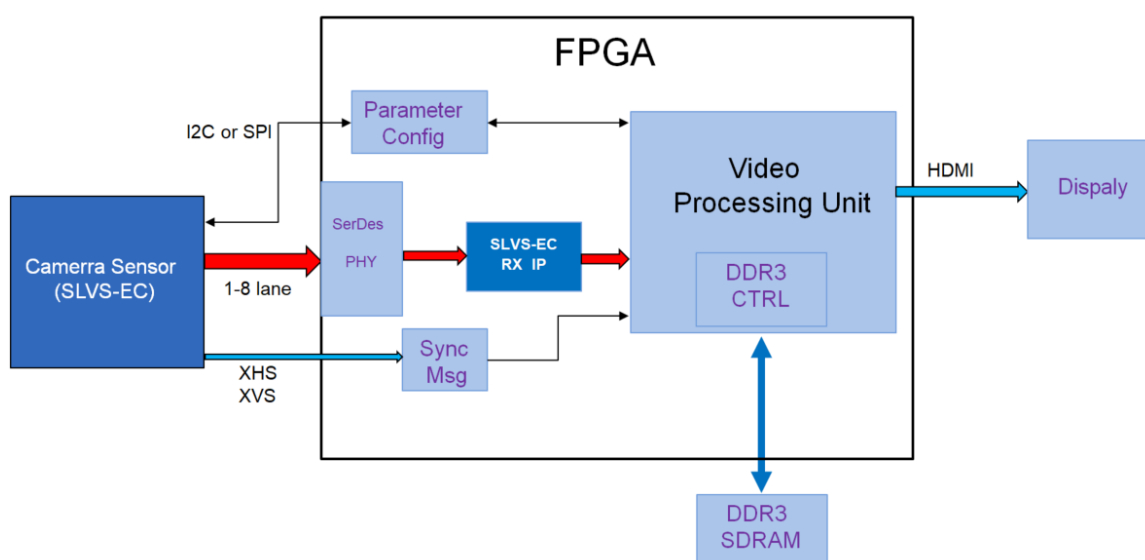
- EVAL_DDR3-PSRAM-SLVS_GW5AT-LV138FPG676_V1.0
- SLVS_EC_IMX421_DaughterCard

Note!

^[1] The development board used in this IP reference design is an internal test board and is not available for sale. It is intended for code verification and design reference only. To evaluate the design on commercially available boards, users need to port the design themselves.

The block diagram of reference design is shown in Figure 5-1.

Figure 5-1 Block Diagram of Reference Design



The reference design adopts the approach that TX and RX are verified independently of each other. The Camera Sensor module is used to generate SLVS-EC protocol video signals, which are input to the IP through the SerDes PHY. After being analyzed and processed, the signals are then

input to the Video Processing Unit. Following frame buffering processing via DDR, they are then output to an HDMI device and ultimately to a display. Camera Sensor registers parameter can be configured through the SPI interface. The Camera Sensor operates in Master mode and outputs XHS and XVS signals.

6 File Delivery

The delivery files for the Gowin SLVS-EC RX IP includes the documents, the design source code, and the reference design.

6.1 Documentation

Table 6-1 Document List

Name	Description
IPUG1176, Gowin SLVS-EC RX IP User Guide	Gowin SLVS-EC RX IP User Guide, namely this one

6.2 Design Source Code (Encryption)

The encrypted code file contains the SLVS-EC RX IP RTL encrypted code which is used for GUI in order to cooperate with Gowin Software to generate the IP core required by users.

Table 6-2 Gowin SLVS-EC RX IP File List

Name	Description
slvs_ec_rx.v	SLVS-EC RX IP file, encrypted.
serdes.v	The top-level file of SerDes-related IP, which provides users with interface information.

6.3 Reference Design

SLVS-EC RX RefDesign folder contains the netlist file, user reference design, constraints file, top-level file, and project file, etc.

Table 6-3 Gowin SLVS-EC RX RefDesign Folder Content List

Name	Description
xxx_top.v	The top module of reference design
xxx.cst	Project physical constraints file
xxx.sdc	Project timing constraints file
serdes	SLVS-EC RX IP folder
i2c_master.v	i2c_master folder, encrypted
gowin_pll.v	gowin_pll folder

