



Gowin MIPI Byte-to-Pixel Converter IP

User Guide

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Revision History

Date	Version	Description
12/07/2023	1.0E	Initial version published.
05/09/2025	1.1E	● Descriptions of o_dt_err, o_wc_err, and o_align_err ports added. ● 1.2 Related Documents updated.

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1 About This Guide

1.1 Purpose

The purpose of Gowin MIPI Byte-to-Pixel Converter IP User Guide is to help users learn the features and usage of Gowin MIPI Byte-to-Pixel Converter IP by providing descriptions of the product overview, functions, GUI, etc.

1.2 Related Documents

1. The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:
 - [IPUG948, Gowin MIPI D-PHY RX TX Advance IP User Guide](#)
 - [DS100, GW1N series of FPGA Products Data Sheet](#)
 - [DS102, GW2A series of FPGA Products Data Sheet](#)
 - [DS226, GW2AR series of FPGA Products Data Sheet](#)
 - [DS961, GW2ANR series of FPGA Products Data Sheet](#)
 - [DS976, GW2AN-55 Data Sheet](#)
 - [DS981, GW5AT series of FPGA Products Data Sheet](#)
 - [DS1103, GW5A series of FPGA Products Data Sheet](#)
 - [DS1239, GW5AST series of FPGA Products Data Sheet](#)
 - [DS1105, GW5AS series of FPGA Products Data Sheet](#)
 - [DS1108, GW5AR series of FPGA Products Data Sheet](#)
 - [DS1118, GW5ART series of FPGA Products Data Sheet](#)

- [SUG100, Gowin Software User Guide](#)
- 2. MIPI Alliance Specification for D-PHY, Version 1.1 November 7, 2011, www.mipi.org
- 3. MIPI Alliance Specification for Display Serial Interface, Version 1.1 November 22, 2011, www.mipi.org
- 4. MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2), Version 1.1, July 18, 2012, www.mipi.org

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
CSI	Camera Serial Interface
CSPS	Chroma Sample Pixel Shifted
DE	Data Enable
DSI	Display Serial Interface
HS	Horizontal Synchronization
IP	Intellectual Property
LUT	Look-up Table
MIPI	Mobile Industry Processor Interface
SSRAM	Shadow SRAM
VS	Vertical Synchronization

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Product Overview

2.1 Introduction

Gowin MIPI Byte-to-Pixel Converter IP is used to convert the parallel payload data from 1~4 lanes output by the MIPI DSI/CSI-2 RX IP into pixel format data. Additionally, it utilizes the packet header information to generate corresponding video synchronization signals such as VS (Vertical Sync), HS (Horizontal Sync), and DE (Data Enable).

Table 2-1 Gowin MIPI Byte-to-Pixel Converter IP Overview

Gowin MIPI Byte-to-Pixel Converter IP	
Logic Resource	See Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9.Beta-3 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features

- Complies with MIPI DSI V1.1 and MIPI CSI-2 V1.1 standards
- Supports RX lanes: 1, 2, 3, or 4
- Supports MIPI RX D-PHY with 1:8 and 1:16 modes
- Supports output of one or two pixels per clock, and some formats support output of four pixels

- Supports three video modes as defined in the MIPI DSI standard
 - Non-Burst Mode with Sync. Pulses
 - Non-Burst Mode with Sync. Events
 - Burst Mode
- The following video formats specified in the MIPI DSI Spec are supported:
 - RGB-888
 - RGB-666
 - RGB-666, loosely packed
 - RGB-565
 - YCbCr-422_24-bit
 - YCbCr-422_16-bit
 - YCbCr-422_20-bit, loosely packed
 - RGB_30-bit
 - RGB_36-bit
- The following video formats specified in the MIPI CSI-2 Spec are supported:
 - RGB-888
 - RGB-666
 - RGB-565
 - RAW-8
 - RAW-10
 - RAW-12
 - RAW-14
 - YUV420 8-bit
 - YUV420 8-bit, CSPS
 - YUV420 10-bit
 - YUV420 10-bit, CSPS
 - YUV422 8-bit
 - YUV422 10-bit

2.3 Resource Utilization

Taking Gowin GW2A-18 series of FPGA as an instance, the resource utilization of Gowin MIPI Byte-to-Pixel Converter IP is as shown in Table 2-2. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades.

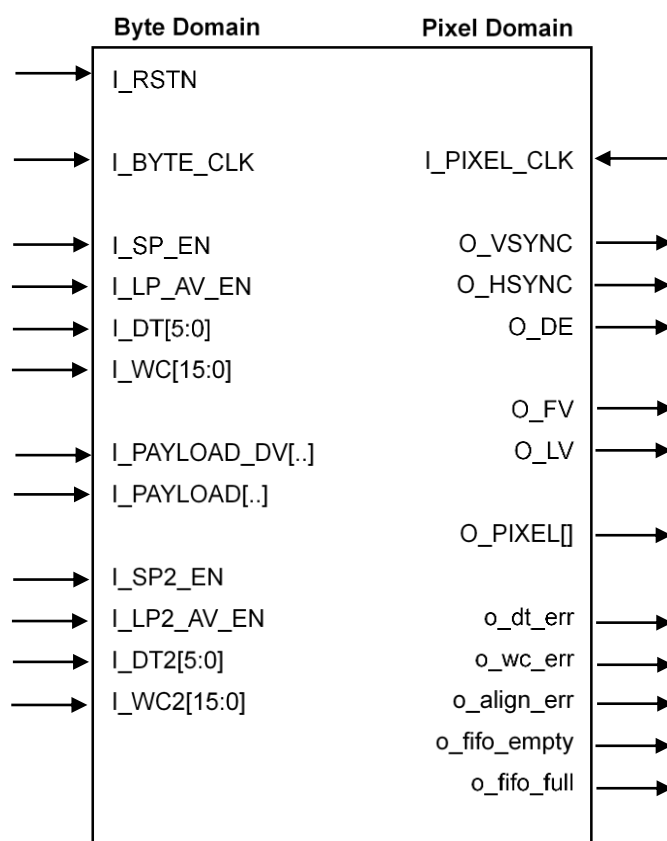
Table 2-2 Resource Utilization (Some Configuration)

Parameter Configuration	Resource Utilization		
	LUT	REG	SSRAM
1:8, 1-Lane,DSI RGB888,1-Pixel Output	223	300	7
1:8, 2-Lane,DSI RGB888,1-Pixel Output	281	328	7
1:8, 3-Lane,DSI RGB888,1-Pixel Output	248	334	7
1:8, 4-Lane,DSI RGB888,1-Pixel Output	383	485	13
1:8, 4-Lane,DSI RGB888,2-Pixel Output	353	501	13
1:16, 1-Lane,DSI RGB888,1-Pixel Output	281	328	7
1:16, 2-Lane,DSI RGB888,1-Pixel Output	383	485	13
1:16, 3-Lane,DSI RGB888,1-Pixel Output	361	502	13
1:16, 4-Lane,DSI RGB888,1-Pixel Output	649	688	19
1:16, 4-Lane,DSI RGB888,2-Pixel Output	543	805	25
1:8, 4-Lane,DSI 36-bit RGB,1-Pixel Output	452	593	19
1:16, 4-Lane,DSI 36-bit RGB,1-Pixel Output	635	698	19
1:8, 4-Lane,CSI-2 RAW10,2-Pixel Output	362	445	11
1:16, 4-Lane,CSI-2 RAW10,2-Pixel Output	658	712	21
1:8, 4-Lane,CSI-2 RAW12,2-Pixel Output	391	481	13
1:16, 4-Lane,CSI-2 RAW12,2-Pixel Output	637	684	19
1:8, 4-Lane,CSI-2 RAW14,2-Pixel Output	397	517	15
1:16, 4-Lane,CSI-2 RAW14,2-Pixel Output	803	848	29

3 Functional Description

3.1 Top Block Diagram

Figure 3-1 Gowin MIPI Byte-to-Pixel Converter IP Overview



The primary function of Gowin MIPI Byte-to-Pixel Converter IP is to convert the payload data packets of MIPI DSI or CSI-2 video into standard pixel format data, and recover video synchronization signals from sync short packets. The input ports of the IP include the control signals (packet headers) and payload data parsed from the D-PHY byte data by Gowin MIPI DSI/CSI-2 RX IP. In the 1:16 data mode with 3-Lane or 4-Lane, two

sets of packet headers may be received and parsed simultaneously in a single clock cycle. Therefore, the input ports also include the second set of control signals.

3.2 Port Description

Table 3-1 Port List of Byte-to-Pixel Converter IP

Signal	I/O	Description
Clock and reset		
I_RSTN	Input	Asynchronous reset signal, active-low
I_BYTE_CLK	Input	Byte domain clock for input side
I_PIXEL_CLK	Input	Pixel domain clock for output side
Input signals for I_BYTE_CLK domain		
I_SP_EN	Input	Short packet valid indicator, active-high
I_LP_AV_EN	Input	Long packet valid indicator, active-high
I_DT[5:0]	Input	Data type in the packet header
I_WC[15:0]	Input	Word count in the packet header
I_PAYLOAD[..]	Input	The payload data, and the bit width depends on the lanes and data modes (1:8/1:16)
		Number of lanes Data Mode Data Width
		1 1:8 8
		2 1:8 16
		3 1:8 24
		4 1:8 32
		1 01:16 16
		2 01:16 32
		3 01:16 48
		4 01:16 64
I_PAYLOAD_DV[..]	Input	The payload data byte valid indicator, active-high; each 8 bits in I_PAYLOAD[..] correspond to 1 bit in I_PAYLOAD_DV[..]
I_SP2_EN	Input	For the 1:16, 3-/4-Lane configuration, it is the second set of short packet valid indicator, active-high
I_LP2_AV_EN	Input	For the 1:16, 3-/4-Lane configuration, it is the second set of long packet valid indicator, active-high
I_DT2[5:0]	Input	For the 1:16, 3-/4-Lane configuration, it is the data

Signal	I/O	Description
		type in the second set of packet header
I_WC2[15:0]	Input	For the 1:16, 3-/4-Lane configuration, it is the word count in the second set of packet header
Output signals for I_PIXEL_CLK domain		
O_VSYNC ^[1]	Output	Field synchronization signal in DSI, active-high
O_HSYNC ^[1]	Output	Line synchronization signal in DSI, active-high
O_DE ^[1]	Output	Data enable signal in DSI, active-high
O_FV ^[2]	Output	Frame valid signal in CSI-2, active-high
O_LV ^[2]	Output	Line valid signal (also serves as data enable) in CSI-2, active-high
O_PIXEL[]	Output	Pixel data input, and possible bit widths include 8 (8-bit pixel), 10 (10-bit pixel), 12 (12-bit pixel), 16 (16-bit pixel / 8-bit pixel x2), 18 (18-bit pixel), 20 (10-bit pixel x2), 24 (24-bit pixel / 12-bit pixel x2), 28 (14-bit pixel x2), 30 (30-bit pixel), 32 (16-bit pixel x2), 36 (36-bit pixel / 18-bit pixel x2), 48 (24-bit pixel x2), 72 (36-bit pixel x2) It is not limited to the above values, depending on the specific configuration.
Other test signals (ports available when enabled)		
o_dt_err	Output	Data Type mismatch flag, active-high (I_BYTE_CLK domain); it indicates that the Data Type specified during IP generation does not match the input long packet I_DT/I_DT2.
o_wc_err	Output	Word Count mismatch flag, active-high (I_BYTE_CLK domain); it indicates that the Word Count calculated based on I_PAYLOAD_DV[..] does not match the input I_WC/I_WC2.
o_align_err	Output	Pixel misalignment flag, active-high (I_BYTE_CLK domain); for details, see 3.6 Number of Pixels and Bytes .

Signal	I/O	Description
o_fifo_full	Output	Internal buffer full Indicator, active-high (I_BYTE_CLK domain).
o_fifo_empty	Output	Internal buffer empty indicator, active-high (I_PIXEL_CLK domain).

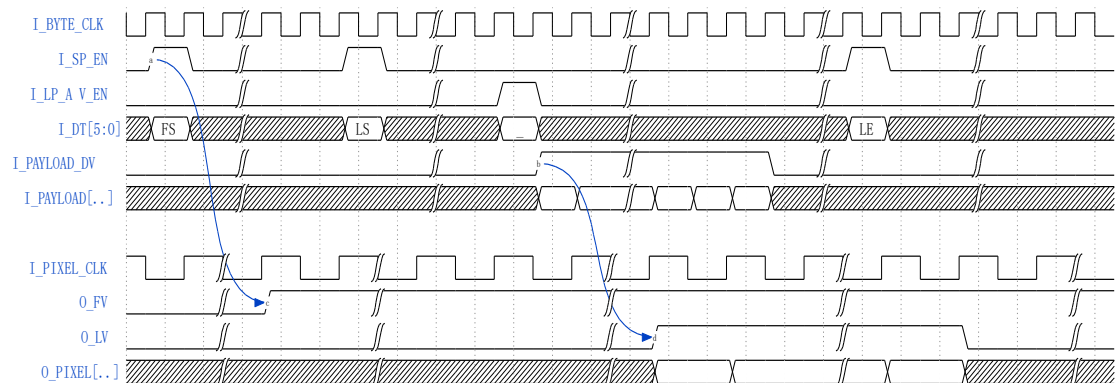
Note!

[1] It is available when "MIPI Interface Type" is DSI.

[2] It is available when "MIPI Interface Type" is CSI-2.

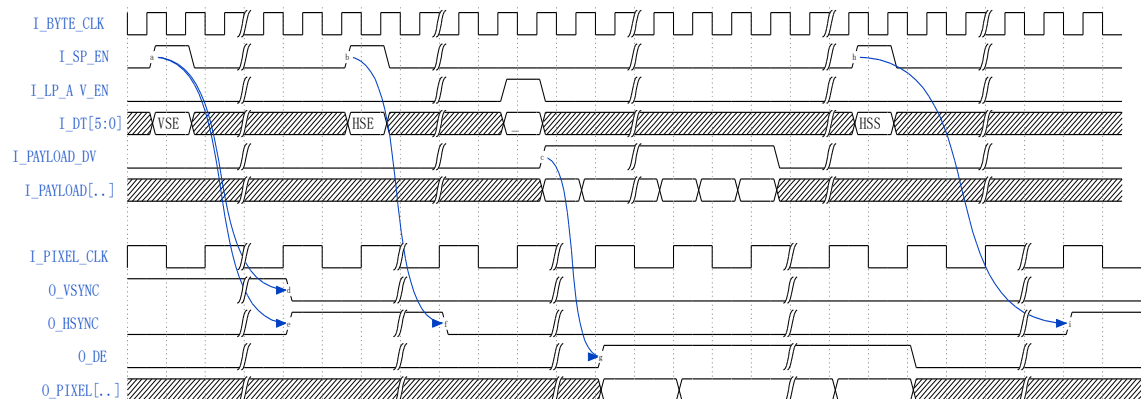
3.3 Timing Description

Figure 3-2 Output and Input Timing in CSI-2 Mode

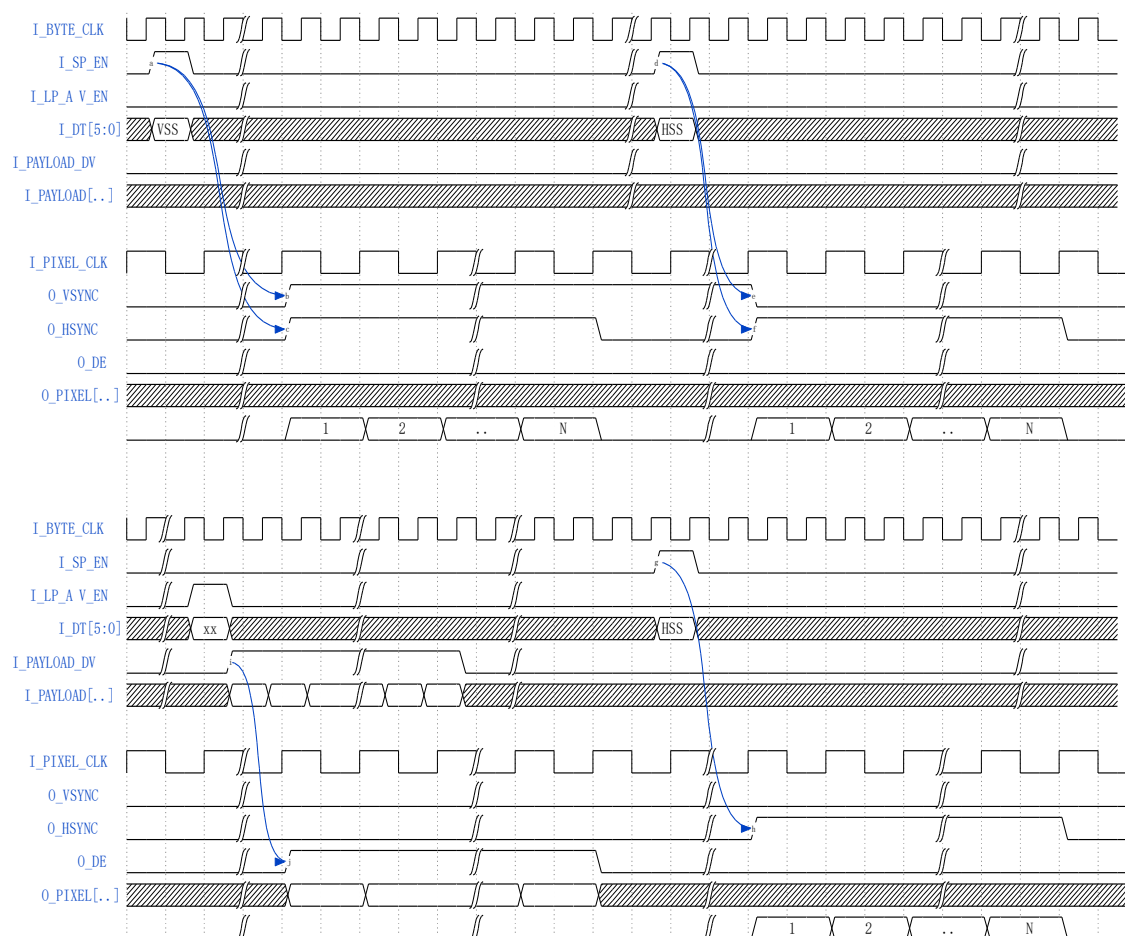
**Note!**

FS: Frame Start, LS: Line Start, LE: Line End.

Figure 3-3 Output and Input Timing in DSI Non-burst mode with Sync Pulse

**Note!**

VSE: VSYNC End, HSE: HSYNC End, HSS: HSYNC Start

Figure 3-4 Output and Input Timing in Burst Mode**Note!**

VSS: VSYNC Start, HSS: HSYNC Start.

The timing for Non-burst Mode with Sync Events is similar to that of Burst Mode.

3.4 Data Type

Table 3-2 and Table 3-3 list the data types supported by Gowin MIPI Byte-to-Pixel Converter IP, and the corresponding bits per pixel. The bits per pixel in the tables follow the definitions in the MIPI DSI Spec and MIPI CSI-2 Spec. Note that the definition of the bits per pixel of YCbCr type in MIPI DSI Spec is different from the YUV type in MIPI CSI-2 Spec.

Table 3-2 DSI Data Type

Data Type	Pixel Format	Bits per Pixel
0x3E	RGB-888	24
0x2E	RGB-666, Loosely packed	24
0x1E	RGB-666	18
0x0E	RGB-565	16

Data Type	Pixel Format	Bits per Pixel
0x2C	YCbCr-422_16bit	16
0x0C	YCbCr-422_20bit, Loosely packed	24
0x1C	YCbCr-422_24bit	24
0x1D	RGB_36bit	36
0x0D	RGB_30bit	30

Table 3-3 CSI-2 Data Type

Data Type	Pixel Format	Bits per Pixel
0x24	RGB-888	24
0x23	RGB-666	18
0x22	RGB-565	16
0x2A	RAW-8	8
0x2B	RAW-10	10
0x2C	RAW-12	12
0x2D	RAW-14	14
0x18	YUV-420_8bit	8
0x19	YUV-420_10bit	10
0x1A	YUV-420_8bit, Legacy	8
0x1C	YUV-420_8bit, CSPS	8
0x1D	YUV-420_10bit, CSPS	10
0x1E	YUV-422_8bit	8
0x1F	YUV-422_10bit	10

3.5 Pixel Organization

Table 3-4 Pixel Organization List

Pixel Format	Pixel Organization List		
DSI/CSI-2 RGB-888	O_PIXEL[23:15]	O_PIXEL[16:8]	O_PIXEL[7:0]
	B	G	R
DSI/CSI-2 RGB-666	O_PIXEL[17:12]	O_PIXEL[11:6]	O_PIXEL[5:0]
	B	G	R
DSI/CSI-2 RGB-565	O_PIXEL[15:11]	O_PIXEL[10:5]	O_PIXEL[4:0]
	B	G	R
DSI YCbCr-	O_PIXEL[23:12]	O_PIXEL[11:0]	

Pixel Format	Pixel Organization List			
422_24bit	Y		Cb	
	Y		Cr	
DSI YCbCr-422_16bit	O_PIXEL[16:8]		O_PIXEL[7:0]	
	Y		Cb	
	Y		Cr	
DSI RGB_36bit	O_PIXEL[35:24]	O_PIXEL[23:12]		O_PIXEL[11:0]
	B	G		R
DSI RGB_30bit	O_PIXEL[29:20]	O_PIXEL[19:10]		O_PIXEL[9:0]
	B	G		R
CSI-2 YUV-422_8bit/ CSI-2 YUV-422_10bit	O_PIXEL[..]4n	O_PIXEL[..]4n+1	O_PIXEL[..]4n+2	O_PIXEL[..]4n+3
	U	Y	V	Y
CSI-2 YUV-420_8bit/ CSI-2 YUV-420_10bit	Even Lines			
	O_PIXEL[..]4n	O_PIXEL[..]4n+1	O_PIXEL[..]4n+2	O_PIXEL[..]4n+3
	U	Y	V	Y
	Odd Lines			
	O_PIXEL[..]4n	O_PIXEL[..]4n+1	O_PIXEL[..]4n+2	O_PIXEL[..]4n+3
	Y	Y	Y	Y
CSI-2 YUV-420_8bit, Legacy	Even Lines			
	O_PIXEL[..]4n	O_PIXEL[..]4n+1	O_PIXEL[..]4n+2	O_PIXEL[..]4n+3
	V	Y	V	Y
	Odd Lines			
	O_PIXEL[..]4n	O_PIXEL[..]4n+1	O_PIXEL[..]4n+2	O_PIXEL[..]4n+3
	U	Y	U	Y

3.6 Number of Pixels and Bytes

In the MIPI D-PHY standard, the data length is measured in terms of the number of bytes, and the data width of the output pixel format is not necessarily a multiple of 8 bits (byte width). The number of pixels per line needs to be restricted to ensure the correct separation of pixel data from MIPI DSI/CSI-2 data packets.

For example, in the case of DSI's RGB-666 format, the number of pixels per line must be a multiple of 4, and each set of 4 pixels occupies 9 bytes, with the total number of bytes per line being a multiple of 9.

Table 3-5 lists various supported pixel formats and the corresponding

requirements for the number of pixels per line and the number of bytes. The pixel count is calculated based on the bits per pixel described in the [3.4 Data Type](#), and it is not the actual number of pixels.

Table 3-5 Pixel and Byte Count Limitations

Pixel Format	Pixel Count	Byte Count
DSI/CSI-2 RGB-888	Multiples of 1	Multiples of 3
DSI/CSI-2 RGB-666	Multiples of 4	Multiples of 9
DSI RGB-666, Loosely packed	Multiples of 1	Multiples of 3
DSI/CSI-2 RGB-565	Multiples of 1	Multiples of 2
DSI YCbCr-422_16bit	Multiples of 2	Multiples of 4
DSI YCbCr-422_20bit, Loosely packed	Multiples of 2	Multiples of 6
DSI YCbCr-422_24bit	Multiples of 2	Multiples of 6
DSI RGB_36-bit	Multiples of 4	Multiples of 18
DSI RGB_30-bit	Multiples of 4	Multiples of 15
CSI-2 RAW-8	Multiples of 1	Multiples of 1
CSI-2 RAW-10	Multiples of 4	Multiples of 5
CSI-2 RAW-12	Multiples of 4	Multiples of 6
CSI-2 RAW-14	Multiples of 4	Multiples of 7
CSI-2 YUV-420_8bit (odd line)	Multiples of 2	Multiples of 2
CSI-2 YUV-420_8bit (even line)	Multiples of 4	Multiples of 4
CSI-2 YUV-422_8bit	Multiples of 4	Multiples of 4
CSI-2 YUV-420_10bit (odd line)	Multiples of 4	Multiples of 5
CSI-2 YUV-420_10bit (even line)	Multiples of 8	Multiples of 10
CSI-2 YUV-422_10bit	Multiples of 4	Multiples of 5

If configured to output 2 pixels per clock, the number of pixels per line must be a multiple of 2; if configured to output 4 pixels per clock, the number of pixels per line must be a multiple of 4.

3.7 Clock Calculation

Gowin MIPI Byte-to-Pixel Converter IP includes two digital logic blocks with asynchronous clock domains. One is the byte clock domain on the input side with the clock signal I_BYTE_CLK. The other is the pixel clock domain on the output side with the clock signal I_PIXEL_CLK. These two clock domains are isolated from each other through an FIFO. The width of the FIFO is greater than or equal to the input signal I_PAYLOAD

bit width and greater than or equal to the output signal O_PIXEL bit width. The depth of the FIFO is just enough for clock domain conversion. To ensure continuous and error-free output pixel, I_BYTE_CLK and I_PIXEL_CLK must satisfy the following relationship:

$$\frac{f_{I_BYTE_CLK}}{f_{I_PIXEL_CLK}} = \frac{\text{Bits per Pixel} \times \text{Pixels per clock}}{D\text{-PHY lanes} \times \text{RX data mode}}$$

Where the RX data width is 8 for 8:1 mode and 16 for 16:1 mode.

For example:

For DSI, RGB-888, 4-Lane, 1:16, with 1 pixel (unit) per clock, the relationship is satisfied as follows:

$$\frac{f_{I_BYTE_CLK}}{f_{I_PIXEL_CLK}} = \frac{24 \times 1}{4 \times 16} = \frac{3}{8}$$

For CSI-2, RAW-14, 2-Lane, 1:8, with 2 pixels (unit) per clock, the relationship is satisfied as follows:

$$\frac{f_{I_BYTE_CLK}}{f_{I_PIXEL_CLK}} = \frac{14 \times 2}{2 \times 8} = \frac{7}{4}$$

3.8 Parameter Configuration

Table 3-6 Parameters of Gowin MIPI Byte-to-Pixel Converter IP

Name	Range	Description
MIPI Interface Type	DSI or CSI-2	Specify MIPI interface type
DSI Video Mode	Non-Burst Mode with Sync Events, Non-Burst Mode with Sync Pulses, Burst Mode	Valid when RX Interface Type is DSI; specify the video synchronization signal mode for the DSI interface.
MIPI D-PHY Mode	1:8 or 1:16	Specify RX D-PHY data mode
Number of RX Lanes	1, 2, 3, or 4	Specify number of RX D-PHY lanes
Number of Pixels Per Clock	1, 2, 4	Specify number of pixels per clock
Data type	See Table 3-3 for CSI-2	Specify the data type to process and determine the Bits per Pixel simultaneously.
Number of HSync Pulses VSync is Active	1, 1023	This parameter is valid when in DSI Non-Burst Mode with Sync Events or DSI Burst Mode. It specifies the number of HSync

Name	Range	Description
		pulses when Vsync is active, i.e., the number of lines occupied by VSync.
Number of Pixel Clock Cycles HSync is Active	2, 1023	This parameter is valid when in DSI Non-Burst Mode with Sync Events or DSI Burst Mode. It specifies the number pixel clock cycles when Hsync is active.
Number of Delayed Pixel Clock Cycles for HSync	0, 255	Number of delayed pixel clock cycles for HSync; When this parameter is set to 0, the rising edge of HS is aligned with the rising edge/falling edge of VS, as shown in Figure 3-3 and Figure 3-4. In certain situations, it may be necessary to delay HS for a certain number of cycles.
Enable Debug Signals	Yes or No	When enabled, the test signals will be brought out.

All data types listed in the Table 3-2 and Table 3-3 support any combination of these three conditions; that is, 1-4 lanes, 1:8/1:16 modes, and output of no more than 2 pixel units per clock. In Table 3-3, the RAW series and YUV series of CSI-2 also support output of 4 pixel units per clock.

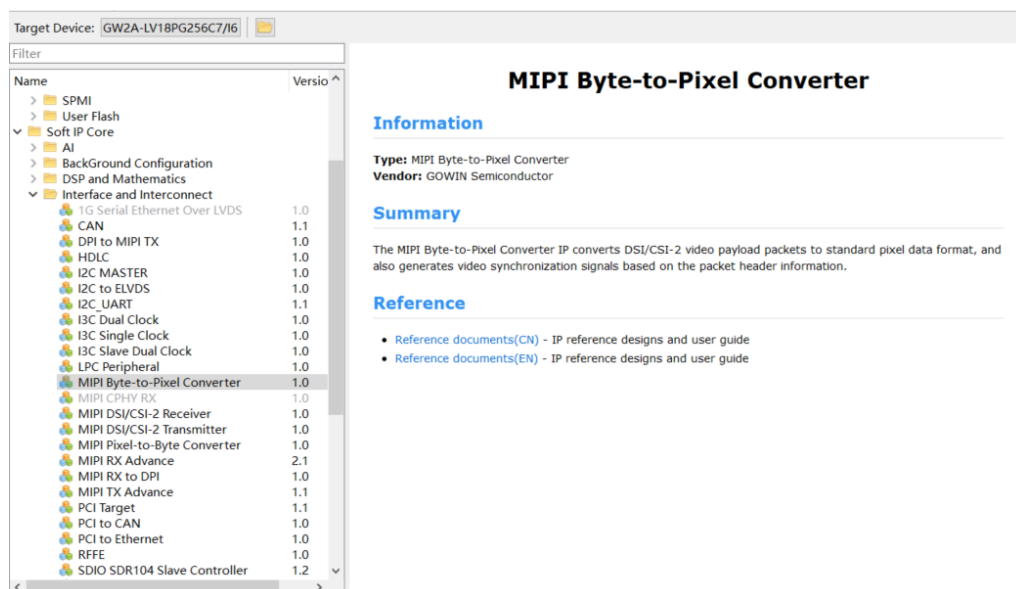
4 Interface Configuration

You can select "Tools" in Gowin Software to start the IP Core Generator to call and configure MIPI Byte-to-Pixel Converter IP.

1. Open IP Core Generator.

After creating the project, click the "Tools" tab in the upper left, click "IP Core Generator" from the drop-down list to open IP Core Generator. Click "Soft IP Core > Interface and Interconnect > MIPI Byte-to-Pixel Converter"; or enter "Byte-to-Pixel" in the "Filter" search box to locate it quickly.

Figure 4-1 IP Core Generator

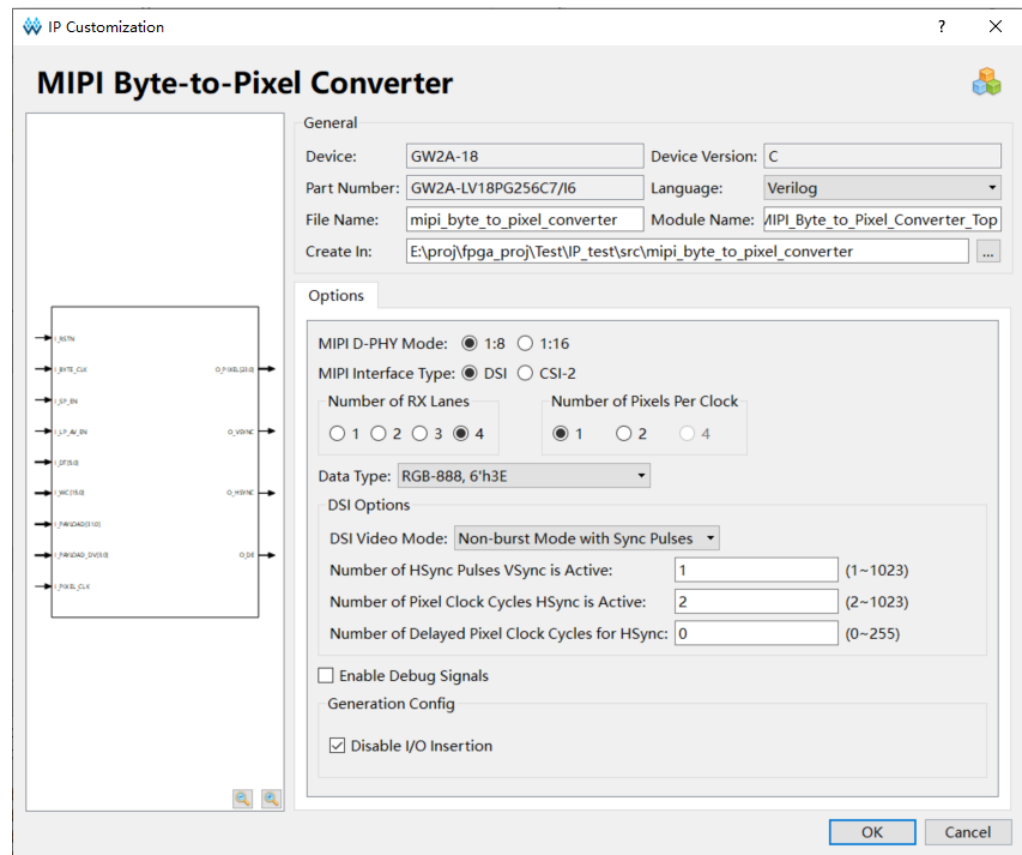


2. MIPI Byte-to-Pixel Converter IP Configuration Interface

Users can open the MIPI Byte-to-Pixel Converter configuration interface by double clicking the "MIPI Byte-to-Pixel Converter IP" item in the "IP Core Generator" tool interface. The port diagram is on the left, and the parameter configuration options (see [3.8 Parameter Configuration](#) for

details) are on the right, as shown in Figure 4-2

Figure 4-2 MIPI Byte-to-Pixel Converter IP Configuration Interface



3. Generation and Instantiation

After configuring the parameters according to requirements, click "OK" to generate MIPI Byte-to-Pixel Converter IP. As shown in Figure 4-3, here is an example of IP instantiation in the user's Verilog program.

Figure 4-3 MIPI Byte-to-Pixel Converter IP Instantiation

