



Gowin MIPI Pixel-to-Byte Converter IP

User Guide

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1 About This Guide

1.1 Purpose

The purpose of Gowin MIPI Pixel-to-Byte Converter User Guide is to help users learn the features and usage of Gowin MIPI Pixel-to-Byte Converter IP by providing descriptions of the product overview, functions, GUI, etc.

1.2 Related Documents

1. The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:
 - [IPUG948, Gowin MIPI D-PHY RX TX Advance IP User Guide](#)
 - [DS100, GW1N series of FPGA Products Data Sheet](#)
 - [DS102, GW2A series of FPGA Products Data Sheet](#)
 - [DS226, GW2AR series of FPGA Products Data Sheet](#)
 - [DS961, GW2ANR series of FPGA Products Data Sheet](#)
 - [DS976, GW2AN-55 Data Sheet](#)
 - [DS981, GW5AT series of FPGA Products Data Sheet](#)
 - [DS1103, GW5A series of FPGA Products Data Sheet](#)
 - [DS1239, GW5AST series of FPGA Products Data Sheet](#)
 - [DS1105, GW5AS series of FPGA Products Data Sheet](#)
 - [DS1108, GW5AR series of FPGA Products Data Sheet](#)
 - [DS1118, GW5ART series of FPGA Products Data Sheet](#)

- [SUG100, Gowin Software User Guide](#)
- 2. MIPI Alliance Specification for D-PHY, Version 1.1 November 7, 2011, www.mipi.org
- 3. MIPI Alliance Specification for Display Serial Interface, Version 1.1 November 22, 2011, www.mipi.org
- 4. MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2), Version 1.1, July 18, 2012, www.mipi.org

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
CSI	Camera Serial Interface
CSPS	Chroma Sample Pixel Shifted
DE	Data Enable
DSI	Display Serial Interface
HS	Horizontal Synchronization
IP	Intellectual Property
LUT	Look-up Table
MIPI	Mobile Industry Processor Interface
SSRAM	Shadow SRAM
VS	Vertical Synchronization

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Product Overview

2.1 Product Overview

MIPI D-PHY is designed to replace traditional parallel video buses based on LVCMOS, LVDS, and the like. However, many processors, displays, or cameras still utilize these traditional interfaces. To connect to MIPI D-PHY TX IP, it is necessary to first convert these traditional parallel video formats into MIPI D-PHY-compatible byte stream formats and then proceed with encapsulation. Gowin MIPI Pixel-to-Byte Converter is precisely designed to convert standard parallel video formats into the required byte stream formats for MIPI DSI or CSI-2.

Table 2-1 Gowin MIPI Pixel-to-Byte Converter Overview

Gowin MIPI Pixel-to-Byte Converter	
Logic Resource	See Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9.Beta-3 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features

- Complies with MIPI DSI V1.1 and MIPI CSI-2 V1.1 standards
- Supports input of one or two pixels per clock, and some formats support input of four pixels

- Supports TX lanes: 1, 2, 3, or 4
- Supports TX D-PHY data mode with 8:1 or 16:1
- The following video formats specified in the MIPI DSI Spec are supported:
 - RGB-888
 - RGB-666
 - RGB-666, loosely packed
 - RGB-565
 - YCbCr-422_24bit
 - YCbCr-422_16bit
 - YCbCr-422_20bit, loosely packed
 - RGB_30bit
 - RGB_36bit
- The following video formats specified in the MIPI CSI-2 Spec are supported:
 - RGB-888
 - RGB-666
 - RGB-565
 - RAW-8
 - RAW-10
 - RAW-12
 - RAW-14
 - YUV420 8 bits
 - YUV420 8 bits, CSPS
 - YUV420 10 bits
 - YUV420 10 bits, CSPS
 - YUV422 8 bits
 - YUV422 10 bits

2.3 Resource Utilization

Taking Gowin GW2A-18 series of FPGA as an instance, the resource utilization of Gowin MIPI Pixel-to-Byte Converter IP is as shown in Table 2-2. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades.

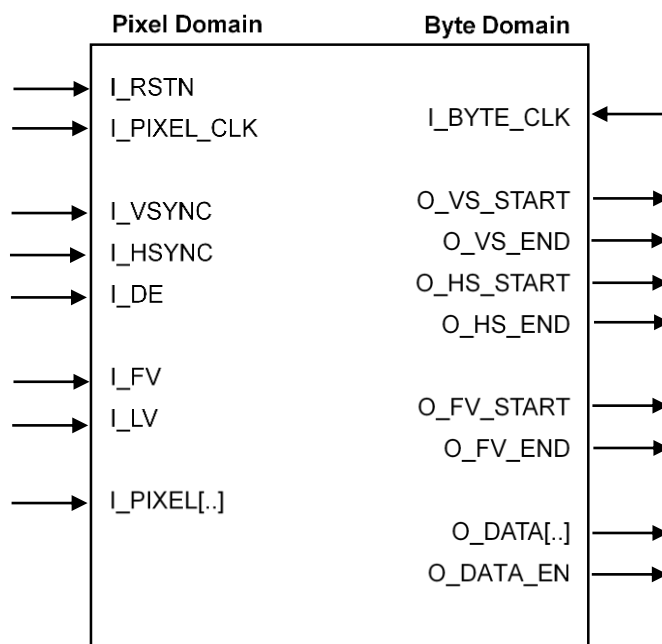
Table 2-2 Resource Utilization (Some Configuration)

Parameter Configuration	Resource Utilization		
	LUT	REG	SSRAM
1:8, 1-Lane,DSI RGB888,1-Pixel Input	219	230	9
1:8, 2-Lane,DSI RGB888,1-Pixel Input	213	238	9
1:8, 3-Lane,DSI RGB888,1-Pixel Input	120	196	7
1:8, 4-Lane,DSI RGB888,1-Pixel Input	190	247	9
1:8, 4-Lane,DSI RGB888,2-Pixel Input	297	367	17
1:16, 1-Lane,DSI RGB888,1-Pixel Input	213	238	9
1:16, 2-Lane,DSI RGB888,1-Pixel Input	190	247	9
1:16, 3-Lane,DSI RGB888,1-Pixel Input	123	294	13
1:16, 4-Lane,DSI RGB888,1-Pixel Input	256	377	17
1:16, 4-Lane,DSI RGB888,2-Pixel Input	256	392	17
1:8, 4-Lane,DSI 36bit RGB,1-Pixel Input	504	371	17
1:16, 4-Lane,DSI 36bit RGB,1-Pixel Input	463	396	17
1:8, 4-Lane,CSI-2 YUV422_10bit,2-Pixel Input	231	242	9
1:8, 4-Lane,CSI-2 YUV422_10bit,4-Pixel Input	355	358	17
1:16, 4-Lane,CSI-2 YUV422_10bit,2-Pixel Input	336	372	17
1:16, 4-Lane,CSI-2 YUV422_10bit,4-Pixel Input	313	383	17
1:8, 4-Lane,CSI-2 RAW14,2-Pixel Input	324	305	9
1:16, 4-Lane,CSI-2 RAW14,2-Pixel Input	479	396	17

3 Functional Description

3.1 Top Block Diagram

Figure 3-1 Top Block Diagram of Pixel-to-Byte Converter IP



Gowin MIPI Pixel-to-Byte Converter IP is precisely designed to convert standard parallel video formats into byte stream formats for MIPI DSI or CSI-2 according to the configuration.

3.2 Port Description

Table 3-1 Port List of Gowin MIPI Pixel-to-Byte Converter IP

Signal	I/O	Description	
Clock and reset			
I_RSTN	Input	Asynchronous reset signal, active-low	
I_PIXEL_CLK	Input	Pixel domain clock for input side	
I_BYTE_CLK	Input	Byte domain clock for output side	
Input signals for I_PIXEL_CLK domain			
I_PIXEL[..]	Input	Pixel data input, with a bit width not exceeding 64. Possible bit widths include: 8 (8-bit pixel), 10 (10-bit pixel), 12 (12-bit pixel), 16 (16-bit pixel / 8-bit pixel x2), 18 (18-bit pixel), 20 (10-bit pixel x2), 24 (24-bit pixel / 12-bit pixel x2), 28 (14-bit pixel x2), 30 (30-bit pixel), 32 (16-bit pixel x2), 36 (36-bit pixel / 18-bit pixel x2), 48 (24-bit pixel x2) It is not limited to the above values, depending on the specific configuration.	
I_DE ^[1]	Input	Parallel video bus data enable signal, configurable polarity	
I_HSYNC ^[1]	Input	Parallel video bus hs sync signal, configurable polarity	
I_VSYNC ^[1]	Input	Parallel video bus vs sync signal, configurable polarity	
I_FV ^[2]	Input	Parallel video bus field valid signal, active-high	
I_LV ^[2]	Input	Parallel video bus line valid signal, active-high	
Output signals for I_BYTE_CLK domain			
O_DATA[..]	Output	The byte data output, and the width is dependent on the lanes (1-4) and data modes (1:8/1:16).	
		<table> <tr> <th>Number of lanes</th><th>Data Mode</th><th>Data Width</th></tr> </table>	Number of lanes
Number of lanes	Data Mode	Data Width	

Signal	I/O	Description		
		1	1:8	8
		2		16
		3		24
		4		32
		1	01:16	16
		2		32
		3		48
		4		64
O_DATA_EN	Output	Byte data valid indicator, active-high		
O_VS_START ^[1]	Output	VS start identifier pulse		
O_VS_END ^[1]	Output	VS end identifier pulse		
O_HS_START ^[1]	Output	HS start identifier pulse		
O_HS_END ^[1]	Output	HS end identifier pulse		
O_FV_START ^[2]	Output	Field valid start identifier pulse		
O_FV_END ^[2]	Output	Field valid end identifier pulse		

Note!

[1] It is available when "MIPI Interface Type" is DSI.

[2] It is available when "MIPI Interface Type" is CSI-2.

3.3 Timing Description

Figure 3-2 Timing Diagram for Parallel Input Interface of a Display (DSI)

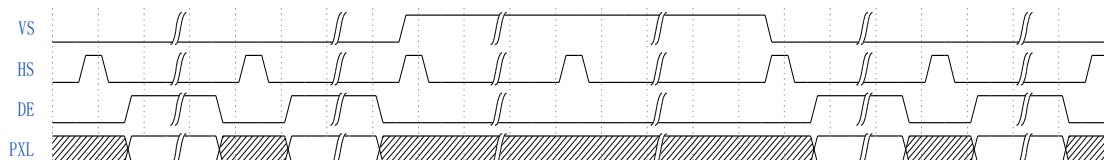


Figure 3-3 Timing Diagram for Parallel Input Interface of a Camera (CSI-2)

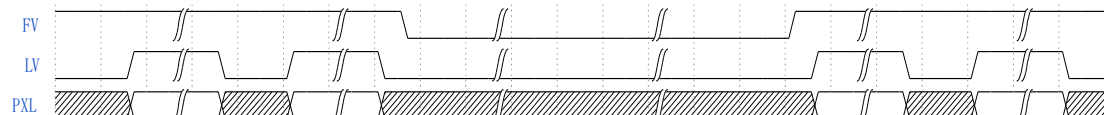
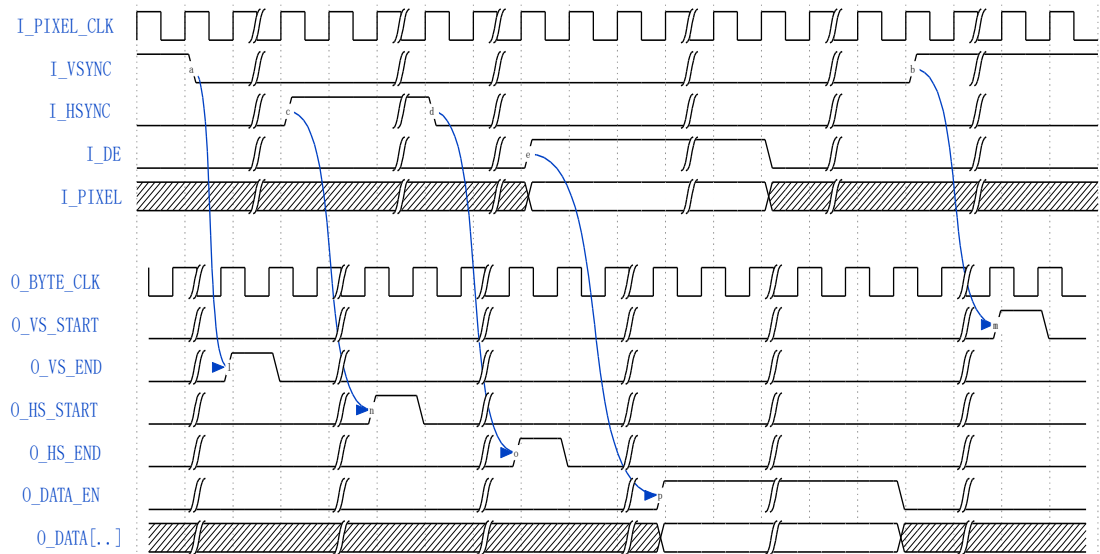


Figure 3-2 and Figure 3-3 show the timing for parallel input interfaces of the display and camera respectively. They follow the MIPI DSI/CSI-2 interface standard; that is, the DSI has VS, HS, and DE signals, and the CSI-2 has FV and LV signals. All these signals are sampled on the rising edge of the pixel clock. The number of pixels per clock is configurable on

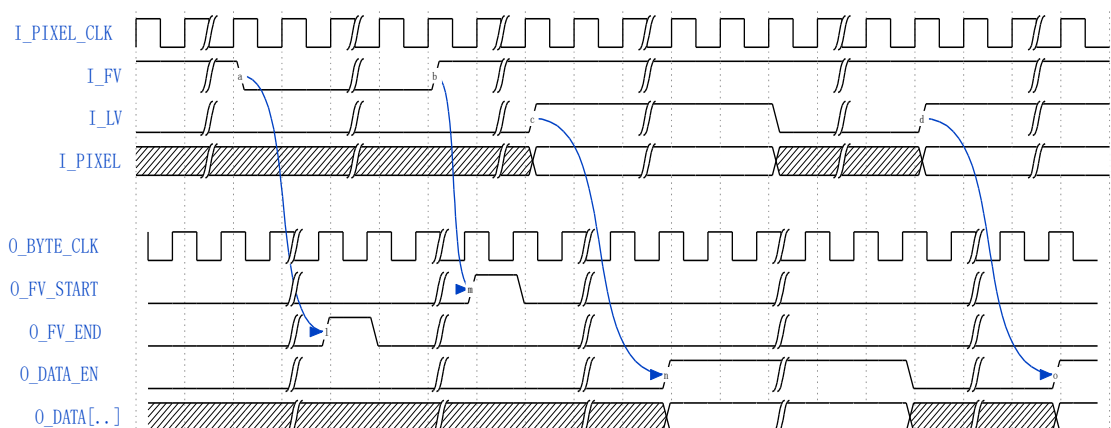
demand.

Figure 3-4 Output and Input Timing in DSI Mode



In DSI mode, when I_VSYNC, I_SYNC and I_DE are configured to be active high, the timing between the input and output is shown in Figure 3-4. Each rising edge of I_VSYNC will generate an O_VS_START pulse signal, and each falling edge will generate an O_VS_END pulse signal. The I_LV signal in CSI-2 mode serves as a valid indicator of the pixel data and is equivalent to the I_DE signal of the DSI, so there are only the start pulse signal O_FV_START and the end pulse signal O_FV_END generated by I_FV. The timing between the input and output for the CSI-2 is shown in Figure 3-5.

Figure 3-5 Output and Input Timing in CSI-2 Mode



3.4 Data Type

Table 3-2 and Table 3-3 list the data types supported by Gowin MIPI Pixel-to-Byte Converter IP, and the corresponding bits per pixel. The bits per pixel in the table follow the definitions in the MIPI DSI Spec and MIPI CSI-2 Spec. Note that the definition of the bits per pixel of YCbCr type in MIPI DSI Spec is different from the YUV type in MIPI CSI-2 Spec.

Table 3-2 DSI Data Type

Data Type	Pixel Format	Bits per Pixel
0x3E	RGB-888	24
0x2E	RGB-666, Loosely packed	24
0x1E	RGB-666	18
0x0E	RGB-565	16
0x2C	YCbCr-422_16bit	16
0x0C	YCbCr-422_20bit, Loosely packed	24
0x1C	YCbCr-422_24bit	24
0x1D	RGB_36bit	36
0x0D	RGB_30bit	30

Table 3-3 CSI-2 Data Type

Data Type	Pixel Format	Bits per Pixel
0x24	RGB-888	24
0x23	RGB-666	18
0x22	RGB-565	16
0x2A	RAW-8	8
0x2B	RAW-10	10
0x2C	RAW-12	12
0x2D	RAW-14	14
0x18	YUV-420_8bit	8
0x19	YUV-420_10bit	10
0x1A	YUV-420_8bit, Legacy	8
0x1C	YUV-420_8bit, CSPS	8
0x1D	YUV-420_10bit, CSPS	10
0x1E	YUV-422_8bit	8
0x1F	YUV-422_10bit	10

3.5 Pixel Organization List

Table 3-4 Pixel Organization List

Pixel Format	Pixel Organization List			
DSI/CSI-2 RGB-888	O_PIXEL[23:15]	O_PIXEL[16:8]	O_PIXEL[7:0]	
	B	G	R	
DSI/CSI-2 RGB-666	O_PIXEL[17:12]	O_PIXEL[11:6]	O_PIXEL[5:0]	
	B	G	R	
DSI/CSI-2 RGB-565	O_PIXEL[15:11]	O_PIXEL[10:5]	O_PIXEL[4:0]	
	B	G	R	
DSI YCbCr- 422_24bit	O_PIXEL[23:12] _{2n}	O_PIXEL[11:0] _{2n}	O_PIXEL[23:12] _{2n+1}	O_PIXEL[11:0] _{2n+1}
	Y	Cb	Y	Cb
DSI YCbCr- 422_16bit	O_PIXEL[16:8] _{2n}	O_PIXEL[7:0] _{2n}	O_PIXEL[16:8] _{2n+1}	O_PIXEL[7:0] _{2n+1}
	Y	Cb	Y	Cb
DSI RGB_36bit	O_PIXEL[35:24]	O_PIXEL[23:12]	O_PIXEL[11:0]	
	B	G	R	
DSI RGB_30bit	O_PIXEL[29:20]	O_PIXEL[19:10]	O_PIXEL[9:0]	
	B	G	R	
CSI-2 YUV- 422_8bit	O_PIXEL[7:0] _{4n}	O_PIXEL[7:0] _{4n+1}	O_PIXEL[7:0] _{4n+2}	O_PIXEL[7:0] _{4n+3}
	U	Y	V	Y
CSI-2 YUV- 422_10bit	O_PIXEL[9:0] _{4n}	O_PIXEL[9:0] _{4n+1}	O_PIXEL[9:0] _{4n+2}	O_PIXEL[9:0] _{4n+3}
	U	Y	V	Y
CSI-2 YUV- 420_8bit	Even Lines			
	O_PIXEL[7:0] _{4n}	O_PIXEL[7:0] _{4n+1}	O_PIXEL[7:0] _{4n+2}	O_PIXEL[7:0] _{4n+3}
	U	Y	V	Y
	Odd Lines			
	O_PIXEL[7:0] _{4n}	O_PIXEL[7:0] _{4n+1}	O_PIXEL[7:0] _{4n+2}	O_PIXEL[7:0] _{4n+3}
	Y	Y	Y	Y
CSI-2 YUV- 420_10bit	Even Lines			
	O_PIXEL[9:0] _{4n}	O_PIXEL[9:0] _{4n+1}	O_PIXEL[9:0] _{4n+2}	O_PIXEL[9:0] _{4n+3}
	U	Y	V	Y
	Odd Lines			
	O_PIXEL[9:0] _{4n}	O_PIXEL[9:0] _{4n+1}	O_PIXEL[9:0] _{4n+2}	O_PIXEL[9:0] _{4n+3}
	Y	Y	Y	Y

Pixel Format	Pixel Organization List			
CSI-2 YUV-420_8bit, Legacy	Even Lines			
	O_PIXEL[7:0] _{4n}	O_PIXEL[7:0] _{4n+1}	O_PIXEL[7:0] _{4n+2}	O_PIXEL[7:0] _{4n+3}
	V	Y	V	Y
	Odd Lines			
	O_PIXEL[7:0] _{4n}	O_PIXEL[7:0] _{4n+1}	O_PIXEL[7:0] _{4n+2}	O_PIXEL[7:0] _{4n+3}
	U	Y	U	Y

3.6 Number of Pixels and Bytes

In the MIPI D-PHY standard, the data length is measured in terms of the number of bytes, and the data width of the input pixel format is not necessarily a multiple of 8 bits (byte width). Therefore, there needs to be a certain limitation on the number of pixels per line to ensure proper encapsulation into MIPI DSI/CSI-2 data packets.

For example, in the case of DSI's RGB-666 format, the number of pixels per line must be a multiple of 4, and each set of 4 pixels occupies 9 bytes, with the total number of bytes per line being a multiple of 9.

Table 3-5 lists various supported pixel formats and the corresponding requirements for the number of pixels per line and the number of bytes. The pixel count is calculated based on the bits per pixel described in the [3.4 Data Type](#), and it is not the actual number of pixels.

Table 3-5 Pixel and Byte Count Limitations

Pixel Format	Pixel Count	Byte Count
DSI/CSI-2 RGB-888	Multiples of 1	Multiples of 3
DSI/ CSI-2/ RGB-666	Multiples of 4	Multiples of 9
DSI RGB-666, Loosely packed	Multiples of 1	Multiples of 3
DSI/ CSI-2/ RGB-565	Multiples of 1	Multiples of 2
DSI YCbCr-422_16bit	Multiples of 2	Multiples of 4
DSI YCbCr-422_20bit, Loosely packed	Multiples of 2	Multiples of 6
DSI YCbCr-422_24bit	Multiples of 2	Multiples of 6
DSI RGB_36-bit	Multiples of 4	Multiples of 18
DSI RGB_30-bit	Multiples of 4	Multiples of 15
CSI-2 RAW-8	Multiples of 1	Multiples of 1
CSI-2 RAW-10	Multiples of 4	Multiples of 5
CSI-2 RAW-12	Multiples of 4	Multiples of 6
CSI-2 RAW-14	Multiples of 4	Multiples of 7

Pixel Format	Pixel Count	Byte Count
CSI-2 YUV-420_8bit (odd line)	Multiples of 2	Multiples of 2
CSI-2 YUV-420_8bit (even line)	Multiples of 4	Multiples of 4
CSI-2 YUV-422_8bit	Multiples of 4	Multiples of 4
CSI-2 YUV-420_10bit (odd line)	Multiples of 4	Multiples of 5
CSI-2 YUV-420_10bit (even line)	Multiples of 8	Multiples of 10
CSI-2 YUV-422_10bit	Multiples of 4	Multiples of 5

If configured to input 2 pixels per clock, the number of pixels per line must be a multiple of 2; if configured to input 4 pixels per clock, the number of pixels per line must be a multiple of 4.

3.7 Clock Calculation

Gowin MIPI Pixel-to-Byte Converter IP includes two digital logic blocks with asynchronous clock domains. One is the pixel clock domain on the input side with the clock signal I_PIXEL_CLK. The other is the byte clock domain on the output side with the clock signal I_BYTE_CLK. These two clock domains are isolated from each other through a FIFO. The width of the FIFO is greater than or equal to the input signal I_PIXEL bit width and greater than or equal to the output signal O_DATA bit width. The depth of the FIFO is just enough for clock domain conversion. To ensure continuous and error-free output data, I_BYTE_CLK and I_PIXEL_CLK must satisfy the following relationship:

$$\frac{f_{I_BYTE_CLK}}{f_{I_PIXEL_CLK}} = \frac{\text{Bits per Pixel} \times \text{Pixels per clock}}{D\text{-PHY lanes} \times \text{TX data mode}}$$

Where the TX data width is 8 for 8:1 mode and 16 for 16:1 mode.

For example:

For DSI, RGB-888, 4-Lane, 1:16, with 1 pixel (unit) per clock, the relationship is satisfied as follows:

$$\frac{f_{I_BYTE_CLK}}{f_{I_PIXEL_CLK}} = \frac{24 \times 1}{4 \times 16} = \frac{3}{8}$$

For CSI-2, RAW-14, 2-Lane, 1:8, with 2 pixels (unit) per clock, the relationship is satisfied as follows:

$$\frac{f_{I_BYTE_CLK}}{f_{I_PIXEL_CLK}} = \frac{14 \times 2}{2 \times 8} = \frac{7}{4}$$

3.8 Parameter Configuration

Table 3-6 Parameters of Gowin MIPI Pixel-to-Byte Converter IP

Name	Range	Description
VSynC Polarity	High or Low	Specify I_VSYNC polarity
HSynC Polarity	High or Low	Specify I_HSYNC polarity
DE Polarity	High or Low	Specify I_DE polarity
Data Type	See Table 3-2 for DSI See Table 3-3 for CSI-2	Specify the data type to process and determine the Bits per Pixel simultaneously
MIPI Interface Type	DSI or CSI-2	Specify MIPI interface type
MIPI D-PHY Mode	8:1 or 16:1	Specify TX D-PHY data mode
Number of RX Lanes	1, 2, 3, 4	Specify number of TX D-PHY lanes
Number of Pixels Per Clock	1, 2, 4	Number of pixels per clock
Number of Delayed Clock Cycles for Pulses	0, 1023	Specify the numbers of delayed clock cycles for pulse signals such as O_VS_START, O_HS_START, O_FV_START, O_VS_END, O_VS_END, O_FV_END

In addition to RGB_36bit, all data types listed in the Table 3-2 and Table 3-3 support any combination of these three conditions; that is, 1-4 lanes, 1:8/1:16 modes, and input of 1 or 2 pixel units per clock. RGB_36bit only supports input of 1 pixel per clock. In Table 3-3, the RAW series and YUV series of CSI-2 also support input of 4 pixels per clock.

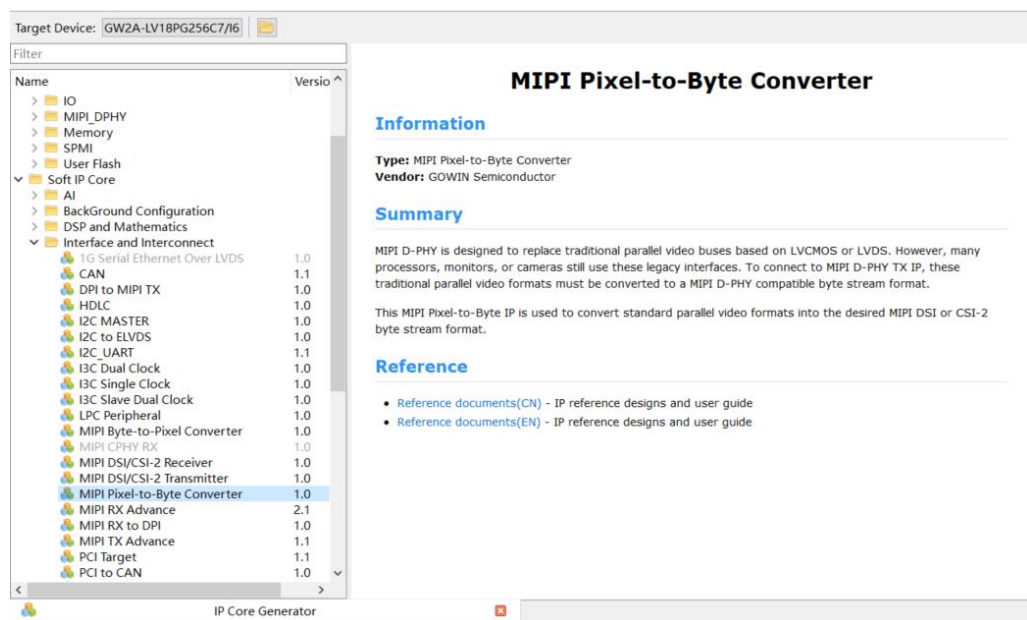
4 Interface Configuration

You can select "Tools" in Gowin Software to start the IP Core Generator to call and configure MIPI Pixel-to-Byte Converter IP.

1. Open IP Core Generator.

After creating the project, click the "Tools" tab in the upper left, click "IP Core Generator" from the drop-down list to open IP Core Generator. Click "Soft IP Core > Interface and Interconnect > MIPI Pixel-to-Byte Converter"; or enter "Pixel-to-Byte" in the "Filter" search box to locate it quickly.

Figure 4-1 IP Core Generator

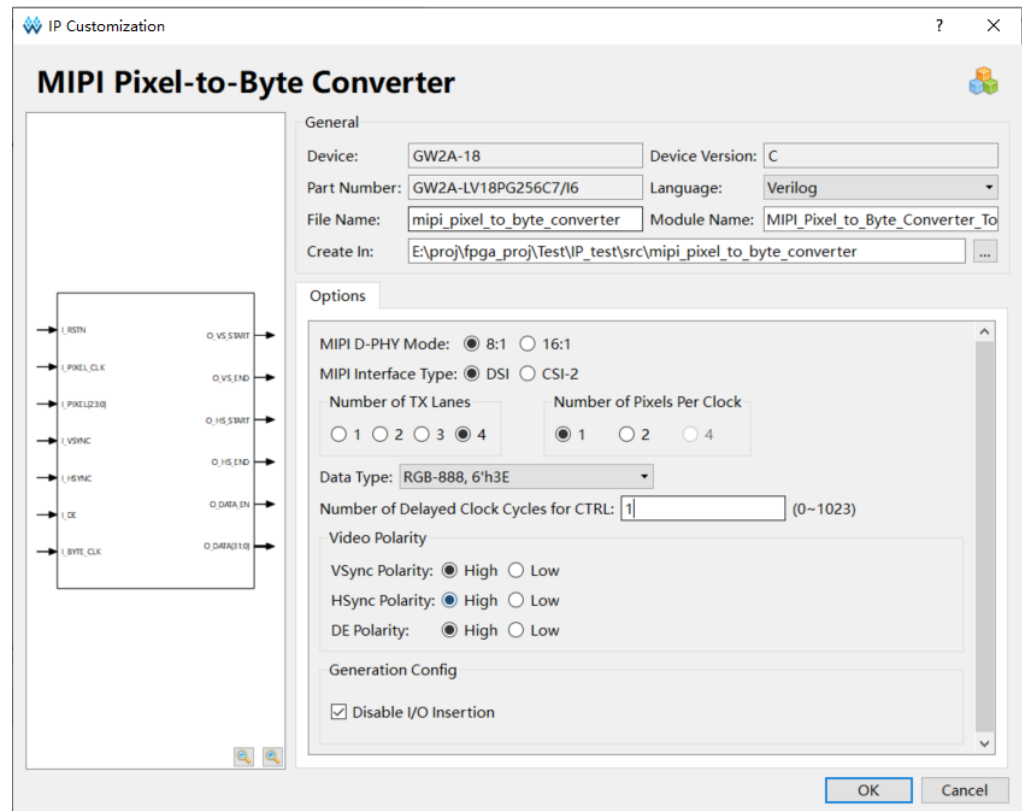


2. MIPI Pixel-to-Byte Converter IP Configuration Interface

Users can open the MIPI Pixel-to-Byte Converter IP configuration interface by double clicking the "MIPI Pixel-to-Byte Converter" item in the "IP Core Generator" tool interface. The port diagram is on the left, and the parameter configuration options (see [3.8 Parameter Configuration](#) for

details) are on the right, as shown in Figure 4-2.

Figure 4-2 MIPI Pixel-to-Byte Converter IP Configuration Interface



3. Generation and Instantiation

After configuring the parameters according to requirements, click "OK" to generate MIPI Pixel-to-Byte Converter IP. As shown in Figure 4-3 MIPI Pixel-to-Byte Converter IP, here is an example of IP instantiation in the user's Verilog program.

Figure 4-3 MIPI Pixel-to-Byte Converter IP Instantiation

