



Gowin Video Frame Buffer with PSRAM IP

User Guide

IPUG752-1.1E, 11/05/2020

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Revision History

Date	Version	Description
09/27/2020	1.0E	Initial version published.
11/05/2020	1.1E	● PSRAM user interface data width updated; ● Table 2-3 added.

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1 About This Guide

1.1 Purpose

The purpose of Gowin Video Frame Buffer with PSRAM IP User Guide is to help users learn the features and usage of this product by providing the description of features, functions, configuration GUI and reference design.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- [DS100](#), GW1N series of FPGA Products Data Sheet
- [DS117](#), GW1NR series of FPGA Products Data Sheet
- [DS821](#), GW1NS series of FPGA Products Data Sheet
- [DS861](#), GW1NSR series of FPGA Products Data Sheet
- [DS881](#), GW1NSER series of FPGA Products Data Sheet
- [DS102](#), GW2A series of FPGA Products Data Sheet
- [DS226](#), GW2AR series of FPGA Products Data Sheet
- [DS961](#), GW2ANR series of FPGA Products Data Sheet
- [SUG100](#), Gowin Software User Guide

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
VESA	Video Electronics Standards Association
VS	Vertical Sync
HS	Horizontal Sync
DE	Data Enable
VFB	Video Frame Buffer

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Overview

Gowin Video Frame Buffer (VFB) IP is used to receive parallel video input data, then cache it to memory, and output parallel video data at the same time, thus realizing the frame cache.

Gowin Video Frame Buffer with PSRAM IP is located between VESA standard video input/output interface and the user interface of PSRAM memory interface IP, so that you can conveniently realize the video frame buffer based on PSRAM memory.

Table 2-1 Gowin Video Frame Buffer with PSRAM IP Overview

Gowin Video Frame Buffer with PSRAM IP	
Supported Devices	GW1N Series GW1NR Series GW1NS Series GW1NSR Series GW1NSER Series GW2A Series GW2AR Series GW2ANR Series
Logic Resource	Please refer to Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software

2.2 Features

- Supports VESA standard interface;
- Supports 16/24/32 bit width;
- Supports Gowin PSRAM Memory Interface IP.

2.3 Resource Utilization

Gowin Video Frame Buffer with PSRAM IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades.

Taking Gowin GW2A-18 FPGA as an instance, the resource utilization is as shown in Table 2-2 and Table 2-3.

Table 2-2 Gowin Video Frame Buffer with PSRAM IP Resource Utilization

Device	GW2A-18	GW2A-18
Video width	16	16
FIFO Depth	1024	2048
LUTs	504(2%)	583(3%)
Registers	408(2%)	430(2%)
BSRAMs	4(8%)	8(17%)

Table 2-3 Number of BSRAM with Different Data Widths and FIFO Depths

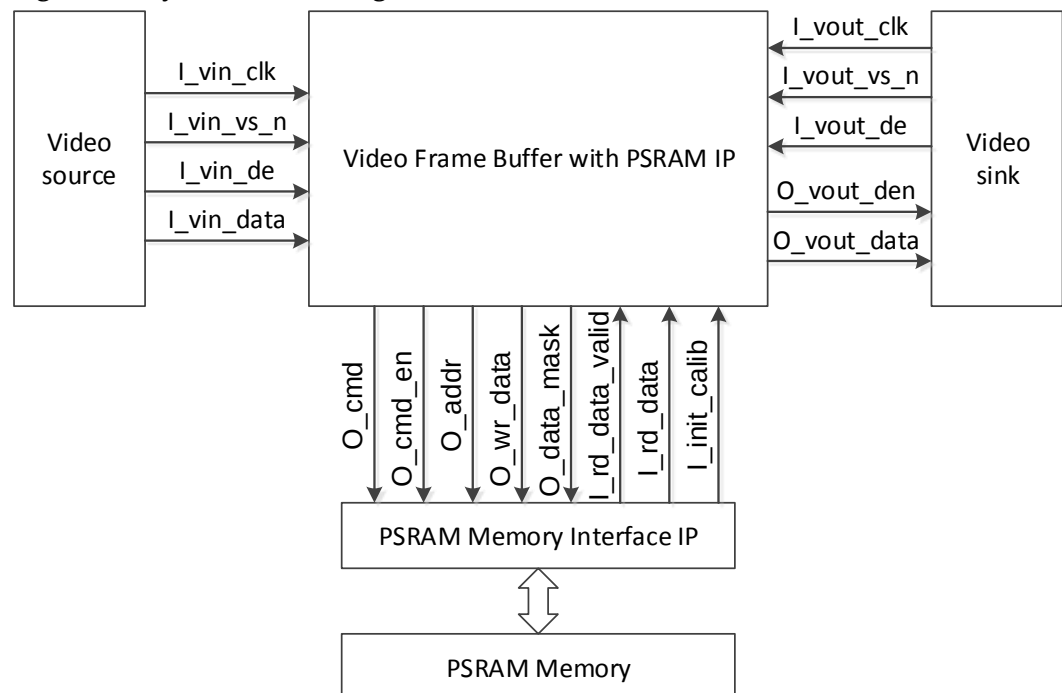
Data Width	Read/Write FIFO Depth	
	1024	2048
32	4	8
64	4	8
128	8	8

3 Functional Description

3.1 System Block Diagram

Gowin Video Frame Buffer with PSRAM IP is used to implement PSRAM-based video input and output frame buffer.

Figure 3-1 System Block Diagram



3.2 Implementation Principle

3.2.1 Circuits

Video frame buffer system includes video source, video sink, video frame buffer with PSRAM, PSRAM memory interface IP and PSRAM memory.

Video Frame Buffer with PSRAM includes four parts: input line buffer control circuit, output line buffer control circuit, base address switching control circuit and arbiter control circuit.

The input line buffer control circuit receives parallel video input data and caches it to the input FIFO line buffer. A PSRAM write request is sent

to the arbitration controller when the data in the FIFO is stored at a preset threshold. When the arbitration controller responds to the request, it starts sending write data, addresses and commands.

The output line buffer control circuit sets a read threshold and transmits a PSRAM read request to the arbiter when the data in the output FIFO line buffer is less than this threshold. When the arbiter responds to the request, the arbiter starts sending read commands and addresses and stores the received data in the output FIFO. When the output FIFO receives the DE signal of the output video, that is, the FIFO read enable signal, the output FIFO outputs the video data.

Three-frame buffer is usually used to avoid image tearing. A three-frame buffer includes one frame in write, one frame in read, and one frame in transition, which can be indicated by read/write pointers, and the read/write pointers respectively point to the start address of the frame buffer, that is, the base address of each frame. The base address switching control circuit is to control the read/write pointers. If you choose not to use three-frame buffer, read and write operations are in the same address space.

The arbiter control circuit is to receive and arbitrate the PSRAM read/write access requests from the input line buffer control circuit and the output line buffer control circuit. At the same time, the data interface of input line buffer control circuit and output line buffer control circuit is connected to the data interface of PSRAM memory interface IP user interface.

3.2.2 Bandwidth Estimation

If the video frame buffer system needs to work normally, the video input/output bandwidth and memory bandwidth must meet certain conditions.

It is assumed that the horizontal resolution of the input video is H_{in} , the vertical resolution is V_{in} , the field frequency is F_{vsin} Hz, and the pixel bit width is N_{in} bit. The horizontal resolution of output video is H_{out} , the vertical resolution is V_{out} , the field frequency is F_{vsout} , and the pixel bit width is N_{out} bit. The PSRAM clock frequency is F_{clk} MHz, the data bit width is D bit. The data is transmitted at rising and falling edges; The efficiency of read/write operations is $e\%$.

The bandwidth estimation method is as follows:

- Video input bandwidth $W_{in} = H_{in} * V_{in} * F_{vsin} * N_{in}$ (bit/s)
- Video output bandwidth $W_{out} = H_{out} * V_{out} * F_{vsout} * N_{out}$ (bit/s)
- Memory theoretical bandwidth $W_{mem} = F_{clk} * D * 2$ (bit/s)
- Memory effective bandwidth $W_{meme} = F_{clk} * D * 2 * e\%$ (bit/s)

Note!

Only when $W_{meme} > (W_{in} + W_{out})$, the video frame buffer system can work normally.

The example is as follows:

Input video format 1280x720@60Hz, pixel format RGB565, pixel bit width 16bit; Output video format 1280x720@60Hz, pixel format RGB565, pixel bit width 16bit; PSRAM clock frequency 166MHz, data bit width 16bit,

read/write operations efficiency 60%.

Note!

The efficiency of read/write operations depends on the bandwidth efficiency of PSRAM and video bandwidth utilization.

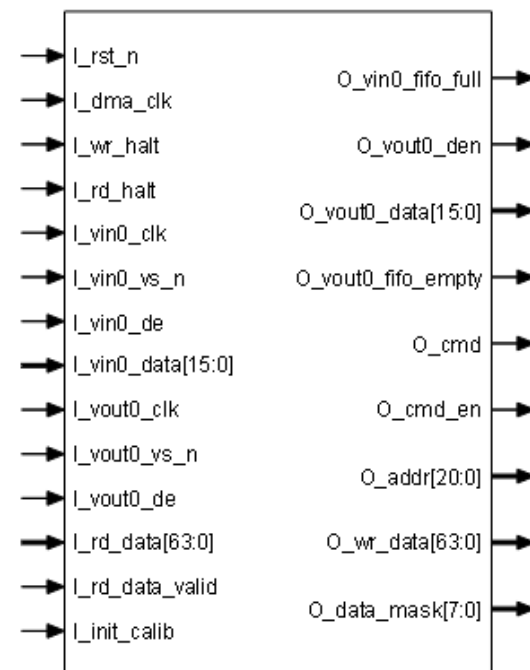
- $W_{in} = 1280 \times 720 \times 60 \times 16 = 884,736,000 \text{ bit/s} = 0.824 \text{ Gbit/s}$
- $W_{out} = 1280 \times 720 \times 60 \times 16 = 884,736,000 \text{ bit/s} = 0.824 \text{ Gbit/s}$
- $W_{meme} = 166 \text{ MHz} \times 16 \times 2 \times 60\% = 3187 \text{ Mbit/s} = 3.112 \text{ Gbit/s}$

Because of $3.112 \text{ Gbit/s} > (0.824 \text{ Gbit/s} + 0.824 \text{ Gbit/s})$, the video frame buffer system can work normally.

3.3 Port List

The I/O port of Gowin Video Frame Buffer with PSRAM IP is shown in Figure 3-2.

Figure 3-2 Ports Diagram



Ports vary slightly depending on the parameters.

The details of I/O ports of Gowin Video Frame Buffer with PSRAM IP are shown in Table 3-1.

Table 3-1 I/O Ports List

No.	Signal Name	I/O	Description	Notes
1	I_rst_n	I	Reset signal, active low.	The I/O of all the signals takes Video Frame Buffer with PSRAM IP as reference.
2	I_dma_clk	I	System operating clock, memory controller output clock.	
3	I_wr_halt	I	Write pointer halt control, and it is valid only in three-frame buffer mode. 0: No halt 1: Write pointer halt	
4	I_rd_halt	I	Read pointer halt control, and it is valid only in three-frame buffer mode.	

No.	Signal Name	I/O	Description	Notes
			0: No halt 1: Read pointer halt	
5	I_vin0_clk	I	Input video clock	
6	I_vin0_vs_n	I	Input video vertical sync, negative polarity.	
7	I_vin0_de	I	Input video data valid	
8	I_vin0_data	I	Input video data	
9	O_vin0_fifo_full	O	Input FIFO full	
10	I_vout0_clk	I	Output video clock	
11	I_vout0_vs_n	I	Output video vertical sync, negative polarity.	
12	I_vout0_de	I	Output video data read enable	
13	O_vout0_den	O	Output video data valid	
14	O_vout0_data	O	Output video data	
15	O_vout0_fifo_empty	O	Output FIFO empty	
16	O_cmd	O	PSRAM command channel	
17	O_cmd_en	O	PSRAM command and address enable signals	
18	O_addr	O	PSRAM address input	
19	O_wr_data	O	PSRAM write data channel	
20	O_data_mask	O	PSRAM write data mask signal	
21	I_rd_data_valid	I	PSRAM read data valid signal	
22	I_rd_data	I	PSRAM read data channel	
23	I_init_calib	I	PSRAM initialization completed signal	

3.4 Parameters Configuration

Table 3-2 Parameters

No.	Name	Range	Default	Description
1	Addr Width	21	21	PSRAM user interface address width
2	Data Width	32/64/128	64	PSRAM user interface data width
3	Write Burst Length	128	128	Write burst length, same as the Burst Mode value in PSRAM Memory Interface IP.
4	Read Burst Length	128	128	Read burst length, same as the Burst Mode value in PSRAM Memory Interface IP.
5	Read FIFO Burst Mult	4/8	4	Read FIFO threshold value, which is a multiple of read burst length.
6	Write FIFO Depth	1024/2048	2048	Write FIFO depth, data unit 32bit
7	Read FIFO depth	1024/2048	2048	Read FIFO depth, data unit 32bit
8	Write Video Data Width	16/24/32	16	Write video data width
9	Read Video Width	16/24/32	16	Read video data width
10	Image Size	21'h000001~21'h1FFFFF	21'h080000	Address space of single frame video

No.	Name	Range	Default	Description
11	Use Three Frame Buffer	Yes/No	Yes	Use three frame buffer or not

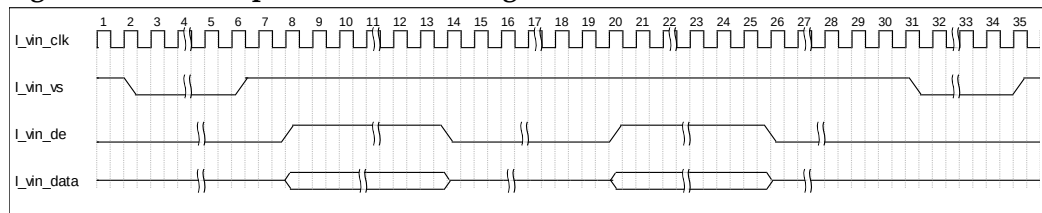
3.5 Timing Description

This section describes the timing of Gowin Video Frame Buffer with PSRAM IP.

3.5.1 Video Interface Timing

The timing diagram of video input interface is as shown in Figure 3-3.

Figure 3-3 Video Input Interface Timing

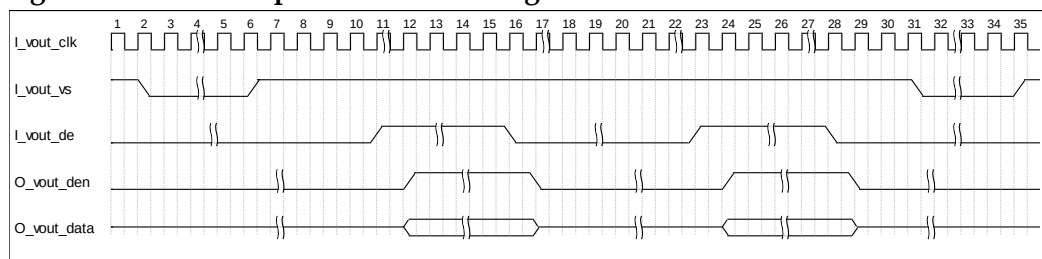


Note!

I_vin_de must be continuous within a line.

The timing diagram of video output interface is as shown in Figure 3-4.

Figure 3-4 Video Output Interface Timing



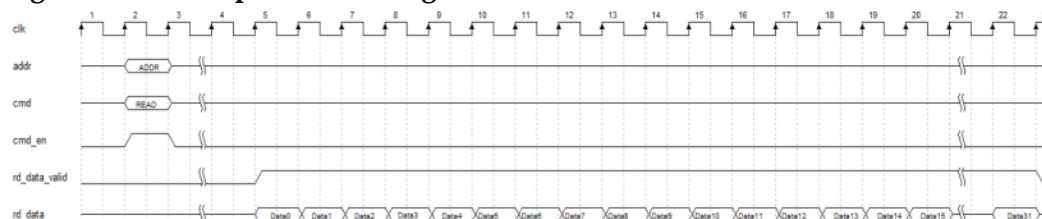
Note!

I_vout_de must be continuous within a line.

3.5.2 PSRAM Memory Interface IP User Interface Timing

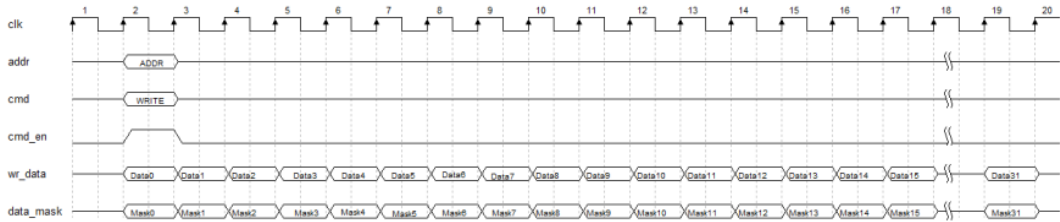
The read operation timing of PSRAM Memory Interface IP user interface is as shown in Figure 3-5, and the burst length is 128.

Figure 3-5 Read Operation Timing



The write operation timing of PSRAM Memory Interface IP user interface is as shown in Figure 3-6, and the burst length is 128.

Figure 3-6 Write Operation Timing



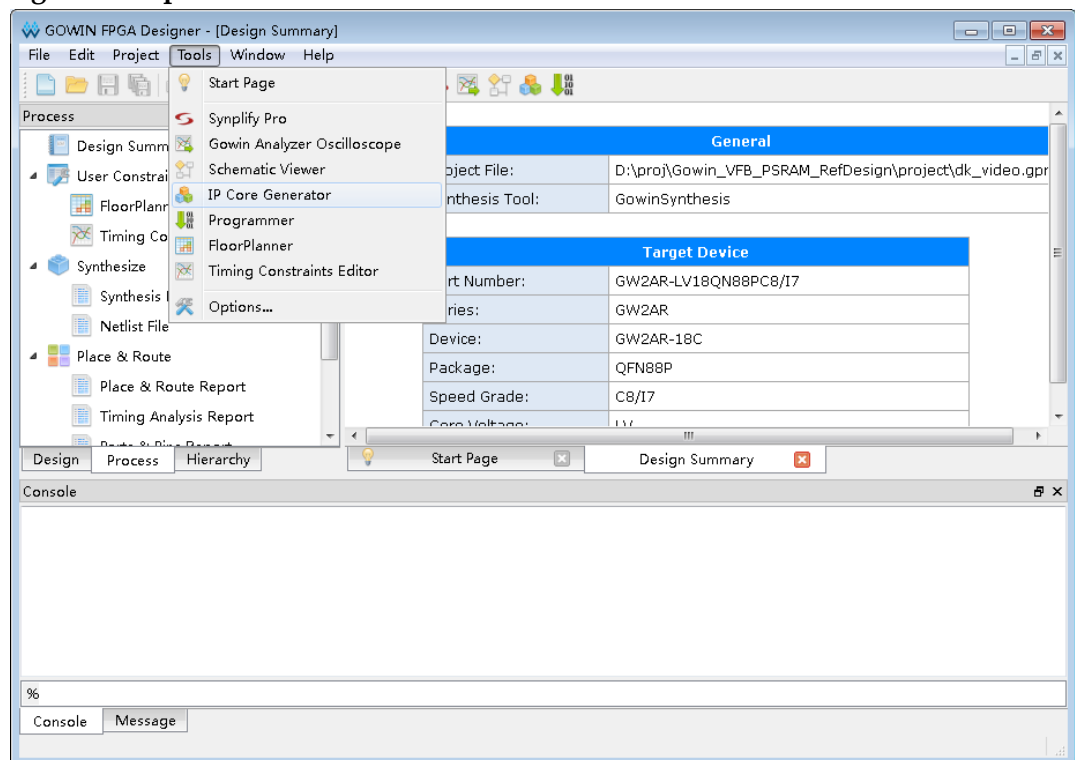
4 Interface Configuration

You can invoke and configure Gowin Video Frame Buffer with PSRAM IP using IP core generator tool in the IDE.

1. Open IP Core Generator

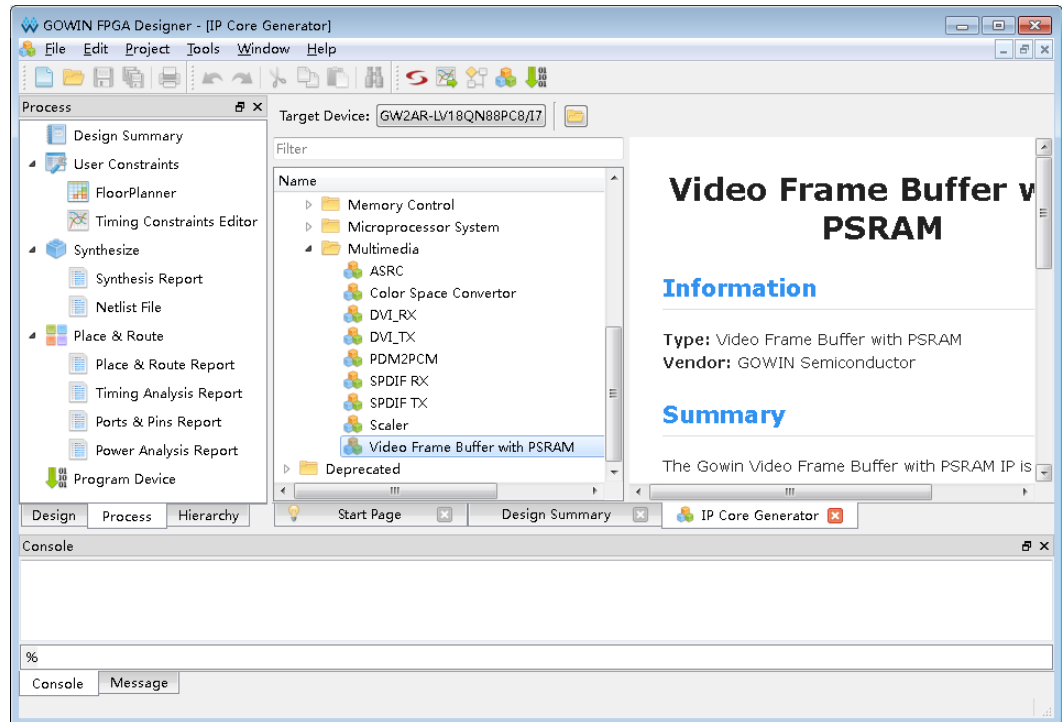
After creating the project, click the "Tools" tab, select and open the IP Core Generator" from the drop-down list, as shown in Figure 4-1.

Figure 4-1 Open IP Core Generator

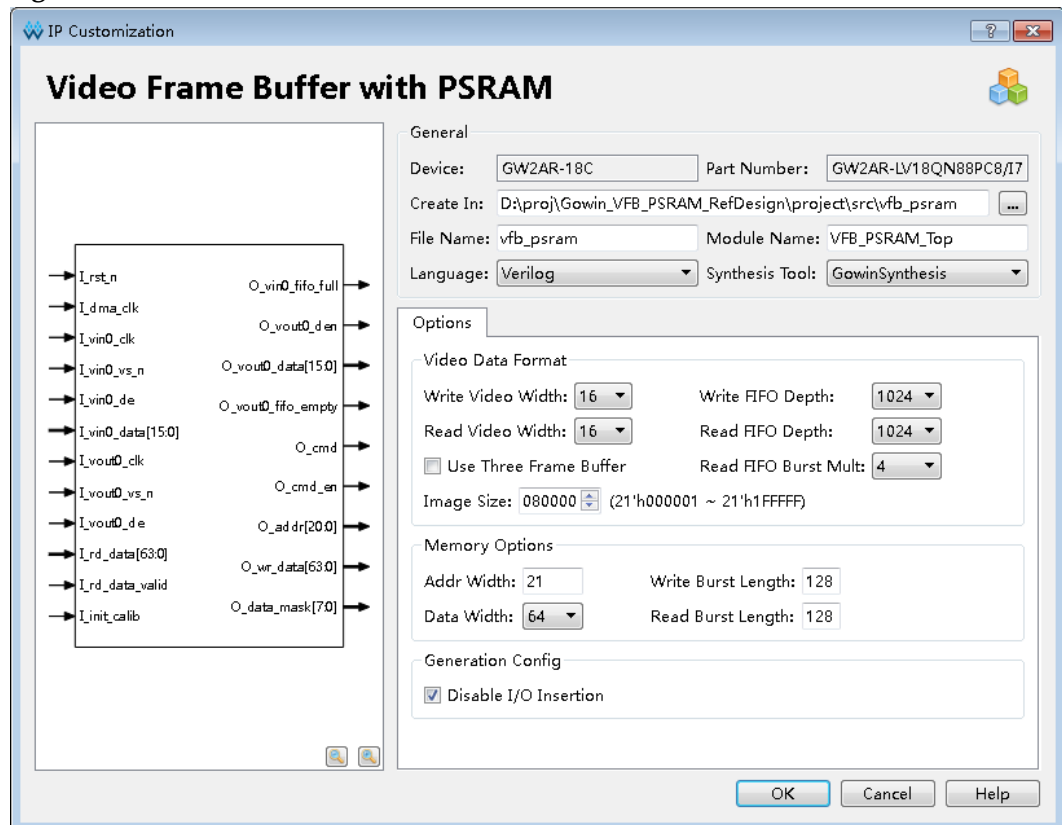


2. Open Video Frame Buffer with PSRAM IP Core

Click "Multimedia" option and double-click "Video Frame Buffer with PSRAM" to open Video Frame Buffer with PSRAM IP core GUI, as shown in Figure 4-2.

Figure 4-2 Open Video Frame Buffer with PSRAM IP Core

3. Video Frame Buffer with PSRAM IP Core Port Diagram
On the left of the configuration interface is the port diagram of Video Frame Buffer with PSRAM IP Core, as shown in Figure 4-3.

Figure 4-3 IP Core GUI

4. Open Help

Click "Help" button in the lower left corner in Figure 4-3 to learn the simple English introduction of configuration options, so as to help users quickly complete the configuration of IP core. The order of options in Help is the same as the one in the interface, as shown in Figure 4-4.

Figure 4-4 Help

Video Frame Buffer with PSRAM

Information

Type: Video Frame Buffer with PSRAM

Vendor: GOWIN Semiconductor

Summary: The Gowin Video Frame Buffer with PSRAM IP is used to receive parallel video input data, cache it to PSRAM Memory, and output parallel video data at the same time. The IP allows designers to create custom systems in one Gowin device that connect easily to VESA standard input/output interface with the PSRAM Memory Interface IP. This IP located between PSRAM Memory Interface IP and the user's logic, reduces the user's effort to deal with the video frame buffer application interface with psram by connecting VESA and PSRAM user interface.

Options & Description

Video Data Format

Write Video Width :

- The data width of VESA write video, support 16/24/32 bits.

Read Video Width :

- The data width of VESA read video, support 16/24/32 bits.

Image Size :

- The address space of single video frame within Addr Width.

Use Three Frame Buffer :

- Whether use three frame buffer: Yes: Three frame buffer mode, No: One frame buffer mode

Write FIFO Depth :

- Write FIFO Depth, the data width is 32 bits.

Read FIFO Depth :

- Read FIFO Depth, the data width is 32 bits.

Read FIFO Burst Mult :

- The threshold of the reading FIFO, which is the integer multiple of Burst Length.

Memory Options

Addr Width :

- The address width of psram user interface.

Data Width :

- The data width of psram user interface.

Write Burst Length :

- The length of write burst, the data width is 16 bits.

Read Burst Length :

- The length of read burst, the data width is 16 bits.

5. Configure the Basic Information

Take GW2AR-18C as an example, and select QFN88P package. The "Module Name" option displays the top-level file name of the generated project, and the default value is "VFB_PSRAM_Top". You can modify the name. The file generated by the IP core is shown in "File Name", which contains the files required by Video Frame Buffer with PSRAM IP core, and the default is "vfb_psram". You can modify the name. "Creat

In" shows the path of IP core file. The default is "\project path\src\vfb_psram". You can modify the path.

Figure 4-5 Basic Information Configuration Interface

General

Device: GW2AR-18C Part Number: GW2AR-LV18QN88PC8/I7

Create In: D:\proj\Gowin_VFB_PSRAM_RefDesign\project\src\vfb_psram

File Name: vfb_psram Module Name: VFB_PSRAM_Top

Language: Verilog Synthesis Tool: GowinSynthesis

6. Options

You can configure parameters of Video Frame Buffer with PSRAM in "Options".

Figure 4-6 Options

Options

Video Data Format

Write Video Width: 16 Write FIFO Depth: 1024

Read Video Width: 16 Read FIFO Depth: 1024

☐ Use Three Frame Buffer Read FIFO Burst Mult: 4

Image Size: 080000 (21'h000001 ~ 21'h1FFFFFF)

Memory Options

Addr Width: 21 Write Burst Length: 128

Data Width: 64 Read Burst Length: 128

Generation Config

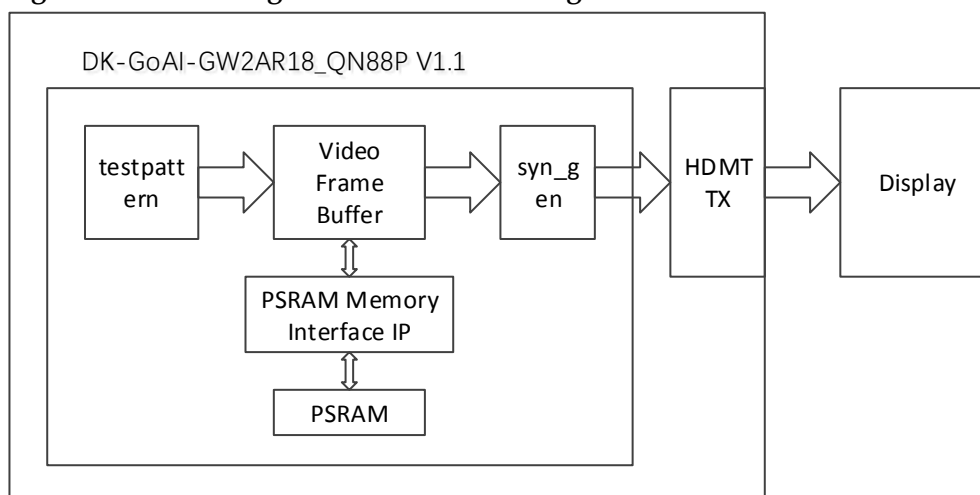
☒ Disable I/O Insertion

5 Reference Design

This chapter describes the use of Video Frame Buffer with PSRAM IP reference design. Please see [Video Frame Buffer with PSRAM reference design](#) for details at Gowinsemi website.

Taking DK-GoAI-GW2AR18_QN88P V1.1 as an example, the diagram is as shown in Figure 5-1. Please see [DK-GoAI-GW2AR18_QN88P V1.1](#) for details at Gowinsemi website.

Figure 5-1 Block Diagram of Reference Design



In the reference design, the test pattern video signal is generated through testpattern module, then input to Video Frame Buffer. Video Frame Buffer is connected to PSRAM controller IP, and syn_gen module generates output video timing. Read the video data from the Video Frame Buffer and output it to the HDMI (J4) port. Connect the HDMI cable to the monitor and you can see the internal test pattern. Test pattern includes color pattern, grid pattern, grayscale pattern and pure color pattern.

6 File Delivery

The delivery files of Gowin Video Frame Buffer with PSRAM IP include the documents, the design source code, and the reference design.

6.1 Documents

The documents folder mainly contains the user guide in PDF.

Table 6-1 Documents List

Name	Description
IPUG752, Gowin Video Frame Buffer with PSRAM IP User Guide	Gowin Video Frame Buffer with PSRAM IP User Guide
RN752, Gowin Video Frame Buffer with PSRAM IP Release Note	–

6.2 Design Source Code (Encryption)

The encryption code folder contains RTL encryption code of Gowin Video Frame Buffer with PSRAM IP used for the GUI.

Table 6-2 Design Source Code

Name	Description
vfb_psram.v	The top-level file of the IP core, which provides you with interface information, encrypted.

6.3 Reference Design

Gowin Video Frame Buffer with PSRAM RefDesign file contains the netlist file, reference design, constraints file, top-level file and the project folder, etc.

Table 6-3 RefDesign Folder

Name	Description
video_top.v	The top module of reference design
testpattern.v	Test pattern generation module
dk_video.cst	Project physical constraints file
dk_video.sdc	Project timing constraints file
vfb_psram	Video Frame Buffer with PSRAM IP folder
psram_memory_interface_hs	PSRAM Memory Interface IP folder
dvi_tx_top	DVI TX IP folder
gowin_rpll	rPLL IP folder
syn_code	Synchronous timing generation module folder

