Gowin Video Frame Buffer IP

User Guide

IPUG769-2.1E, 05/23/2025

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Revision History

Date	Version	Description
03/05/2021	1.0E	Initial version published.
03/31/2023	1.1E	● The description of "One Frame Address Space" parameter updated. ● Interface screenshots updated.
08/18/2023	2.0E	DDR3 memory ports and parameters updated.
05/23/2025	2.1E	● SDRAM Memory descriptions added. ● UHS2 PSRAM memory descriptions added.

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1 About This Guide

1.1 Purpose

The purpose of Gowin Video Frame Buffer IP is to help you learn the features and usage of Gowin Video Frame Buffer IP by providing the descriptions of features, functions, ports, timing, GUI and reference design, etc. The software screenshots in this manual are based on V1.9.11.02 (64-bit). As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

You can find the related documents at www.gowinsemi.com:

- DS100, GW1N series of FPGA Products Data Sheet
- DS117, GW1NR series of FPGA Products Data Sheet
- DS821, GW1NS series of FPGA Products Data Sheet
- DS861, GW1NSR series of FPGA Products Data Sheet
- DS881, GW1NSER series of FPGA Products Data Sheet
- DS891, GW1NRF series FPGA Products Data Sheet
- DS102, GW2A series of FPGA Products Data Sheet
- DS226, GW2AR series of FPGA Products Data Sheet
- DS961, GW2ANR series of FPGA Products Data Sheet
- DS976, GW2A-55 Data Sheet
- DS981, GW5AT series of FPGA Products Data Sheet
- DS1103, GW5A series of FPGA Products Data Sheet
- DS1239, GW5AST series of FPGA Products Data Sheet
- DS1105, GW5AS series of FPGA Products Data Sheet
- DS1108, GW5AR series of FPGA Products Data Sheet
- DS1118, GW5ART series of FPGA Products Data Sheet
- SUG100, Gowin Software User Guide

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
DE	Data Enable
FPGA	Field Programmable Gate Array
HS	Horizontal Sync
IP	Intellectual Property
VESA	Video Electronics Standards Association
VS	Vertical Sync

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Overview

Video Frame Buffer is used to receive parallel video input data, then cache it to memory, and output parallel video data at the same time, thus realizing the frame cache.

Gowin Video Frame Buffer IP is located between VESA standard video input/output interface and the memory interface controller IP, so that you can realize the video frame buffer based on memory.

Table 2-1 Gowin Video Frame Buffer IP

Gowin Video Frame Buffer IP	
Logic Resource	Please refer to Table 2-2 and Table 2-3.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.7.01Beta and above)

Note!

For the devices supported, you can click here to get the information.

2.2 Features

- Supports VESA standard video interfaces
- Supports video data widths of 16, 24, 32, 48, 64, 96, and 128 bits
- Supports Gowin DDR3/PSRAM/HyperRAM/SDRAM/UHS2 PSRAM Memory Interface IPs

2.3 Resource Utilization

Gowin Video Frame Buffer IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades.

Take GW2A-18 FPGA as an instance, and the resource utilization is as shown in Table 2-2 and Table 2-3.

Table 2-2 Gowin Video Frame Buffer IP Resource Utilization

Memory	DDR3	PSRAM	HyperRAM	SDRAM	UHS2 PSRAM
Device	GW2A-18	GW2A-18	GW2A-18	GW2AR-18	GW5ART-15
Video width	16	16	16	16	16
FIFO Depth	2048	2048	2048	2048	2048
LUTs	818	642	589	477	506
Registers	402	386	419	354	341
BSRAMs	8	8	8	4	4

Table 2-3 Number of BSRAM

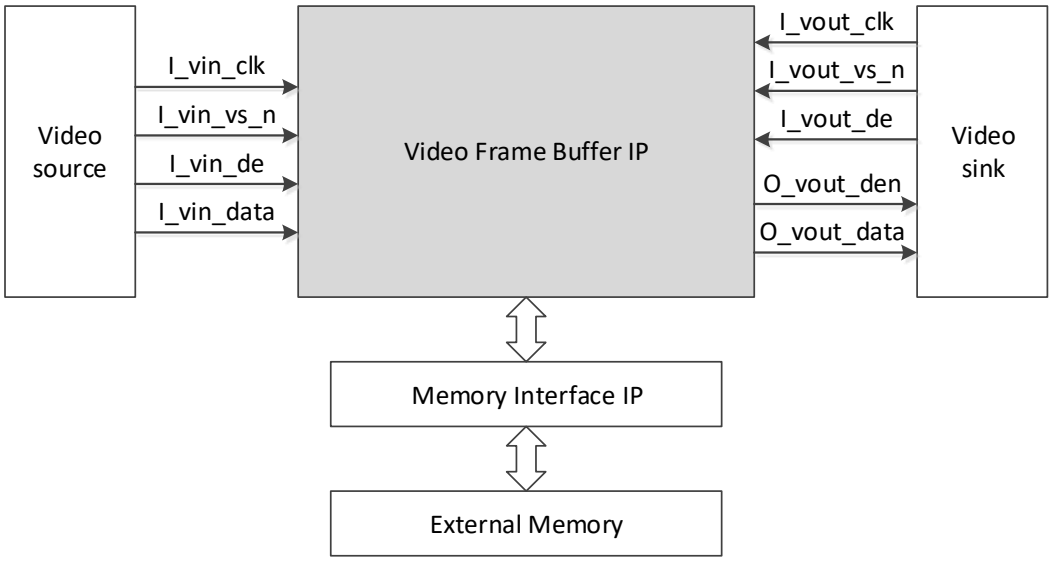
Memory Data Bit Width	32		64		128	
Read and Write FIFO Depth	1024	2048	1024	2048	1024	2048
Number of BSRAM	4	8	4	8	8	8

3 Functional Description

3.1 Block Diagram

Gowin Video Frame Buffer with IP is used to implement video input and output frame buffer based on external memory. The system diagram is as shown in Figure 3-1.

Figure 3-1 Block Diagram



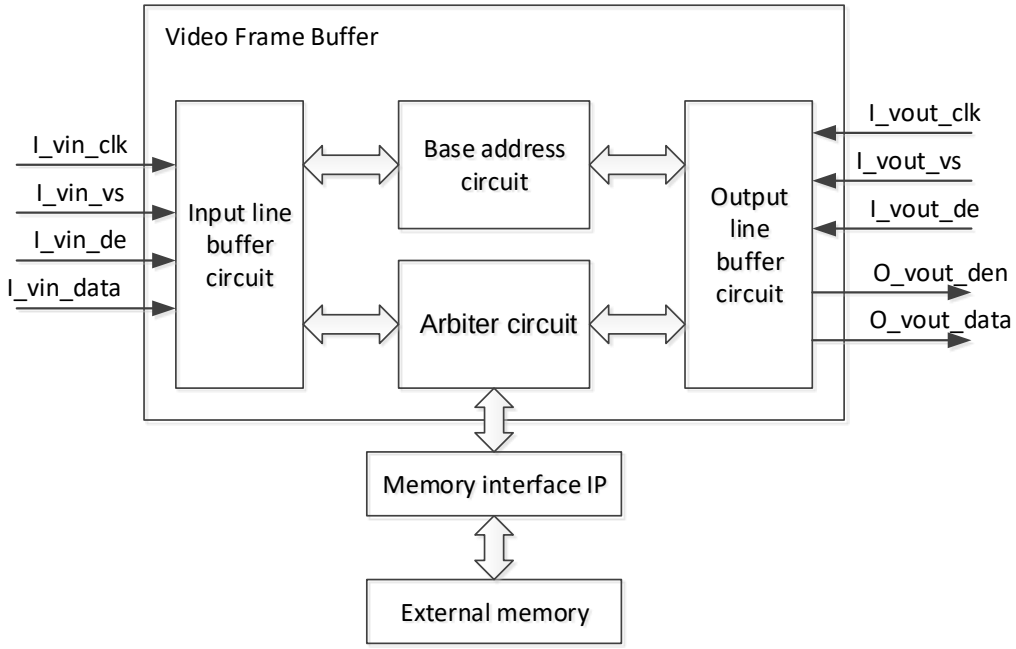
3.2 Implementation Principle

3.2.1 Circuit

Video frame buffer system includes video source, video sink, video frame buffer, memory interface IP and external memory.

Video Frame Buffer includes four parts: input line buffer circuit, output line buffer circuit, base address circuit and arbiter circuit. The circuit structure is shown in Figure 3-2.

Figure 3-2 Block Diagram

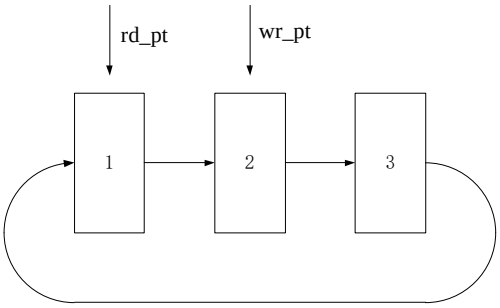


The input line buffer circuit receives parallel video input data and caches it to the input FIFO line buffer. A write request is sent to the arbiter controller when the data in the FIFO reaches the preset threshold. When the arbiter controller responds to the request, it starts sending write data, addresses and commands.

The output line buffer circuit sets a read threshold and sends a request to the arbiter when the data in the output FIFO line buffer is below this threshold. When the arbiter responds to the request, the arbiter starts sending read commands and addresses and stores the received data in the output FIFO. When the output FIFO receives the DE signal of the output video, that is, the FIFO read enable signal, the output FIFO outputs the video data.

Three-frame buffer is usually used to avoid image tearing. A three-frame buffer includes one frame in write, one frame in read, and one frame in transition, which can be indicated by read/read pointers, and the read/write pointers respectively points to the start address of the frame buffer, that is, the base address of each frame. The base address control circuit is to control the read/write pointers. If you do not choose three frame buffer, read and write operations are in the same address space.

Figure 3-3 Three- frame Buffer Diagram



As shown in Figure 3-3, the three-frame buffer is represented by three boxes labeled with numbers; the read pointer is represented by rd_pt, and the write pointer is represented by wr_pt.

1. Both read and write pointers are cyclic in the order of frame 1, frame 2, frame 3.
2. rd_pt points to the next frame when one frame of data has been read.
3. wr_pt points to the next frame when one frame of data has been written.
4. After the initial reset, both read and write pointers start from frame 1.
5. When read is faster than write, it will be adjusted by repeating read frame, i.e., the output frame rate is larger than the input frame rate, and the switching of the read pointer is faster than that of the write pointer. As shown in Figure 3-3, when a frame of data is read, rd_pt should be switched from frame 1 to frame 2, if it is found that wr_pt is still in frame 2, then rd_pt still stops at frame 1, and read the data from frame 1, i.e., repeating frame 1 data one time.
6. When write is faster than read, it will be adjusted by writing a new frame to overwrite the previous frame, i.e., the input frame rate is greater than the output frame rate, and the switching of write pointer is faster than that of the read pointer. As shown in Figure 3-3, when one frame of data is written, wr_pt is to be switched to frame 3 from frame 2; at this time, frame 3 is not occupied, then wr_pt is switched to frame 3 to write the data; because write is fast, after writing a frame of data, wr_pt should be switched to frame 1 from frame 3; if it is found that rd_pt is still in frame 1, then rd_pt still stops at frame 3, then the data is still written to frame 3 buffer, overwriting the previously written data.
7. When the read and write rates are the same, i.e., the output frame rate is equal to the input frame rate, then the read pointer will always follow the write pointer, switching at the same rate.

The arbiter circuit is to receive and arbitrate the memory read/write access requests from the input line buffer control circuit and the output line buffer control circuit. At the same time, the data interface of input line buffer control circuit and output line buffer control circuit is connected to the user data interface of memory interface IP.

3.2.2 Bandwidth Estimation

In order to make a video frame buffer system work properly, it must ensure that the video input/output bandwidths and memory bandwidths meet certain conditions. Take PSRAM memory as an example.

Assume that the input video horizontal resolution is H_{in}, vertical resolution is V_{in}, field frequency is F_{vsin} Hz, pixel bit width N_{in} bit; output video horizontal resolution is H_{out}, vertical resolution is V_{out}, field frequency is F_{vsout}, pixel bit width N_{out} bit; PSRAM clock frequency is F_{clk} MHz, data bit width D bit, double edge data transmission (i.e. data bandwidth needs to be multiplied by 2), read and write operation efficiency e%.

The bandwidth estimation method is as follows:

- Video input bandwidth $W_{in} = H_{in} * V_{in} * F_{vsin} * N_{in}$ (bit/s)
- Video output bandwidth $W_{out} = H_{out} * V_{out} * F_{vsout} * N_{out}$ (bit/s)
- Memory theoretical bandwidth $Wmem = F_{clk} * D * 2$ (bit/s)
- Memory effective bandwidth $Wmeme = F_{clk} * D * 2 * e\%$ (bit/s)

Note!

The video frame buffer system can only work properly when Wmeme > (Win+Wout).

For example, the input video format 1280x720@60Hz, pixel format RGB565, pixel bit width 16bit; output video format 1280x720@60Hz, pixel format RGB565, pixel bit width 16bit; PSRAM clock frequency 166MHz, data bit width 16bit, read/write operation efficiency 60%.

- W_{in} = 1280*720*60*16= 884,736,000bit/s = 0.824Gbit/s
- W_{out} = 1280*720*60*16= 884,736,000bit/s = 0.824Gbit/s
- W_{meme} = 166MHz*16*2*60% = 3187Mbit/s = 3.112Gbit/s

Note!

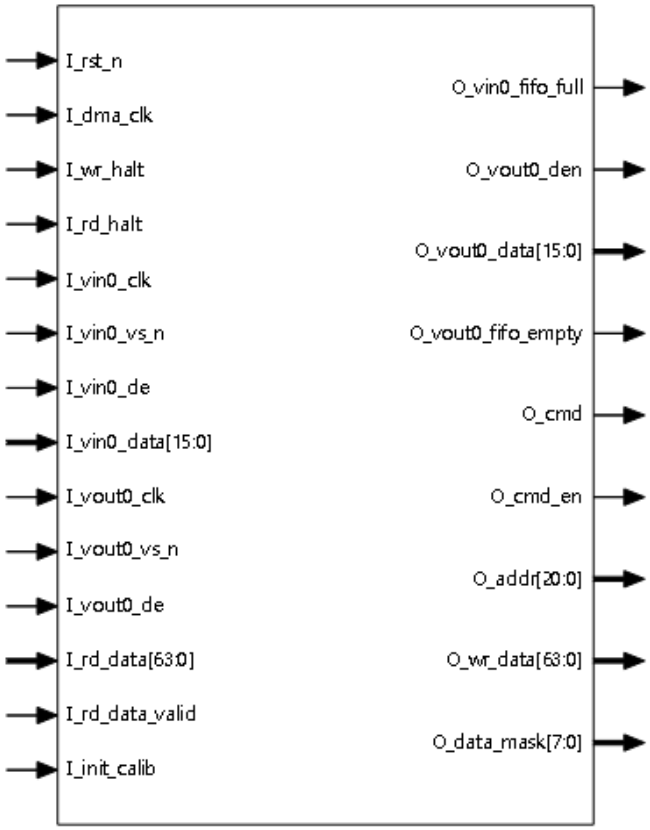
The efficiency of read/write operation depends on the bandwidth efficiency of PSRAM and video.

Since 3.112Gbit/s > (0.824Gbit/s + 0.824Gbit/s), the video frame buffer system can work properly.

3.3 Port List

The IO ports of Gowin Video Frame Buffer IP are shown in Figure 3-4.

Figure 3-4 Ports Diagram



Ports vary slightly depending on the parameters.

The details of I/O ports are shown in Table 3-1.

Table 3-1 I/O List

No.	Signal Name	I/O	Description	Note
1	I_rst_n	I	Reset signal, active-low.	The I/O of all the signals takes Video Frame Buffer IP as reference.
2	I_dma_clk	I	Memory W/R clock signal	
3	I_wr_halt	I	Write pointer halt signal, 1: halt; Valid in three-frame buffer mode If not debugging the write pointer at the debug ports, the port must be assigned the value 0.	
4	I_rd_halt	I	Read pointer halt signal, 1: halt; Valid in three-frame buffer mode If not debugging the write pointer at the debug ports, the port must be assigned the value 0.	
5	I_vin0_clk	I	Input video clock signal	
6	I_vin0_vs_n	I	Input vs, negative polarity.	
7	I_vin0_de	I	Input data valid signal	

No.	Signal Name	I/O	Description	Note
8	I_vin0_data	I	Input video data signal	
9	O_vin0_fifo_full	O	Input FIFO full signal	
10	I_vout0_clk	I	Output video clock signal	
11	I_vout0_vs_n	I	Output vs, negative polarity.	
12	I_vout0_de	I	Output data read enable signal	
13	O_vout0_den	O	Output data valid signal, 2 clock cycles delayed than I_vout0_de signal	
14	O_vout0_data	O	Output video data signal	
15	O_vout0_fifo_empty	O	Output FIFO empty signal	
DDR3 Interface (1)				
16	I_cmd_ready	I	Memory interface receives commands and addresses at high level	
17	O_cmd	O	Command channel	
18	O_cmd_en	O	Command and address enable signal	
19	O_app_burst_number	O	Port of continuous burst times, only available when Burst Number Enable is checked	
20	O_addr	O	Address input	
21	I_wr_data_rdy	I	MC can receive the user data at high level	
22	O_wr_data_en	O	wr_data enable signal	
23	O_wr_data_end	O	High level indicates that the current clock cycle is the last cycle of this wr_data.	
24	O_wr_data	O	Write data channel	
25	O_wr_data_mask	O	Provides the mask signal for wr_data	
26	I_rd_data_valid	I	rd_data valid signal	
27	I_rd_data_end	I	High-level indicates the end cycle of the current rd_data.	
28	I_rd_data	I	Read data channel	
29	I_init_calib_complete	I	Initialization completed signal	
PSRAM/HyperRAM Interface (2)				
31	O_cmd	O	Command channel	
32	O_cmd_en	O	Command and address enable signal	
33	O_addr	O	Address input	
34	O_wr_data	O	Write data channel	
35	O_data_mask	O	Write data mask signal	
36	I_rd_data_valid	I	Read data valid signal	

No.	Signal Name	I/O	Description	Note
37	I_rd_data	I	Read data channel	
38	I_init_calib	I	Initialization completed signal	
SDRAM Interface (3)				
39	I_sdrc_busy_n	I	Memory controller idle indication; user logic can initiate R/W. 1: Idle 0: Busy	
40	O_sdrc_wr_n	O	Write enable, active-low.	
41	O_sdrc_rd_n	O	Read enable, active-low.	
42	O_sdrc_addr	O	Address input	
43	O_sdrc_data_len	O	Read/Write data length. Taking I_sdrc_data_len[7:0] as an example, the input range is 0–255, which corresponds to a valid read/write length range of 1~256.	
44	O_sdrc_data	O	Write data channel	
45	O_sdrc_dqm	O	Write data mask control	
46	I_sdrc_rd_valid	I	Read data valid indication, active-high, aligned with valid data.	
47	I_sdrc_data_out	I	Read data channel	
48	I_sdrc_init_done	I	Power-on initialization indication: 1: Done 0: Not done	
UHS2 PSRAM Interface (4)				
49	I_cmd_ready	I	Memory cmd write enable flag: 0: Cannot be written 1: Can be written	
50	O_cmd	O	Read/Write command	
51	O_cmd_en	O	Command/address enable signal: 0: Invalid 1: Valid	
52	O_burst_num	O	Number of bursts per operation. Input range: 0–255, corresponding to burst count of 1–256.	
53	O_addr	O	Read/Write start address	

No.	Signal Name	I/O	Description	Note
54	I_wr_data_rdy	I	Write data write enable flag: 0: Cannot write data 1: Can write data	
55	O_wr_data_en	O	Write data enable signal: 0: Data invalid 1: Data valid	
56	O_wr_data	O	Write data channel	
57	O_wr_data_mask	O	Write data mask control	
58	I_rd_data_valid	I	Read data valid indication, active-high.	
59	I_rd_data	I	Read data channel	
60	I_init_calib_complete	I	Initialization done signal	

Note!

- For DDR3 ports descriptions, you can see *IPUG281, Gowin DDR3 Memory Interface IP User Guide*.
- For PSRAM ports descriptions, you can see *IPUG943, Gowin PSRAM HS Memory Interface IP User Guide*.
- For HyperRAM ports descriptions, you can see *IPUG944, Gowin HyperRam Memory Interface IP User Guide*.
- For SDRAM ports descriptions, you can see *IPUG279, Gowin SDRAM Controller IP User Guide*.
- For UHS2 PSRAM ports descriptions, you can see *IPUG1194, Gowin UHS2 PSRAM Memory Interface IP User Guide*.

3.4 Parameter Configuration

Table 3-2 Gowin Video Frame Buffer IP Parameters

No.	Name	Range	Default	Description
1	Memory Type	DDR3/PSRAM/HyperRAM/SDRAM/UHS2 PSRAM	DDR3	External memory type
2	Addr Width	21/22/23/25/26/27/28/29/30/31/32	28	Memory interface IP user interface address width
3	Data Width	16/32/64/128/256/512	128	Memory interface IP user interface address width
4	Write Burst Length	16/32/64/128	64	Continuous burst write length
5	Read Burst Length	16/32/64/128	64	Continuous burst read length

No.	Name	Range	Default	Description
6	Write Video Width	8/16/24/32/48/64/96/128	16	Write video data width
7	Read Video Width	8/16/24/32/48/64/96/128	16	Read video data width
8	One Frame Address Space	0x00000001 ~0xFFFFFFFF	0x00800000	One frame address space; the data bit width of address depends on memory type.
9	Use Three Frame Buffer	Yes/No	Yes	Use three frame buffer or not
10	Write FIFO Depth	1024/2048/4096	2048	Write FIFO depth, 32 bits
11	Read FIFO Depth	1024/2048/4096	2048	Read FIFO depth, 32 bits
12	Burst Number Enable	Yes/No	No	Burst length enable, valid only when Memory Type is DDR3

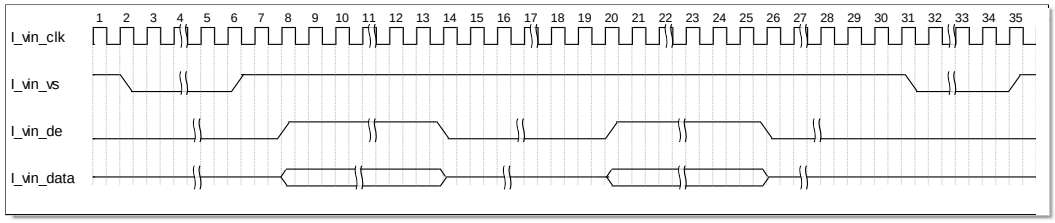
3.5 Timing Description

This section describes the timing of Gowin Video Frame Buffer IP.

3.5.1 Video Interface Timing

The timing diagram of video interface is as shown in Figure 3-5.

Figure 3-5 Timing Diagram of Video Interface

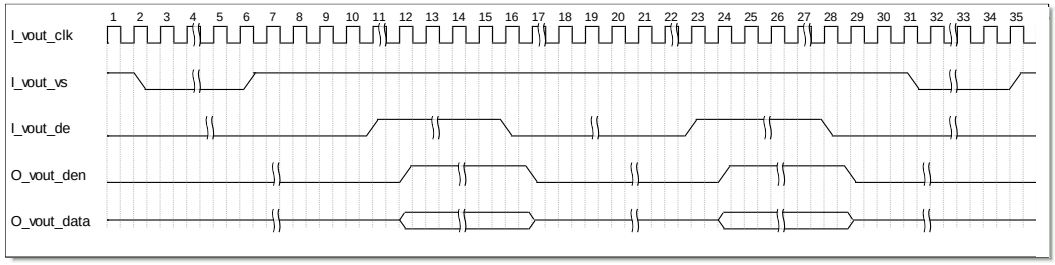


Note!

- I_vin_vs is negative polarity, i.e., low during vs synchronization.
- I_vin_de must be continuous within a line, DE discontinuity within a line is not supported.

The timing diagram of video output interface is as shown in Figure 3-5.

Figure 3-6 Video Output Interface Timing



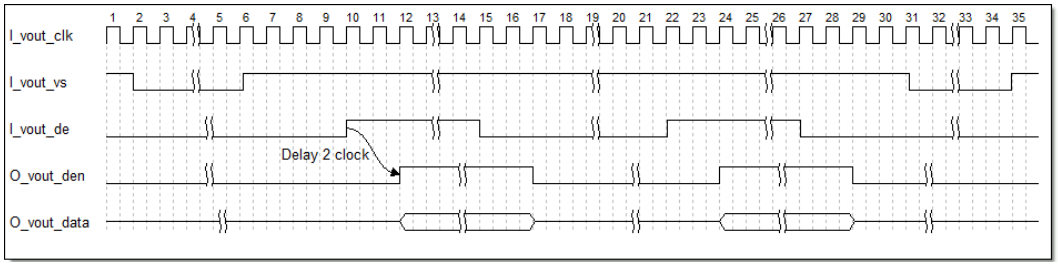
Note!

- I_vout_vs is negative polarity, i.e., low during vs synchronization.
- I_vout_de must be continuous within a line, DE discontinuity within a line is not supported.

For the Read Video Width parameter, the available options are 8/16/24/32/48/64/96/128. When 24/48/96 is selected, data width conversion is involved, which results in different read delays.

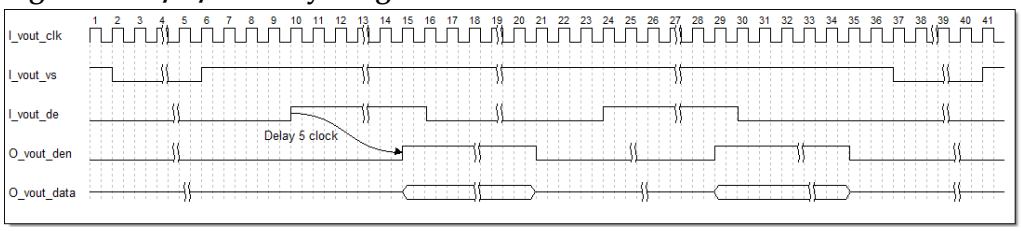
The delay diagram for selecting 8/16/32/64/128 is shown in Figure 3-7.

Figure 3-7 8/16/32/64/128 Delay Diagram



The delay diagram for selecting 24/48/96 is shown in Figure 3-8.

Figure 3-8 24/48/96 Delay Diagram



3.5.2 Memory Interface IP User Interface Timing

- For the read and write timing of DDR3 memory interface IP, you can see *IPUG281, Gowin DDR3 Memory Interface IP User Guide*.
- For the read and write timing of PSRAM memory interface IP, you can see *IPUG943, Gowin PSRAM HS Memory Interface IP User Guide*.
- For the read and write timing of HyperRAM memory interface IP, you can see *IPUG944, Gowin HyperRam Memory Interface IP User Guide*.
- For the read and write timing of SDRAM memory interface IP, you can see *IPUG279, Gowin SDRAM Controller IP User Guide*.
- For the read and write timing of UHS2 PSRAM memory interface IP, you can see *IPUG1194, Gowin UHS2 PSRAM Memory Interface IP User Guide*.

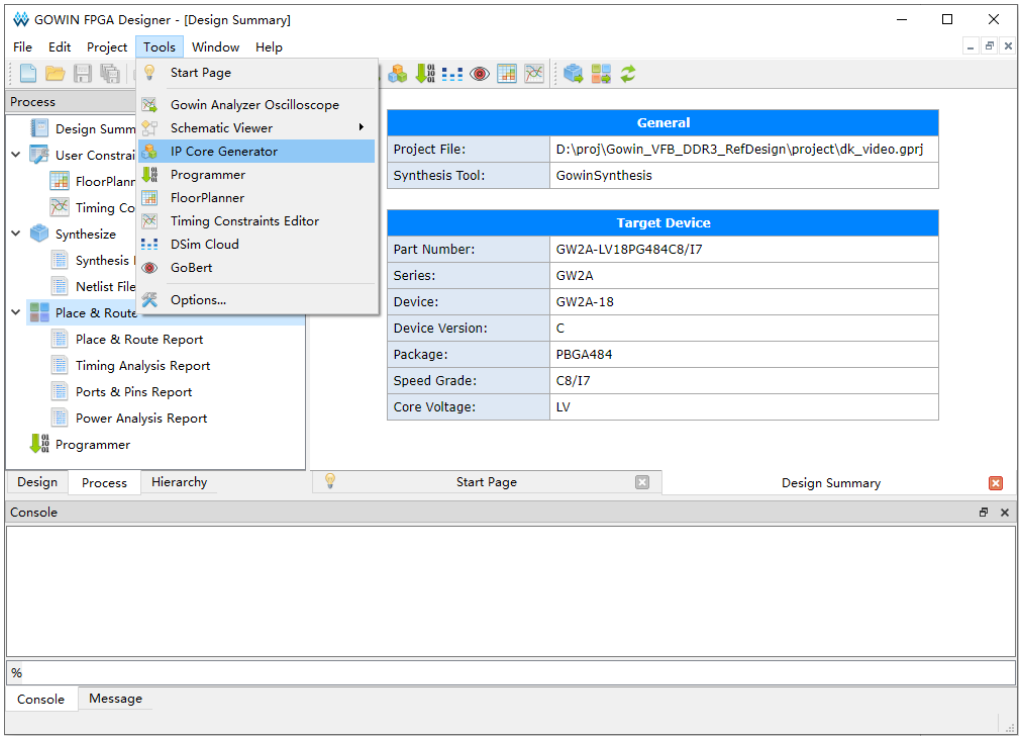
4 GUI

You can invoke and configure Video Frame Buffer IP using IP core generator tool in the IDE.

1. Open IP Core Generator

After creating the project, click the “Tools” tab in the upper left, select and open the IP Core Generator from the drop-down list, as shown in Figure 4-1.

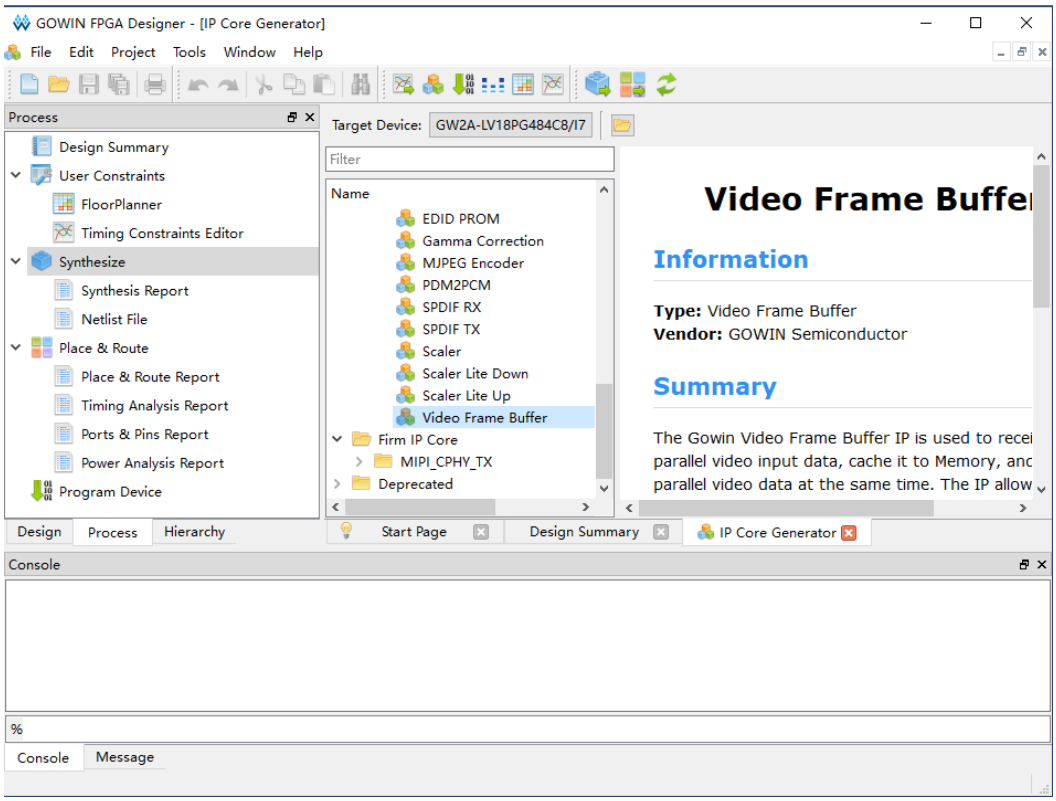
Figure 4-1 Open IP Core Generator



2. Open Video Frame Buffer IP Core

Click "Multimedia" and double click "Video Frame Buffer" to open the configuration interface, as shown in Figure 4-2.

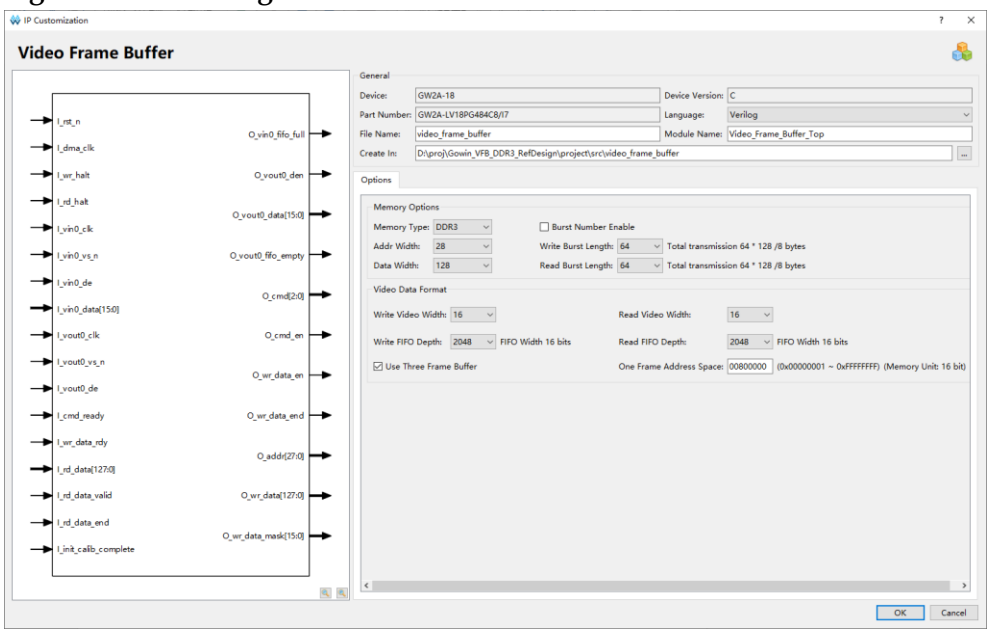
Figure 4-2 Open Video Frame Buffer IP Core



3. Video Frame Buffer IP Core Ports

On the left of the configuration interface is the ports diagram of Video Frame Buffer IP core, as shown in Figure 4-3.

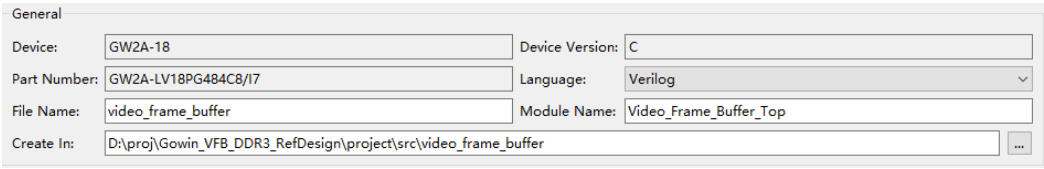
Figure 4-3 Ports Diagram of Video Frame Buffer IP



4. Configure Basic Information

See the project basic information in the configuration interface. Take GW2A-18C and PBGA484 package as an example. The "Module Name" displays the top-level file name of the generated project, and the default is "Video_Frame_Buffer_Top". You can modify the name. The "File Name" displays the folder generated by the IP core, which contains the files required by Video Frame Buffer IP core, and the default is "video_frame_buffer". You can modify the path."Create In" displays the path of IP core folder. The default is "\project path\src\video_frame_buffer". You can modify the path.

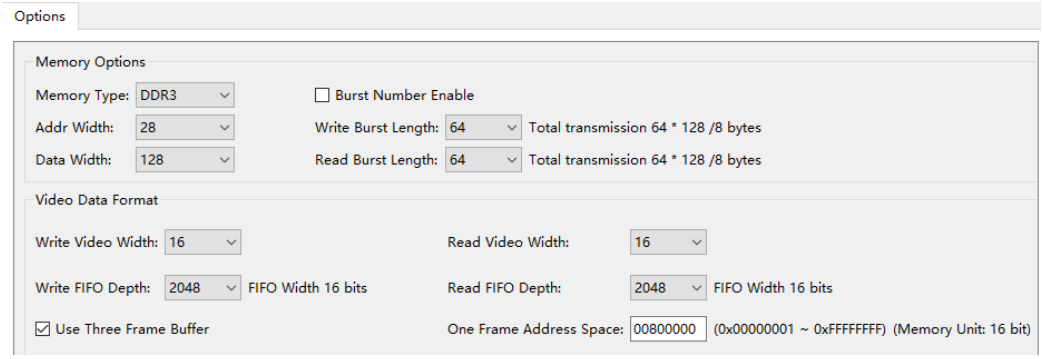
Figure 4-4 Basic Information Configuration Interface



5. Options

You can configure memory type and video data format in the Options.

Figure 4-5 Options



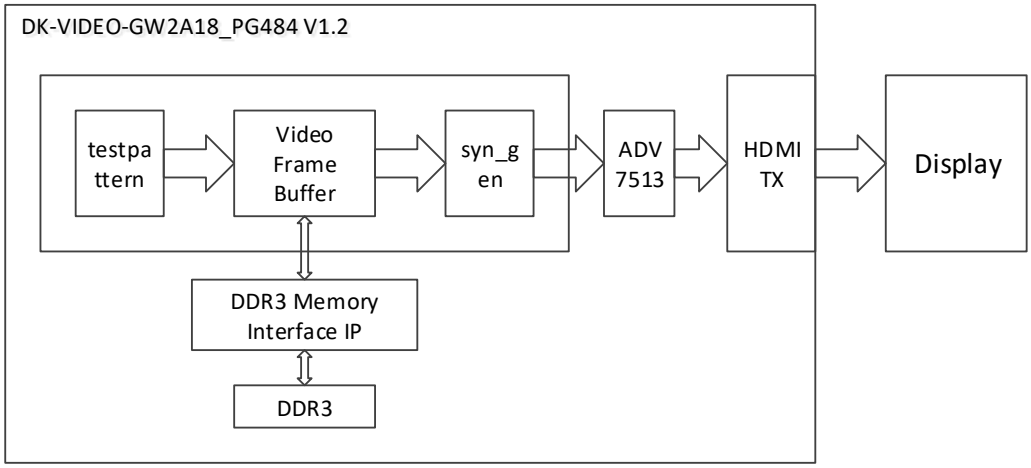
5 Reference Design

This chapter introduces the usage and constructure of the reference design instance of Video Frame Buffer IP. Please see the Video Frame Buffer Reference Design for details at Gowinsemi website.

5.1 Design Instance 1

Use DK-VIDEO-GW2A18-PG484V1.2 as an example, and the block diagram of the design is as shown in Figure 5-1. For details of DK-VIDEO-GW2A18-PG484V1.2 development board, click here to get.

Figure 5-1 Block Diagram of Reference Design 1

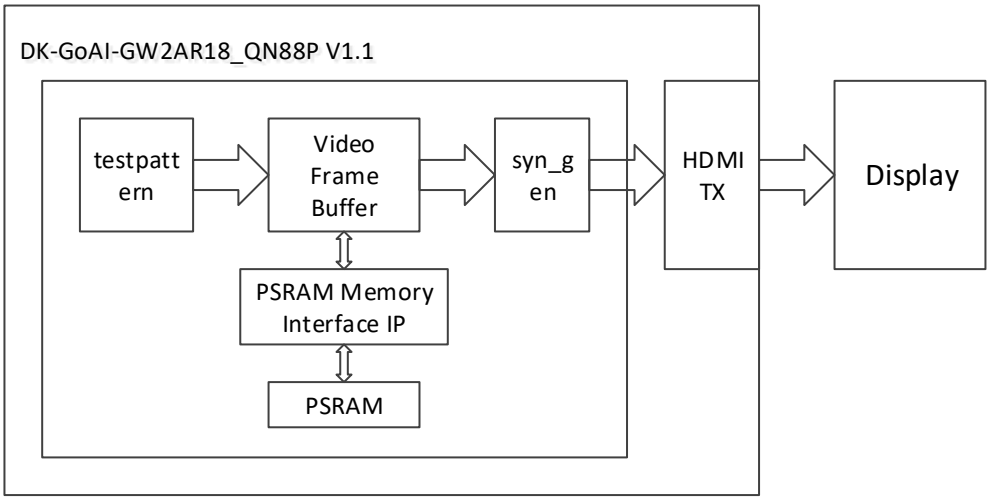


In the reference design, the test pattern video signal is generated through testpattern module and input to Video Frame Buffer. Video Frame Buffer is connected to DDR3 controller IP, and syn_gen module is used to generate output video timing and read the video data from the Video Frame Buffer. The data is then output to HDMI2 TX. Connect the HDMI cable to the display and you can see the internal test pattern on the display. These test pattern include color pattern, grid pattern, grayscale pattern and solid color pattern.

5.2 Design Instance 2

Use DK-GoAI-GW2AR18-QN88P V1.1 as an example, and the block diagram of the design in Figure 5-2. For details of DK-GoAI-GW2AR18-QN88P V1.1 development board, click here to get.

Figure 5-2 Block Diagram of Reference Design 3

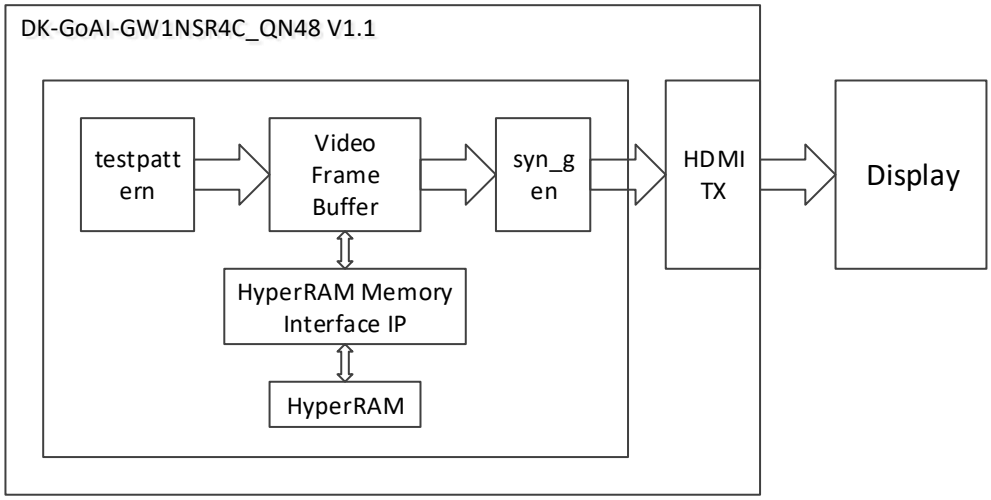


In the reference design, the test pattern video signal is generated through testpattern module and input to Video Frame Buffer. Video Frame Buffer is connected to PSRAM controller IP, and syn_gen module is used to generate output video timing and read the video data from the Video Frame Buffer. The data is then output to the HDMI (J4) port. Connect the HDMI cable to the display and you can see the internal test pattern on the display. These test pattern include color pattern, grid pattern, grayscale pattern and solid color pattern.

5.3 Design Instance 3

Use DK-GoAI-GW1NSR4C-QN48 V1.1 as an example, and the block diagram of the design is as shown in Figure 5-3. For details of DK-GoAI-GW1NSR4C-QN48 V1.1 development board, click here to get.

Figure 5-3 Block Diagram of Reference Design 3

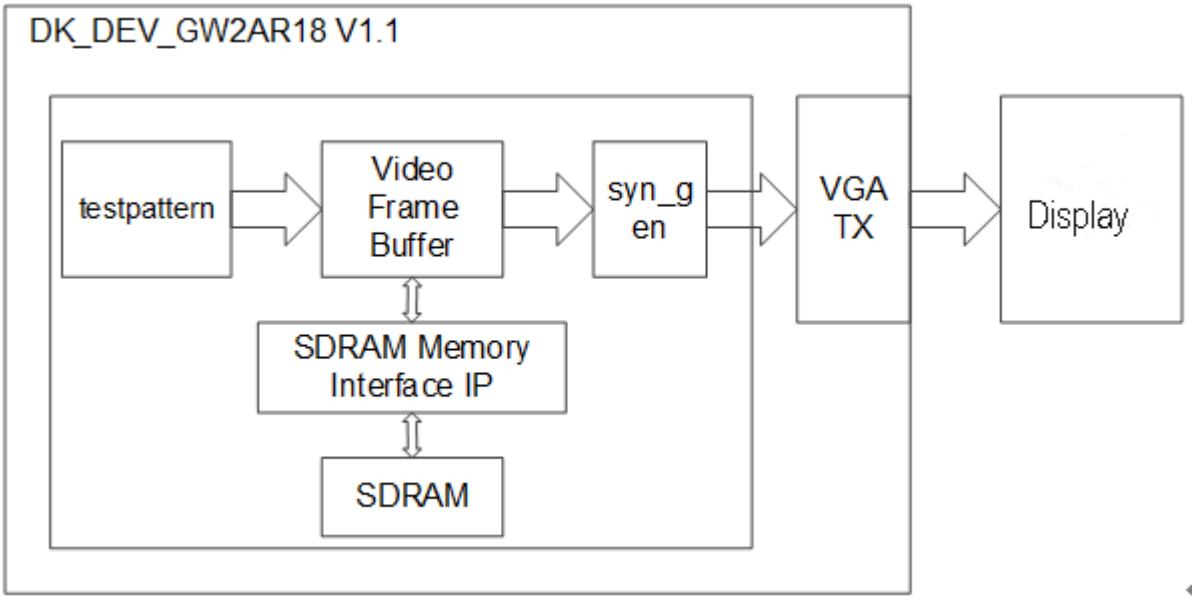


In the reference design, the test pattern video signal is generated through test pattern module and input to Video Frame Buffer. Video Frame Buffer is connected to HyperRAM controller IP, and syn_gen module is used to generate output video timing and read the video data from the Video Frame Buffer. The data is then output to the HDMI (J4) port. Connect the HDMI cable to the display and you can see the internal test pattern. These test patterns include color pattern, grid pattern, grayscale pattern and solid color pattern.

5.4 Design Instance 4

Use DK_DEV_GW2AR18 V1.1 development board as an example, and the block diagram of the design is shown in Figure 5-4.

Figure 5-4 Block Diagram of Reference Design 4



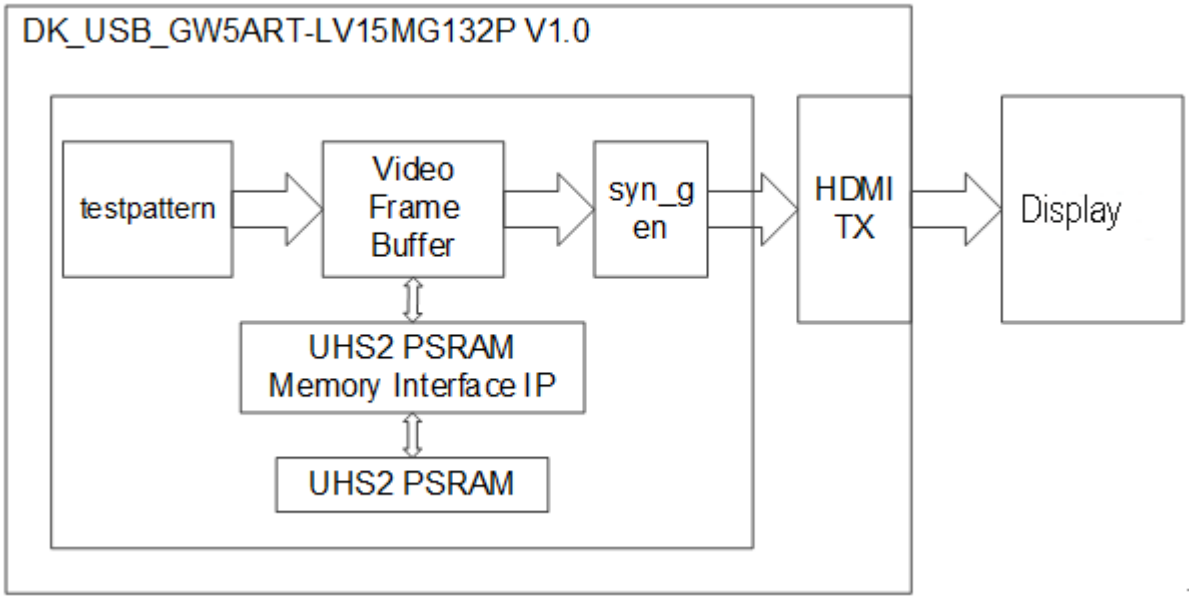
In the reference design, the test pattern video signal is generated through test pattern module and input to Video Frame Buffer. The Video

Frame Buffer is connected to the SDRAM controller IP. The syn_gen module is used to generate the output video signals and read video data from the Video Frame Buffer. The data is then output through a parallel GPIO interface, converted to VGA format by a GPIO-to-VGA converter, and transmitted to a monitor via a VGA cable, which can display the internally generated test patterns. These patterns include color bars, grid, grayscale, and solid color images.

5.5 Design Instance 5

Use DK_USB_GW5ART-LV15MG132P_V1.0 development board as an example, and the basic block diagram of the design is shown in Figure 5-5.

Figure 5-5 Block Diagram of Reference Design 5



In the reference design, the test pattern video signal is generated through test pattern module and input to Video Frame Buffer. The Video Frame Buffer is connected to the UHS2 PSRAM Controller IP. The syn_gen module is used to generate output video signals and read video data from the Video Frame Buffer. The data is then output to the HDMI (J12) port, transmitted to a monitor via an HDMI cable, which can display the internally generated test patterns. The test patterns include color bars, grid, grayscale, and solid color images.

6 File Delivery

The delivery files for the Gowin Video Frame Buffer IP include the documents, the design source code, and the reference design.

6.1 Documents

The documents mainly contain the user guide in PDF.

Table 6-1 Documents List

Name	Description
IPUG769, Gowin Video Frame Buffer IP User Guide	Gowin IP User Guide, namely this one.

6.2 Design Source Code (Encryption)

The encrypted code file contains the RTL encrypted code of the Gowin Video Frame Buffer IP which is used for GUI in order to cooperate with Gowin software to generate the IP core required by you.

Table 6-2 Design Source Code List

Name	Description
video_frame_buffer.v	The top-level file of the IP core, which provides you with interface information, encrypted.

6.3 Reference Design

The Ref. Design folder contains the netlist file, user reference design, constraints file, top-level file and the project file, etc.

Table 6-3 Gowin VFB DDR3 RefDesign Folder List

Name	Description
video_top.v	The top module of reference design
testpattern.v	Test pattern generation module
dk_video.cst	Project physical constraints file
dk_video.sdc	Project timing constraints file
video_frame_buffer	Video Frame Buffer IP folder
ddr3_memory_interface	Gowin DDR3 Memory Interface IP folder
i2c_master	I2C Master IP folder

Name	Description
gowin_rpll	rPLL IP folder
syn_code	Sync timing generation module folder

The Ref. Design folder contains the netlist file, user reference design, constraints file, top-level file and the project file, etc.

Table 6-4 Gowin VFB PSRAM RefDesign Folder List

Name	Description
video_top.v	The top module of reference design
testpattern.v	Test pattern generation module
dk_video.cst	Project physical constraints file
dk_video.sdc	Project timing constraints file
video_frame_buffer	Video Frame Buffer IP folder
psram_memory_interface_hs	PSRAM Memory Interface IP folder
dvi_tx_top	DVI TX IP folder
gowin_rpll	rPLL IP folder
syn_code	Sync timing generation module folder

The Ref. Design folder contains the netlist file, user reference design, constraints file, top-level file and the project file, etc.

Table 6-5 Gowin VFB HyperRAM RefDesign Folder List

Name	Description
video_top.v	The top module of reference design
testpattern.v	Test pattern generation module
dk_video.cst	Project physical constraints file
dk_video.sdc	Project timing constraints file
video_frame_buffer	Video Frame Buffer IP folder
hyperram_memory_interface_hs	HyperRAM Memory Interface IP file
dvi_tx_top	DVI TX IP folder
gowin_pllvr	PLLVR IP folder
syn_code	Sync timing generation module folder

The Ref. Design folder contains the netlist file, user reference design, constraints file, top-level file and the project file, etc.

Table 6-6 Gowin SDRAM RefDesign Folder List

Name	Description
video_top.v	The top module of reference design
testpattern.v	Test pattern generation module
dk_video.cst	Project physical constraints file
dk_video.sdc	Project timing constraints file

Name	Description
video_frame_buffer	Video Frame Buffer IP folder
SDRAM_controller_top_SIP	SDRAM Memory Interface IP file
gowin_rpll	rpll IP folder
syn_code	Sync timing generation module folder

The Ref. Design folder contains the netlist file, user reference design, constraints file, top-level file and the project file, etc.

Table 6-7 Gowin VFB UHS2PSRAM RefDesign Folder List

Name	Description
video_top.v	The top module of reference design
testpattern.v	Test pattern generation module
dk_video.cst	Project physical constraints file
dk_video.sdc	Project timing constraints file
video_frame_buffer	Video Frame Buffer IP folder
uhs2_psram_memory_interface	UHS2 PSRAM Memory Interface IP file
dvi_tx_top	DVI TX IP folder
gowin_pll	PLL IP folder
syn_code	Sync timing generation module folder

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