



Gowin Scaler Lite Down & Up IP User Guide

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Revision History

Date	Version	Description
03/12/2021	1.0E	Initial version published.
10/12/2021	1.1E	Zoom Direction and Line Buffer Depth options added.
03/17/2022	1.2E	● Zoom ratio added. ● Scaler algorithm added.

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1 About This Guide

1.1 Purpose

The purpose of Gowin Scaler Lite Down & Up IP is to help you learn the features and usage of Gowin Scaler Lite Down & Up IP by providing the descriptions of features, functions, configurations and, reference design, etc.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS821, GW1NS series of FPGA Products Data Sheet](#)
- [DS861, GW1NSR series of FPGA Products Data Sheet](#)
- [DS881, GW1NSER series of FPGA Products Data Sheet](#)
- [DS891, GW1NRF series of FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [DS971, GW2AN-18X/9X Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
VESA	Video Electronics Standards Association
VS	Vertical Sync

Terminology and Abbreviations	Meaning
HS	Horizontal Sync
DE	Data Enable
IP	Intellectual Property

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Overview

The Video Scaler is a common function in image processing to convert the input image from one resolution to another for output, meanwhile meeting the requirement of real-time video input and output. Scaler Lite IP is used for bilinear algorithm and low scaling. Scaler Lite Down IP implements the scaling down function and Scaler Lite Up IP implements the scaling up function.

Table 2-1 Gowin Scaler Lite Down & Up IP

Gowin Scaler Lite Down & Up IP	
Logic Resource	Please refer to Table 2-2 and Table 2-3.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.8.05 Beta and above)

2.2 Features

- Supports VESA RGB 24 bits, MIPI RGB 32 bits, MIPI RGB 64 bits data formats.
- Supports 2:1, 3:2, 4:3, 5:4, 6:5, 7:6, 8:7 scaling down.
- Supports 1:2, 2:3, 3:4, 4:5, 5:6, 6:7, 7:8 scaling up.

2.3 Resource Utilization

Scaler Lite Down and Scaler Lite Up can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW1NR-9 series of FPGA as an instance, the resource utilization of Gowin Scaler Lite Down & Up IP is as shown in Table 2-2 and Table 2-3.

Table 2-2 Scaler Lite Down Resource Utilization

Zoom Ratio	Device	Scaler Algorithm	Data Format	Buffer Depth	Register	LUT	BSRAM
5:4	GW1NR-9	Simple Without DSP	24 bits	2048	132	285	3
5:4			32 bits	2048	173	491	4
5:4			64 bits	2048	275	1018	4

Table 2-3 Scaler Lite Up Resource Utilization

Zoom Ratio	Device	Scaler Algorithm	Data Format	Buffer Depth	Register	LUT	BSRAM
4:5	GW1NR-9	Simple Without DSP	24 bits	2048	136	191	3
4:5			32 bits	2048	206	495	4
4:5			64 bits	2048	300	937	4

3 Functional Description

3.1 System Block Diagram

Gowin Scaler Lite Down & Up IP includes Scaler Lite Down IP and Scaler Lite Up IP, and the block diagram is as shown in Figure 3-1 and Figure 3-2.

Figure 3-1 Scaler Lite Down Block Diagram

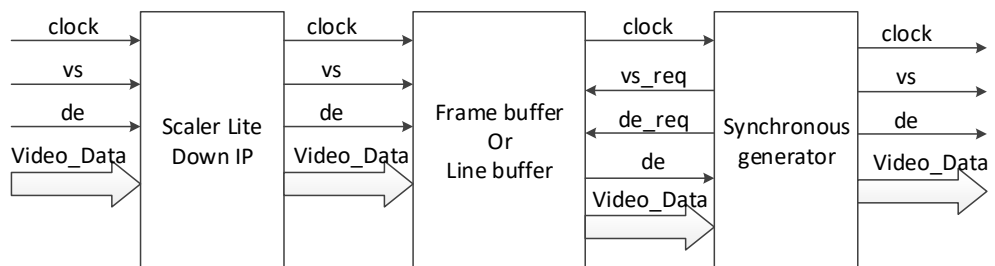
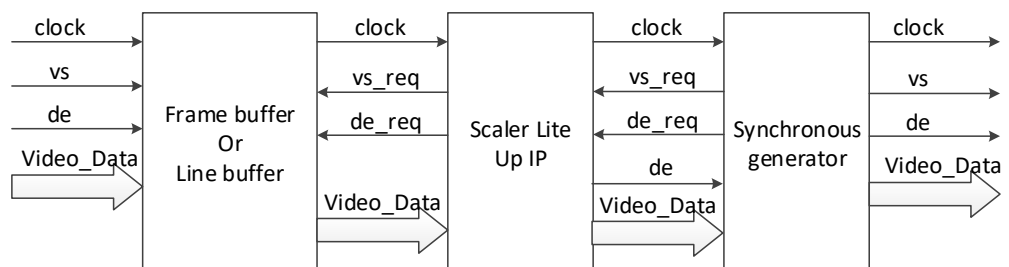


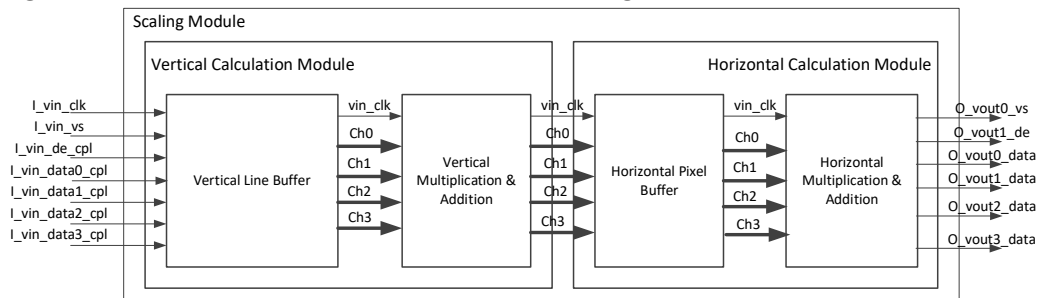
Figure 3-2 Scaler Lite Up Block Diagram



3.2 Implementation Diagram

3.2.1 Scaler Lite Down

Figure 3-3 Scaler Lite Down Implementation Diagram



Scaler Lite Down IP mainly consists of a scaling module, which contains a vertical calculation module and a horizontal calculation module.

After zooming out the image, the output bandwidth is smaller than the input bandwidth, so using the input pixel clock as the system processing clock completely can meet the requirement.

The data processing flow is as follows:

1. Firstly, line buffers the input data. Taking a line length of 2048 as an instance to calculate, the capacity of one BSRAM is 8 bits x 2048, according to the input data bit width, 24 bits need 3 BSRAMs, and 32 bits need 4 BSRAMs.
2. Then the two lines of data are weighted according to the zoom ratio. Since only one line is buffered, each new input line is first multiplied and added with the previous buffered line, while the data of the new input line is buffered into the BSRAM to replace the data of the previous line.
3. Then the data after the operation is delayed, and then the weighting of two adjacent points is calculated according to the zoom ratio. If it is VESA RGB 24 bits data format, each clock corresponds to 24 bits, and each clock still corresponds to 24 bits after the operation. If it is MIPI 32 bits data format, each clock corresponds to 32 bits, and each clock still corresponds to 32 bits after the operation. If it is MIPI 64 bits data format, each clock corresponds to 64 bits, and each clock still corresponds to 64 bits after the operation.
4. Finally, the data is output directly, and no additional cache is needed.

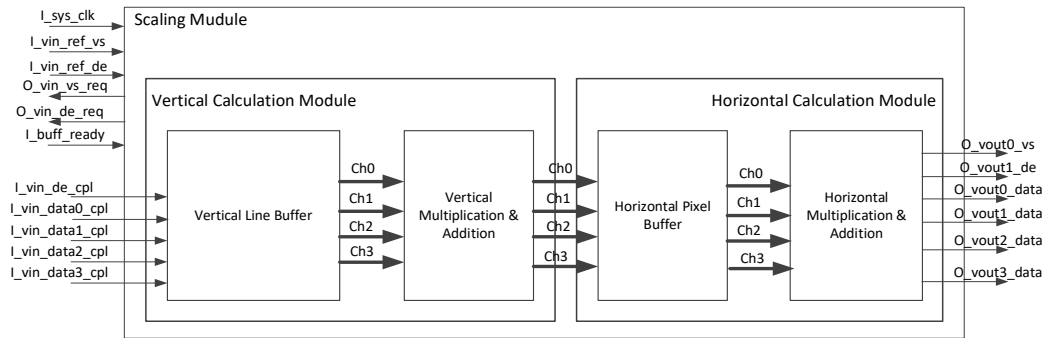
Note!

- Each line of the input data valid signal DE must be continuous.
- The output is not evenly spaced from line to line because the data decreases after the zooming out. And within a line, the number of points is reduced, and the output DE is not continuous.
- The input VS signal must be positive and the output VS signal is a positive pulse signal with 4096 clock cycles in width.

- Depending on the capacity of the BSRAM, the length of the input image line is limited to less than or equal to the line buffer depth, and the length must be an integer multiple of the zoom ratio. Depending on the capacity of the selected chip, the line buffer depth can be divided into three types, 1024, 2048 or 4096. And it must be an integer multiple of 4 when the data format is MIPI 32 bits and an integer multiple of 8 when the data format is MIPI 64 bits.
- The image height is unlimited, but must be an integer multiple of the zoom ratio.

3.2.2 Scaler Lite Up

Figure 3-4 Scaler Lite Up Implementation Diagram



The basic structure of Scaler Lite Up and Scaler Lite Down is similar, but there is a difference in the port.

After zooming in, the output bandwidth is increased, so the output pixel clock is used as the processing clock. In addition, since the data of the same line will be processed multiple times for the zoom in operation, it is not possible to complete the scaling operation with just one line of cache. Therefore, it is necessary to have a multi-line buffer or an external memory to provide the buffer function. In the block diagram, the external memory is used with the Video Frame Buffer to realize the scaling function.

The data processing flow is as follows.

1. The output timing generation module will output the VS signal and DE signals to Scaler Lite Up IP, which will output the scaling data. After receiving VS and DE signals, the IP will regenerate the read enable signal de_req from Frame Buffer or Line Buffer according to the calculation of data timing and read data from Buffer.
2. After the data outputs to Scaler Lite Up IP from Frame Buffer or Line Buffer, it first enters the line buffer. With a line length of 2048, the capacity of one BSRAM is 8 bits x 2048, and according to the input data bit width, 24 bits need 3 BSRAMs, and 32 bits need 4 BSRAMs.
3. Then the two lines of data are weighted according to the zoom in ratio. Since only one line is buffered, each new input line is first multiplied and added with the previous buffered line, while the data of the new input line is buffered into the BSRAM to replace the data of the previous line.
4. Then the data after the operation is delayed several cycles, and then the weighting of two adjacent points is calculated according to the zoom ratio. If it is VESA RGB 24 bits data format, each clock corresponds to 24 bits, and each clock still corresponds to 24 bits after the operation. In it is MIPI 32 bits data format, each clock corresponds

to 32 bits, and each clock still corresponds to 32 bits after the operation. In it is MIPI 64 bits data format, each clock corresponds to 64 bits, and each clock still corresponds to 64 bits after the operation.

5. Finally, the data is output directly, and no additional cache is needed.

Note!

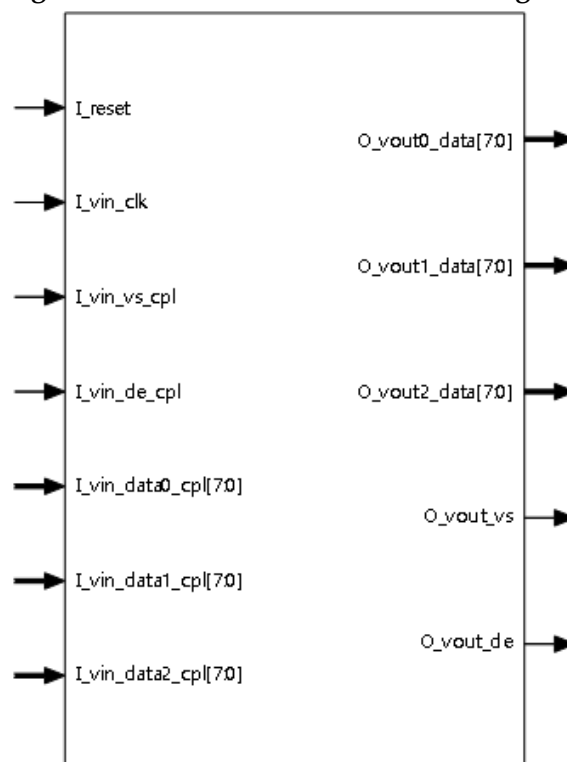
- After the read data enable signal `de_req` is output to the Video Frame Buffer, the return data must be delayed at least 2 cycles before outputs to the Scaler Lite Up IP. The exact number of cycles delayed must be specified and used as a parameter in the Scaler Lite Up IP generation.
- The output DE is continuous and can be used to drive the display directly.
- Input VS signal, and `iit` must be positive.
- Depending on the capacity of the BSRAM, the length of the input image line is limited to less than or equal to the line buffer depth, and the length must be an integer multiple of the zoom ratio. Depending on the capacity of the selected chip, the line buffer depth can be divided into three types, 1024, 2048 or 4096. And it must be an integer multiple of 4 when the data format is MIPI 32 bits and an integer multiple of 8 when the data format is MIPI 64 bits.
- The length of the input image graphics is less than or equal to 8192 and the length must be an integer multiple of the zoom ratio.

3.3 Port List

3.3.1 Scaler Lite Down Port

The IO ports of Gowin Scaler Lite Down IP are shown in Figure 3-5.

Figure 3-5 Scaler Lite Down IO Port Diagram



Ports vary slightly depending on the parameters.

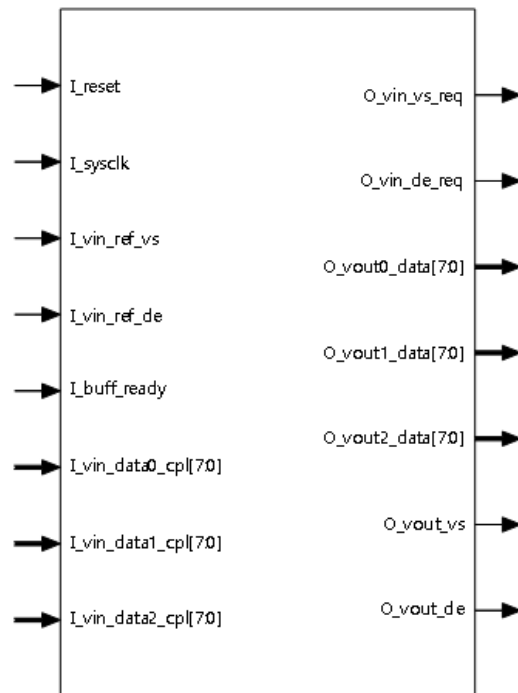
The details of I/O ports of Gowin Scaler Lite Down IP are shown in Table 3-1.

Table 3-1 Gowin Scaler Lite Down IP Port List

No.	Signal Name	I/O	Description	Note
1	I_reset	I	Reset signal, active-high	The I/O of all the signals takes Scaler Lite Down IP as reference.
2	I_vin_clk	I	Input pixel clock.	
3	I_vin_vs_cpl	I	Input vs signal, positive	
4	I_vin_de_cpl	I	Input data enable de signal	
5	I_vin_data0_cpl	I	Input video data signal	
6	I_vin_data1_cpl	I	Input video data signal	
7	I_vin_data2_cpl	I	Input video data signal	
8	I_vin_data3_cpl	I	Input video data signal, valid only in MIPI data format.	
9	O_vval_de	O	Debug option; vertical calculation outputs de signal	
10	O_vval_data0	O	Debug option; vertical calculation outputs data signal	
11	O_vval_data1	O	Debug option; vertical calculation outputs data signal	
12	O_vval_data2	O	Debug option; vertical calculation outputs data signal	
13	O_vval_data3	O	Debug option; vertical calculation outputs data signal, valid only in MIPI format	
14	O_vout_vs	O	Output video vs signal, positive	
15	O_vout_de	O	Output video data enable de signal	
16	O_vout0_data	O	Output video data signal	
17	O_vout1_data	O	Output video data signal	
18	O_vout2_data	O	Output video data signal	
19	O_vout3_data	O	Output video data signal, valid only in MIPI data format	

3.3.2 Scaler Lite Up Port

The IO ports of Gowin Scaler Lite Up IP are shown in Figure 3-6.

Figure 3-6 Scaler Lite Up IO Port Diagram

Ports vary slightly depending on the parameters.

The details of I/O ports of Gowin Scaler Lite Up IP are shown in Table 3-2.

Table 3-2 Gowin Scaler Lite Up IP Port List

No.	Signal Name	I/O	Description	Note
1	I_reset	I	Reset signal, active-high.	The I/O of all the signals takes Scaler Lite Up IP as reference.
2	I_sys_clk	I	System working clock	
3	I_vin_ref_vs	I	Reference vs signal, positive	
4	I_vin_ref_de	I	Reference data enable de signal	
5	O_vin_vs_req	O	Output vs request signal, positive; 2 cycles delay than I_vin_ref_vs, output to buffer module	
6	O_vin_de_req	O	Data enable de request signal, output to buffer module	
7	I_buf_fstline_rdy	I	First line in buffer ready signal	
8	I_vin_data0_cpl	I	Input video data signal	
9	I_vin_data1_cpl	I	Input video data signal	
10	I_vin_data2_cpl	I	Input video data signal	
11	I_vin_data3_cpl	I	Input video data signal, valid only in MIPI data format	
12	O_vout_vs	O	Output video vs signal, positive	
13	O_vout_de	O	Output video data enable de signal	

No.	Signal Name	I/O	Description	Note
14	O_vout0_data	O	Output video data signal	
15	O_vout1_data	O	Output video data signal	
16	O_vout2_data	O	Output video data signal	
17	O_vout3_data	O	Output video data signal, valid only in MIPI data format	

3.4 Parameter Configuration

3.4.1 Scaler Lite Down Parameter

Table 3-3 Scaler Lite Down Parameter

No.	Name	Range	Default	Description
1	Data Format	VESA_RGB_24BIT, MIPI4LANES_RGB_32BIT, MIPI 4 lanes RGB 64bits	VESA_RGB_24BIT	Input Data Format
2	Zoom Ratio	2:1, 3:2, 4:3, 5:4	2:1	Zoom Ratio
3	Zoom Direction	Both/Vertical/Horizontal	Both	Zoom Direction - Both: Zoom in both vertical and horizontal directions - Vertical: Zoom in vertical direction only - Horizontal: Zoom in horizontal direction only
4	Line Buffer Depth	1024/2048/4096	2048	Buffer depth of one line
5	Vertical Data Enable	Yes/No	No	Debug option, available only for bi-direction; display the data calculated vertically when enabled.
6	Scaler Algorithm	Simple Without DSP/Bilinear With DSP	Simple Without DSP	Scaler Algorithm

3.4.2 Scaler Lite Up Parameter

Table 3-4 Scaler Lite Up Parameter

No.	Name	Range	Default	Description
1	Data Format	VESA_RGB_24BIT, MIPI4LANES_RGB_32BIT, MIPI 4 lanes RGB 64bits	VESA_RGB_24BIT	Input Data Format
2	Zoom Ratio	1:2, 2:3, 3:4, 4:5	1:2	Zoom Ratio
3	Input	1~4096	1280	Input horizontal resolution

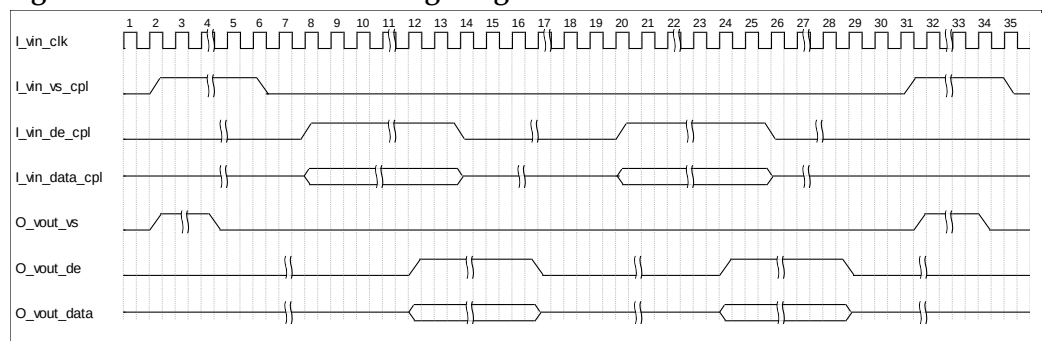
No.	Name	Range	Default	Description
	Frame Width			- It must be an integer multiple of 4 when data format is MIPI4LANES_RGB_32 BIT. - It must be an integer multiple of 8 when data format is MIPI4LANES_RGB_64 BIT.
4	Input Frame Height	1~8192	720	Input vertical resolution
5	Fetch Data Delay Value	2~16	2	Fetch data delay value
6	Zoom Direction	Both/Vertical/Horizontal	Both	Zoom Direction - Both: Zoom in both vertical and horizontal directions - Vertical: Zoom in vertical direction only - Horizontal: Zoom in horizontal direction only
7	Line Buffer Depth	1024/2048/4096	2048	Buffer depth of one line
8	Scaler Algorithm	Simple Without DSP/Bilinear With DSP	Simple Without DSP	Scaler Algorithm

3.5 Timing Description

This chapter describes the timing of Gowin Scaler Lite Down & Up IP.

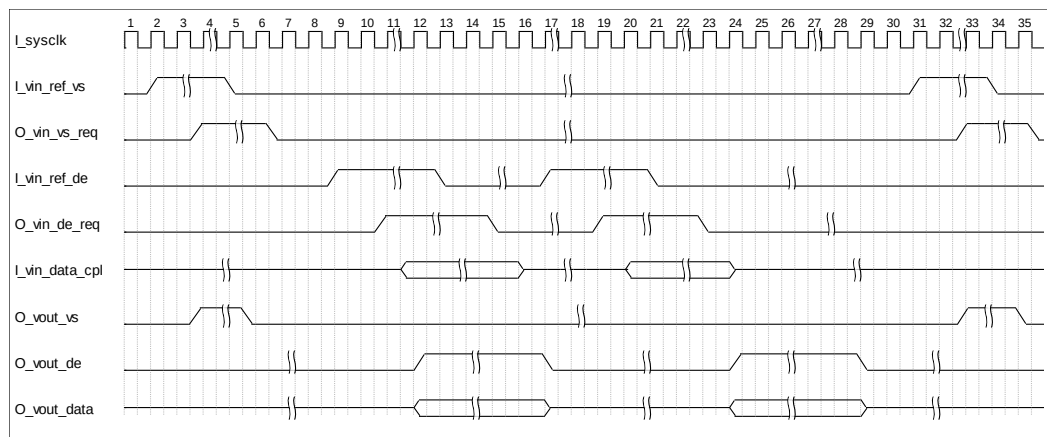
The video timing diagram of Scaler Lite Down is as shown in Figure 3-7.

Figure 3-7 Video Interface Timing Diagram of Scaler Lite Down



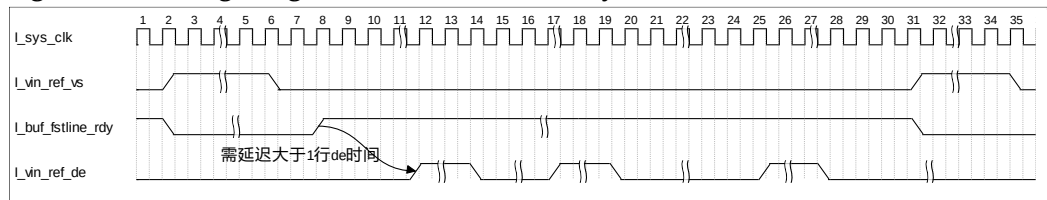
The video timing diagram of Scaler Lite Up is as shown in Figure 3-8.

Figure 3-8 Video Interface Timing Diagram of Scaler Lite Up



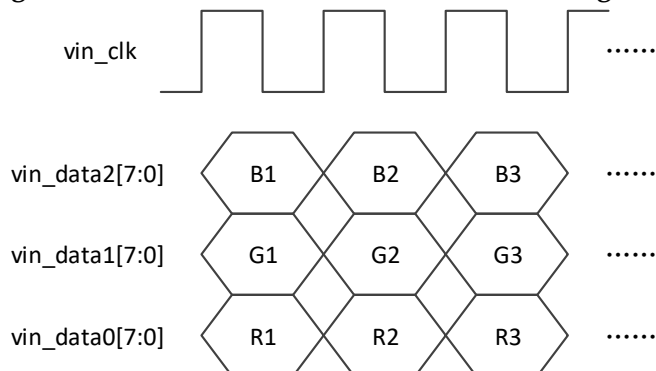
I_buf_fstline_rdy signal timing diagram is as shown in Figure 3-9.

Figure 3-9 Timing Diagram of I_buf_fstline_rdy

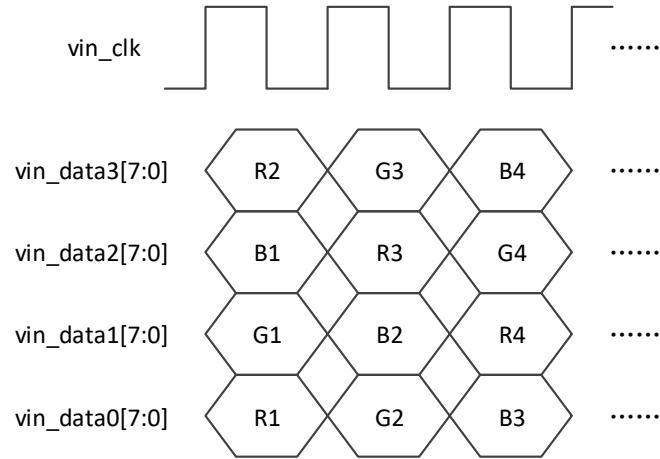


VESA_RGB_24BIT data format diagram is as shown in Figure 3-10.

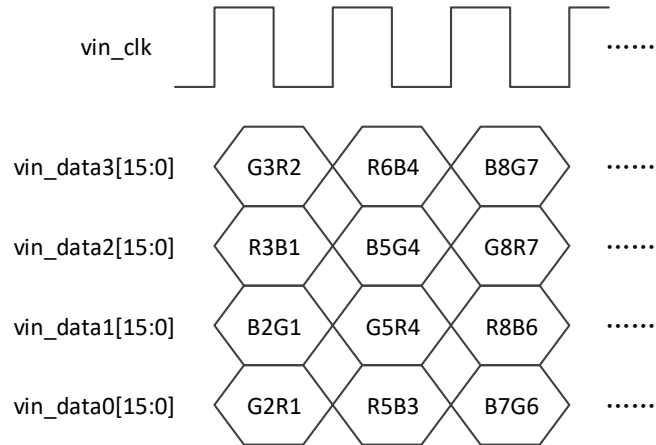
Figure 3-10 VESA_RGB_24BIT Data Format Diagram



MIPI4LANES_RGB_32BIT data format diagram is as shown in Figure 3-11.

Figure 3-11 MIPI4LANES_RGB_32BIT Data Format Diagram

VESA_RGB_24BIT data format diagram is as shown in Figure 3-12.

Figure 3-12 VESA_RGB_24BIT Data Format Diagram

4 Interface Configuration

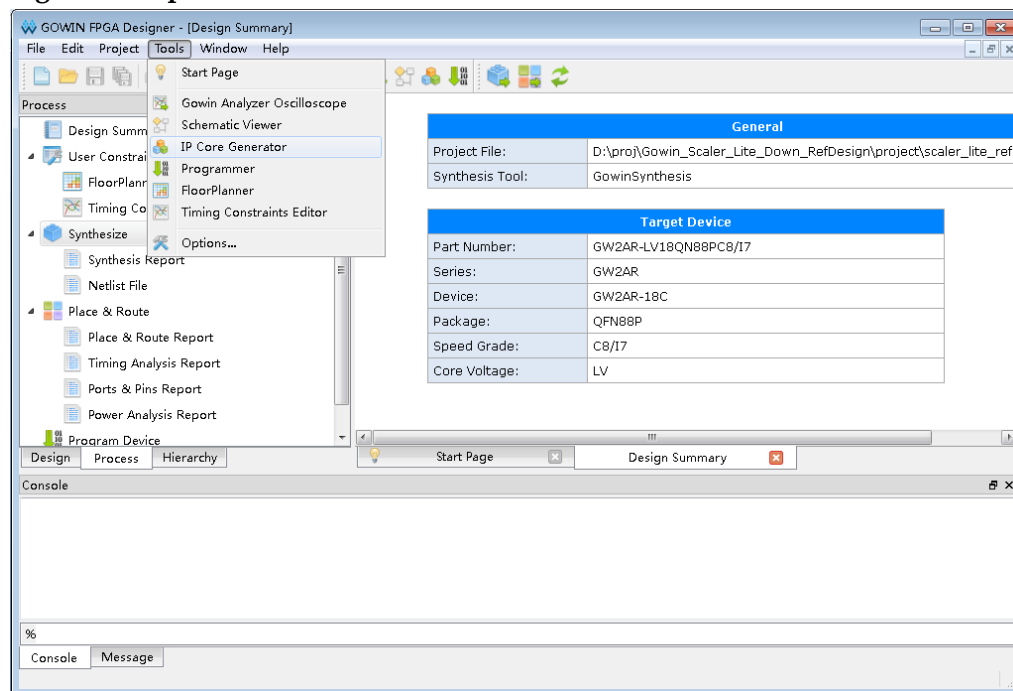
You can use IP core generator tool in Gowin Software to call and configure Scaler Lite Down IP and Scaler Lite Up IP.

4.1 Scaler Lite Down IP Configuration

1. Open IP Core Generator

After creating the project, click the "Tools" tab in the upper left, click "IP Core Generator" from the drop-down list to open Gowin IP Core Generator, as shown in Figure 4-1.

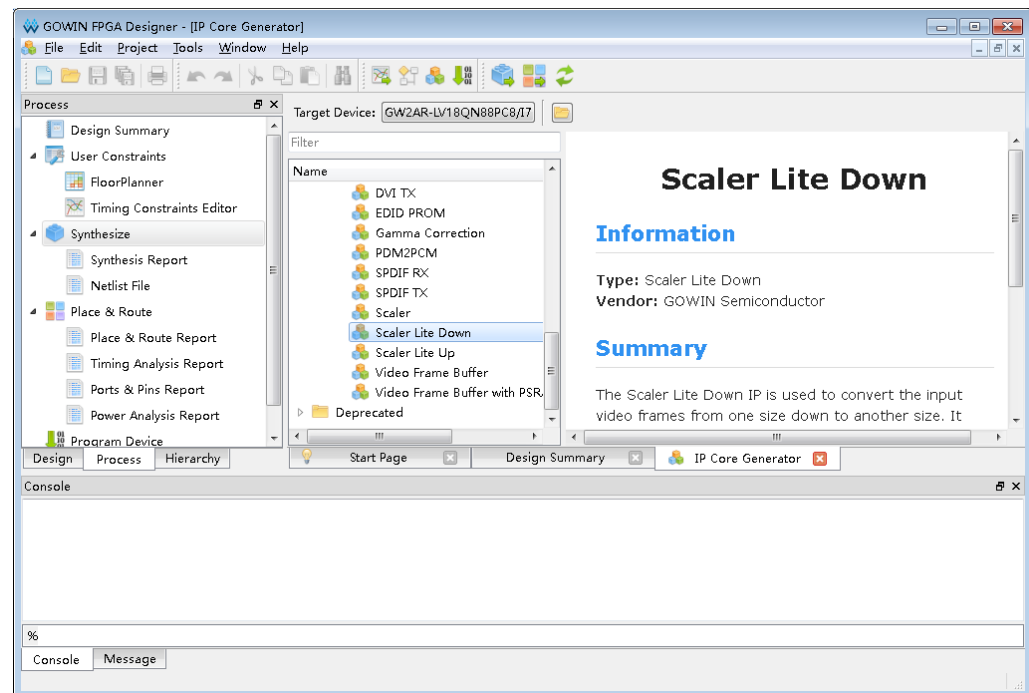
Figure 4-1 Open IP Core Generator



2. Open Scaler Lite Down IP Core

Click "Multimedia" and double click "Scaler Lite Down" to open the configuration interface, as shown in Figure 4-2.

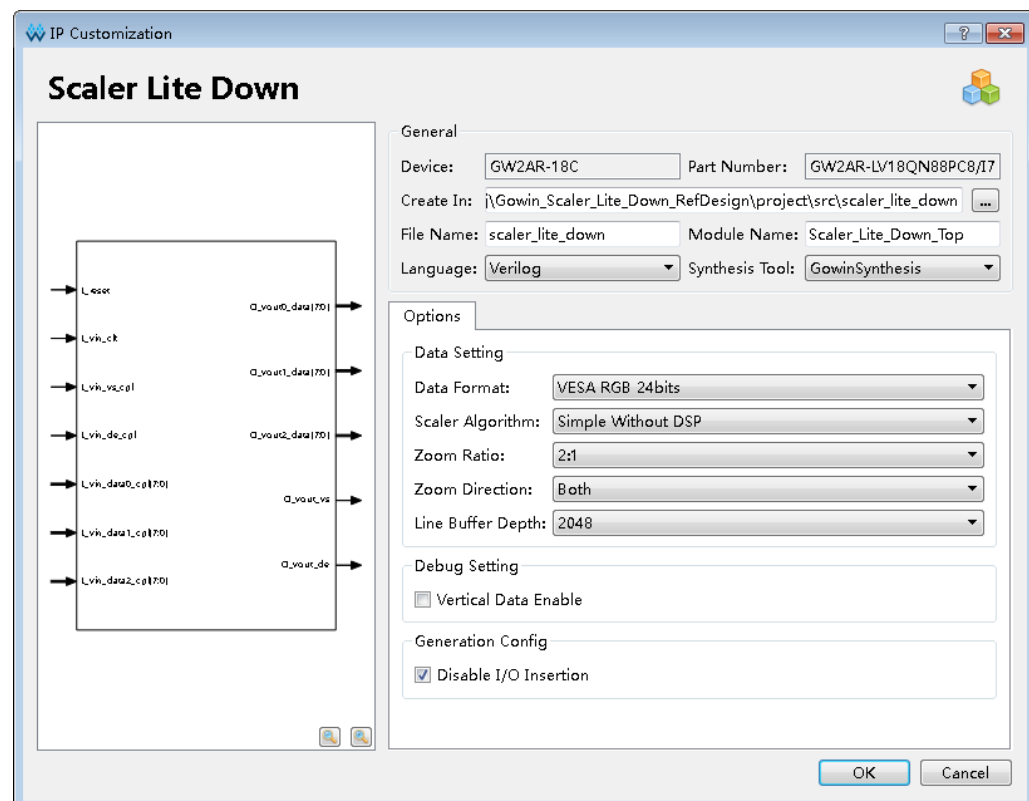
Figure 4-2 Open Scaler Lite Down IP Core



3. Scaler Lite Down IP Core Port Interface

On the left of the configuration interface is the port diagram of Scaler Lite Down IP core, as shown in Figure 4-3.

Figure 4-3 Scaler Lite Down IP Core Port Diagram



4. Configure Basic Information

See the project basic information in the configuration interface. Take GW2AR-18C and QFN88P package as an example. The "Module Name" displays the top-level file name of the generated project, and the default is "Scaler_Lite_Down_Top". You can modify the name. The "File Name" displays the folder generated by the IP core, which contains the files required by Scaler Lite Down IP core, and the default is "scaler_lite_down". You can modify the path. "Create In" displays the path of IP core folder. The default is "\\project path\\src\\scaler_lite_down". You can modify the path.

Figure 4-4 Basic Information Configuration Interface

General

Device: GW2AR-18C Part Number: GW2AR-LV18QN88PC8/I7

Create In: \\Gowin_Scaler_Lite_Down_RefDesign\\project\\src\\scaler_lite_down ...

File Name: scaler_lite_down Module Name: Scaler_Lite_Down_Top

Language: Verilog Synthesis Tool: GowinSynthesis

5. Options

In the tab, you need to configure information about parameters such as the data format used by Scaler Lite Down.

Figure 4-5 Options

Options

Data Setting

Data Format: VESA RGB 24bits

Scaler Algorithm: Simple Without DSP

Zoom Ratio: 2:1

Zoom Direction: Both

Line Buffer Depth: 2048

Debug Setting

☐ Vertical Data Enable

Generation Config

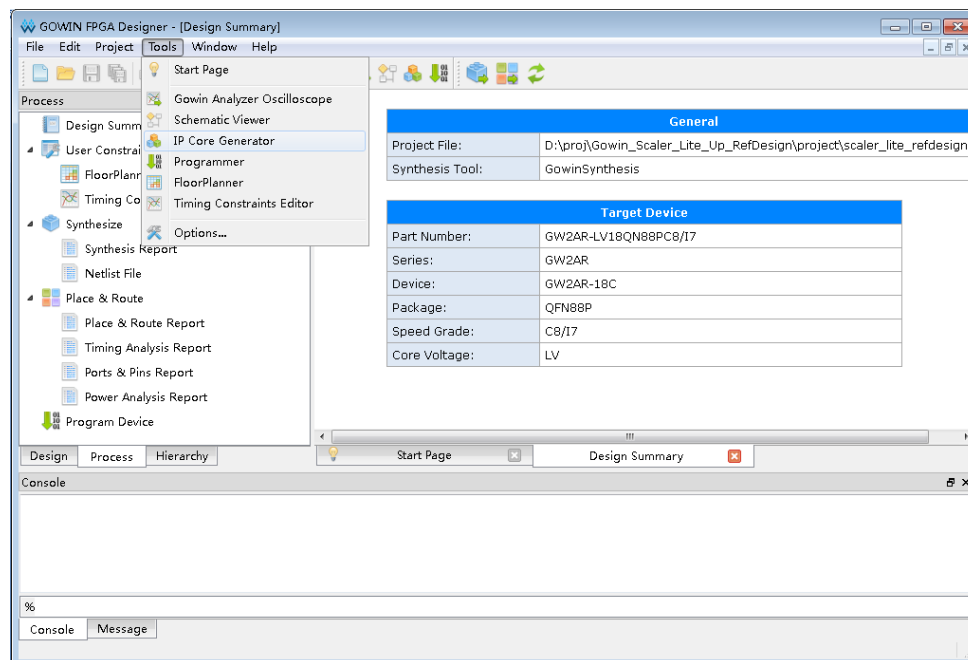
☒ Disable I/O Insertion

4.2 Scaler Lite Up IP Configuration

1. Open IP Core Generator

After creating the project, click the "Tools" tab in the upper left, click "IP Core Generator" from the drop-down list to open Gowin IP Core Generator, as shown in Figure 4-6.

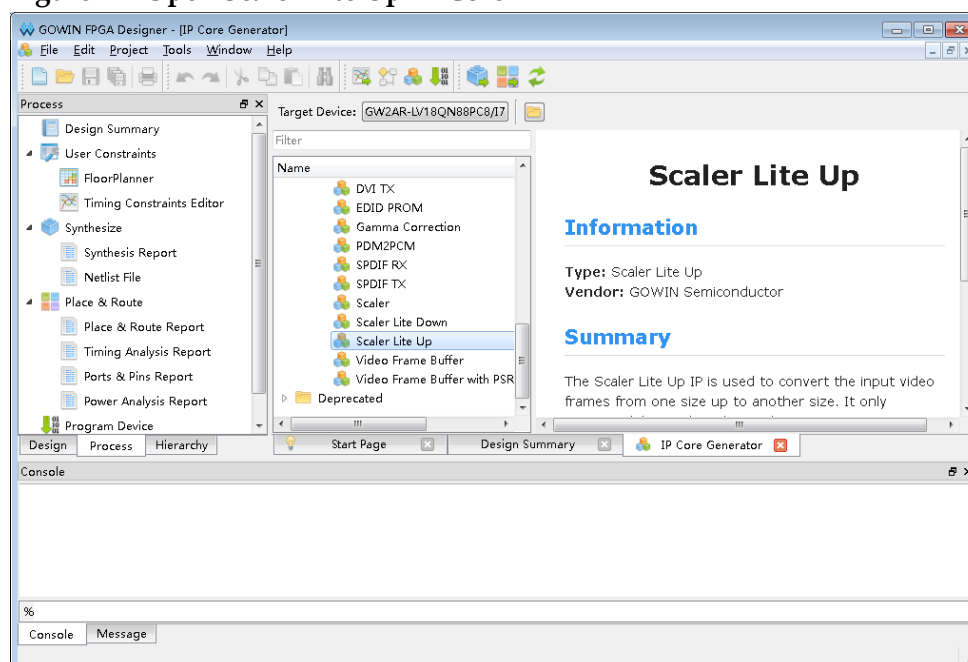
Figure 4-6 Open IP Core Generator



2. Open Scaler Lite Up IP Core

Click "Multimedia" and double click "Scaler Lite Up" to open the configuration interface, as shown in Figure 4-7.

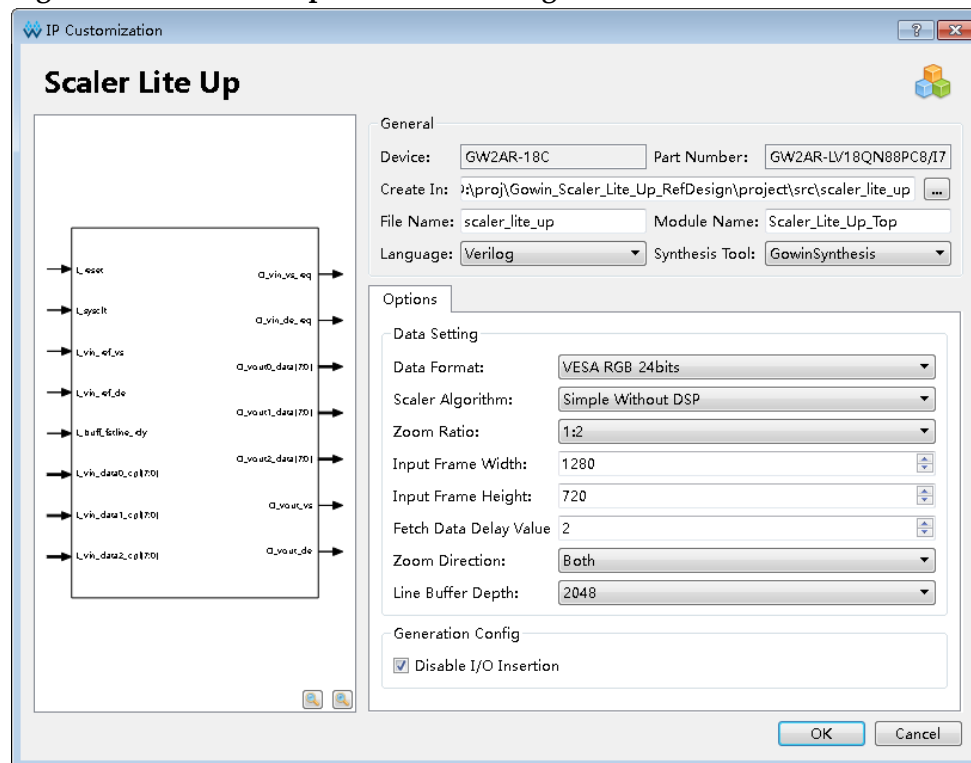
Figure 4-7 Open Scaler Lite Up IP Core



3. Scaler Lite Up IP Core Port Interface

On the left of the configuration interface is the port diagram of Scaler Lite Up IP core, as shown in Figure 4-8.

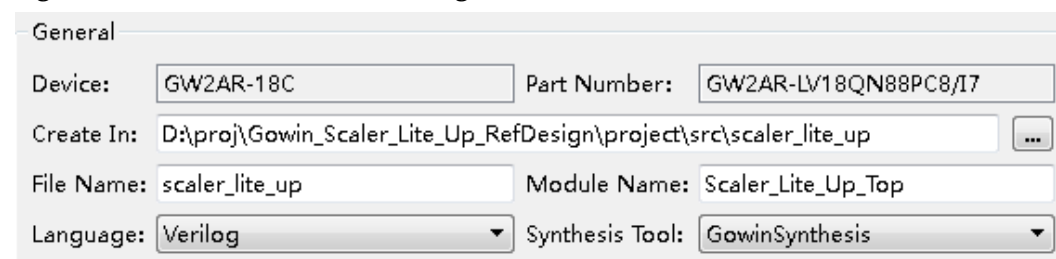
Figure 4-8 Scaler Lite Up IP Core Port Diagram



4. Configure Basic Information

See the project basic information in the configuration interface. Take GW2AR-18C and QFN88P package as an example. The "Module Name" displays the top-level file name of the generated project, and the default is "Scaler_Lite_Up_Top". You can modify the name. The "File Name" displays the folder generated by the IP core, which contains the files required by Scaler Lite Up IP core, and the default is "scaler_lite_up". You can modify the path. "Create In" displays the path of IP core folder. The default is "\project path\src\scaler_lite_up". You can modify the path.

Figure 4-9 Basic Information Configuration Interface



5. Options

In the tab, you need to configure information about parameters such as the data format used by Scaler Lite Up.

Figure 4-10 Options

Options

Data Setting

Data Format: VESA RGB 24bits

Scaler Algorithm: Simple Without DSP

Zoom Ratio: 1:2

Input Frame Width: 1280

Input Frame Height: 720

Fetch Data Delay Value: 2

Zoom Direction: Both

Line Buffer Depth: 2048

Generation Config

☒ Disable I/O Insertion

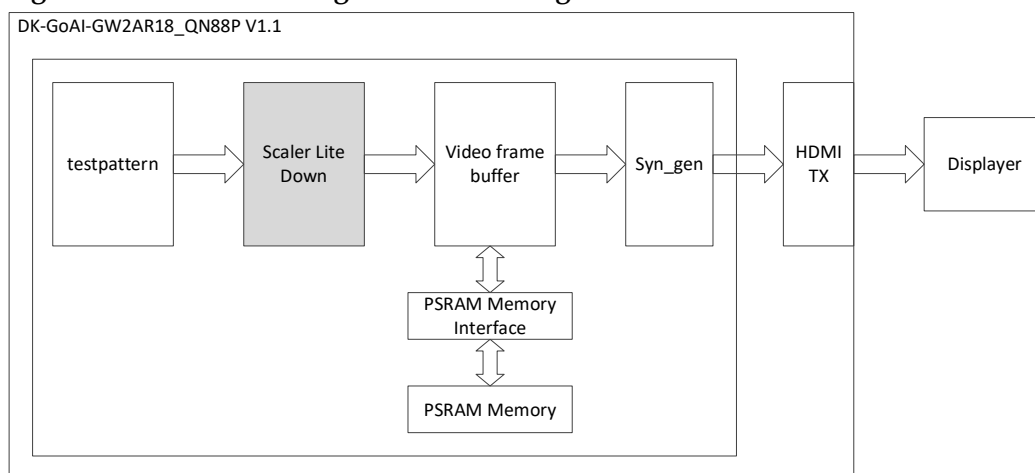
5 Reference Design

This chapter introduces the structure and usage of Gowin Scaler Lite Down & Up IP reference design. Please see [Reference Design](#) for details at Gowinsemi website.

5.1 Design Instance 1

Take DK-GoAI-GW2AR18_QN88P V1.1 as an example, the diagram is as shown in Figure 5-1. For the details of DK-GoAI-GW2AR18_QN88P V1.1, you can click [here](#).

Figure 5-1 Reference Design Instance 1 Diagram

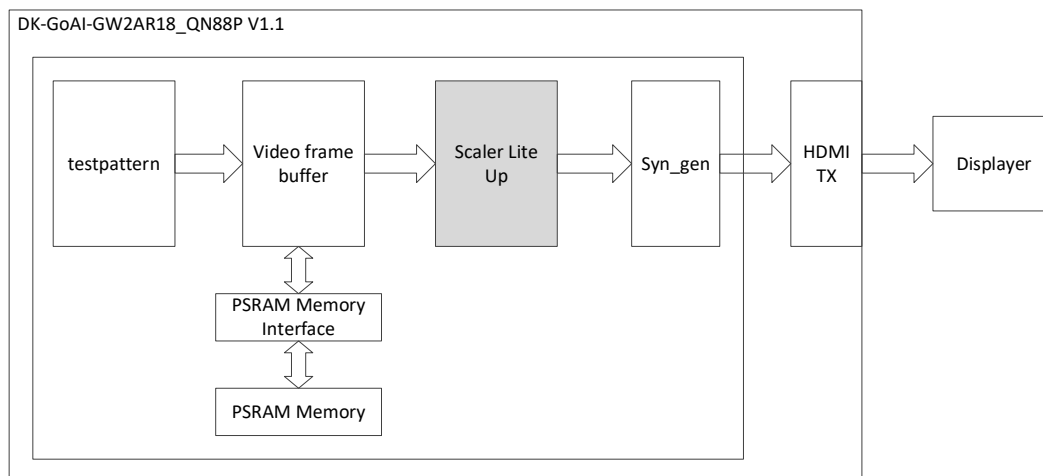


In the reference design instance 1, the testpattern module generates the test pattern video signal, which is scaled down by the Scaler Lite Down module at a fixed ratio and then input to the Video Frame Buffer for video data buffer. The Video Frame Buffer is connected to the PSRAM controller IP, the syn_gen module generates output video timing, reads video data from Video Frame Buffer, and then outputs to HDMI (J4) port, which is connected to the display via HDMI cable, that is, you can see the generated test pattern after zooming out. Test pattern includes color pattern, grid pattern, grayscale pattern and checkerboard pattern.

5.2 Design Instance 2

Take DK-GoAI-GW2AR18_QN88P V1.1 as an example, the diagram is as shown in Figure 5-2.

Figure 5-2 Reference Design Instance 2 Diagram



In the reference design example 2, the testpattern module generates the test pattern video signal, which is first input to the Video Frame Buffer for video data buffer. The Video Frame Buffer is connected to the PSRAM controller IP, the syn_gen module generates the output video timing, which is output to the Scaler Lite Up module. Scaler Lite Up module reads video data from Video Frame Buffer and then scaling up it at a fixed ratio, and finally the data is output to HDMI (J4) port, which is connected to the display via HDMI cable, that is, you can see the generated test pattern after zooming in. Test pattern includes color pattern, grid pattern, grayscale pattern and checkerboard pattern.

6 File Delivery

The delivery file for Gowin Scaler Lite Down & Up IP includes documents, design source code and reference design.

6.1 Documents

The documents mainly contain the user guide in PDF.

Table 6-1 Documents List

Name	Description
IPUG772, Gowin Scaler Lite Down & Up IP User Guide	Gowin Scaler Lite Down & Up IP User Guide, namely this one

6.2 Design Source Code (Encryption)

The encrypted code file contains the Gowin Scaler Lite IP RTL encrypted code which is used for GUI in order to cooperate with Gowin software to generate the IP core required by users.

Table 6-2 Design Source Code List of Scaler Lite Down

Name	Description
scaler_lite_down.v	The top-level file of the IP core, which provides users with interface information, encrypted.

Table 6-3 Design Source Code List of Scaler Lite Up

Name	Description
scaler_lite_up.v	The top-level file of the IP core, which provides users with interface information, encrypted.

6.3 Reference Design

The Gowin Scaler Lite Down RefDesign folder contains the netlist file for Gowin Scaler Lite Down IP, user reference design, constraints file, top-level file, and the project file, etc.

Table 6-4 Gowin Scaler Lite Down RefDesign File List

Name	Description
scaler_lite_test_top.v	The top module of reference design
scaler_lite_test_top.cst	Project physical constraints file

Name	Description
scaler_lite_test_top.sdc	Project timing constraints file
testpattern.v	Reference Design file
dvi_tx_top	DVI TX IP folder
gowin_rpll	rPLL IP folder
line_buffer	Line buffer folder
psram_memory_interface_hs	PSRAM Memory Interface IP folder
scaler_lite_down	Scaler Lite Down IP folder
syn_code	Syn timing generation module folder
video_frame_buffer	Video Frame Buffer IP folder

The Gowin Scaler Lite Up RefDesign folder contains the netlist file for Gowin Scaler Lite Up IP, user reference design, constraints file, top-level file, and the project file, etc.

Table 6-5 Gowin Scaler Lite Up RefDesign File List

Name	Description
scaler_lite_test_top.v	The top module of reference design
scaler_lite_test_top.cst	Project physical constraints file
scaler_lite_test_top.sdc	Project timing constraints file
testpattern.v	Reference Design file
dvi_tx_top	DVI TX IP folder
gowin_rpll	rPLL IP folder
psram_memory_interface_hs	PSRAM Memory Interface IP folder
scaler_lite_up	Scaler Lite Up IP folder
syn_code	Syn timing generation module folder
video_frame_buffer	Video Frame Buffer IP folder

