



Gowin MIPI DSI/CSI-2 Transmitter IP User Guide

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Revision History

Date	Version	Description
10/24/2023	1.0E	Initial version published.
12/29/2023	1.1E	● DSI/CSI-2 frame structure diagram added. ● Descriptions of 3.3.6 DSI/CSI-2 TX Timing Diagram updated.
07/31/2024	1.1.1E	1.2 Related Documents updated.
05/30/2025	1.1.2E	Descriptions of "Generation Config" option added.

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1 About This Guide

1.1 Purpose

The purpose of Gowin MIPI DSI/CSI-2 Transmitter IP User Guide is to help users learn the features and usage of Gowin MIPI DSI/CSI-2 Transmitter IP by providing descriptions of the product overview, functions, GUI, etc.

1.2 Related Documents

1. The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:
 - [IPUG948, Gowin MIPI IP User Guide](#)
 - [DS100, GW1N series of FPGA Products Data Sheet](#)
 - [DS117, GW1NR series of FPGA Products Data Sheet](#)
 - [DS821, GW1NS series of FPGA Products Data Sheet](#)
 - [DS861, GW1NSR series of FPGA Products Data Sheet](#)
 - [DS841, GW1NZ series of FPGA Products Data Sheet](#)
 - [DS102, GW2A series of FPGA Products Data Sheet](#)
 - [DS226, GW2AR series of FPGA Products Data Sheet](#)
 - [DS971, GW2AN-18X & 9X Data Sheet](#)
 - [DS976, GW2AN-55 Data Sheet](#)
 - [DS961, GW2ANR series of FPGA Products Data Sheet](#)
 - [DS1228, Arora V FPGA Products Overview](#)
 - [DS981, Arora V 138K & 75K FPGA Products Data Sheet](#)
 - [DS1225, Arora V 60K FPGA Products Data Sheet](#)
 - [DS1103, Arora V 25K FPGA Products Data Sheet](#)

- [DS1118, Arora V 15K FPGA Products Data Sheet](#)
 - [SUG100, Gowin Software User Guide](#)
2. MIPI Alliance Specification for D-PHY, Version 1.1 November 7, 2011, www.mipi.org
 3. MIPI Alliance Specification for Display Serial Interface, Version 1.1 November 22, 2011, www.mipi.org
 4. MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2), Version 1.1, July 18, 2012, www.mipi.org

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
CSI	Camera Serial Interface
DSI	Display Serial Interface
DT	Data Type
ECC	Error Correction Code
EoT	End of Transmission
EoTP	End of Transmission Packet
HBP	Horizontal Back Porch
HFP	Horizontal Front Porch
HSA	Horizontal Sync Active
HSE	Horizontal Sync End
HSS	Horizontal Sync Start
IP	Intellectual Property
LP	Low Power
LUT	Look-up Table
MIPI	Mobile Industry Processor Interface
VBP	Vertical Back Porch
VC	Virtual Channel
VFP	Vertical Front Porch
VSA	Vertical Sync Active
VSE	Vertical Sync End

Terminology and Abbreviations	Meaning
VSS	Vertical Sync Start

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Product Overview

2.1 Product Overview

Gowin MIPI DSI/CSI-2 Transmitter IP receives byte-aligned pixel streams and synchronization control signals, and composes pixel data frames and synchronization control frames in accordance with the DSI/CSI-2 protocol and user-configured parameters, and then drives the Gowin MIPI D-PHY TX Advance IP interface to realize MIPI DSI/CSI-2 D-PHY transmission.

The current version simplifies the transmission logic. In DSI mode, it temporarily supports only single-packet mode. Similar to CSI-2 mode, it sends only one short packet or one long packet in a single transmission, which reduces resource utilization.

Table 2-1 Gowin MIPI DSI/CSI-2 Transmitter IP Overview

Gowin MIPI DSI/CSI-2 Transmitter IP	
Logic Resource	See Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9.Beta-3 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features

- Complies with MIPI DSI V1.1 and MIPI CSI-2 V1.1 standards
- Supports MIPI D-PHY TX input with 1, 2, 3, or 4 data lanes
- Supports MIPI D-PHY TX mode with 8:1 and 1:16
- Supports various data types (DT) with different virtual channel (VC) identifiers
- Supports ECC generation for packet headers
- Supports CRC generation for the data byte stream (optional)
- Supports continuous clock mode (non-continuous clock mode is currently not supported)
- Supports Low Power (LP) mode during vertical and horizontal blank interval
- Supports the insertion of End of Transmission Packet (EoTP) short packets as defined in the MIPI DSI standard
- Supports three video modes as defined in the MIPI DSI standard
 - Non-burst mode with sync pulses
 - Non-burst mode with sync events
 - Burst mode

2.3 Resource Utilization

Taking Gowin GW2A-18 series of FPGA as an instance, the resource utilization of Gowin MIPI DSI/CSI-2 Transmitter IP is as shown in Table 2-2. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades.

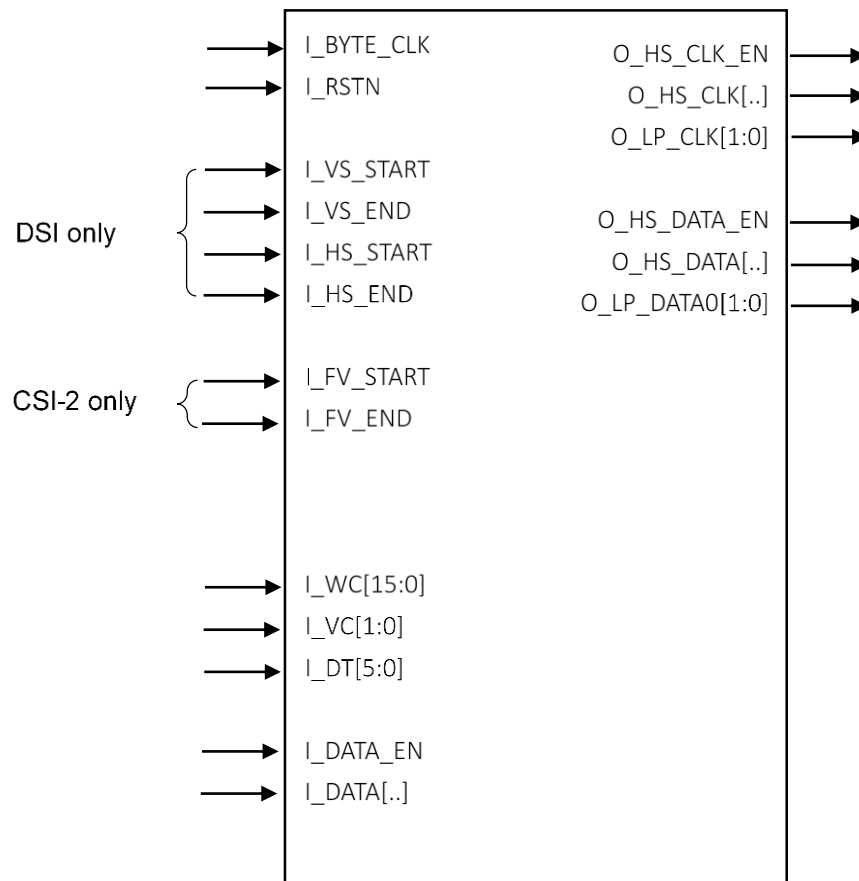
Table 2-2 Gowin MIPI DSI/CSI-2 Transmitter IP Resource Utilization Based on GW2A-18

Parameter Configuration	Resource Utilization			
	LUTs	REGs	SSRAM	BSRAM
DSI,8:1, 1-Lane	597	348	4	1
DSI,8:1, 2-Lane	883	406	4	2
DSI,8:1, 3-Lane	1108	453	4	2
DSI,8:1, 4-Lane	1292	471	4	2
DSI,16:1, 1-Lane	887	405	4	2
DSI,16:1, 2-Lane	1274	468	4	2
DSI,16:1, 3-Lane	1629	523	4	2
DSI,16:1, 4-Lane	2449	621	4	2

3 Functional Description

3.1 Top Block Diagram

Figure 3-1 Top Block Diagram of Gowin MIPI DSI/CSI-2 Transmitter IP



3.2 Port Description

Table 3-1 Gowin MIPI DSI/CSI-2 Transmitter IP I/O Ports

Signal	I/O	Description
I_BYTE_CLK	Input	Operating clock
I_RSTN	Input	Asynchronous reset signal, active-low
I_VS_START	Input	In DSI mode, vertical synchronization starts, active-high
I_VS_END	Input	In DSI mode, vertical synchronization ends, active-high
I_HS_START	Input	In DSI mode, horizontal synchronization starts, active-high
I_HS_END	Input	In DSI mode, horizontal synchronization ends, active-high
I_FV_START	Input	In CSI-2 mode, field valid starts, active-high
I_FV_END	Input	In CSI-2 mode, field valid ends, active-high
I_DATA_EN	Input	Byte data enable, active-high
I_DATA[..]	Input	Byte data, and the bit width depending on number of D-PHY lanes and modes (8:1/16:1)
		Number of lanes 8:1 mode 16:1 mode
		1 8 16
		2 16 32
		3 24 48
		4 32 64
I_WC[15:0]	Input	Packet header word count field for counting the number of long packet bytes
I_VC[1:0]	Input	Packet header virtual channel ID field
I_DT[5:0]	Input	Packet header data type field
O_HS_CLK_EN	Output	Clock enable in HS mode, active-high
O_HS_CLK[..]	Output	Clock output in HS mode When "MIPI TX D-PHY Mode" is set to 8:1, the width is 8 bits, such as 8'b01010101; When "MIPI TX D-PHY Mode" is set to 16:1, the bit width is 8 bits, such as 16'b0101010101010101.
O_LP_CLK[1:0]	Output	Clock output in LP mode In the case where only the continuous clock mode is currently supported, a high-speed clock initialization

Signal	I/O	Description
		process of '11' → '01' → '00' will be output for a period of time after the reset signal is released
O_HS_DATA_EN	Output	Data enable in HS mode, active-high
O_HS_DATA0[..]	Output	Data output for channel #n in HS mode, $0 \leq n \leq 3$. When "MIPI TX D-PHY Mode" is set to 8:1, the bit width is 8; when set to 1:16, the bit width is 16; When "Number of TX Lanes" is set to 4, O_HS_DATA0~ O_HS_DATA3 ports all exist; when set to 3, only O_HS_DATA0~ O_HS_DATA2 ports exist; when set to 2, only O_HS_DATA0, O_HS_DATA1 ports exist; when set to 1, only O_HS_DATA0 port exists.
O_HS_DATA1[..]	Output	
O_HS_DATA2[..]	Output	
O_HS_DATA3[..]	Output	
O_LP_DATA0[1:0]	Output	Data output for channel #0 in LP mode

3.3 Timing Description

3.3.1 D-PHY HS Data Burst Transmission

Figure 3-2 HS Data Burst Transmission

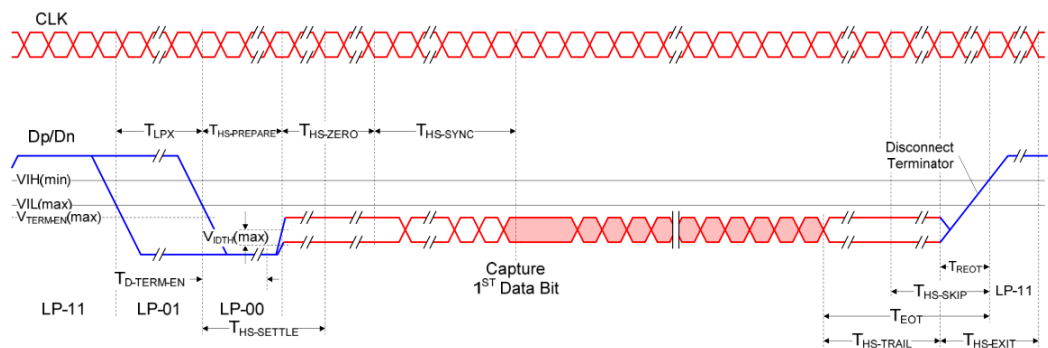
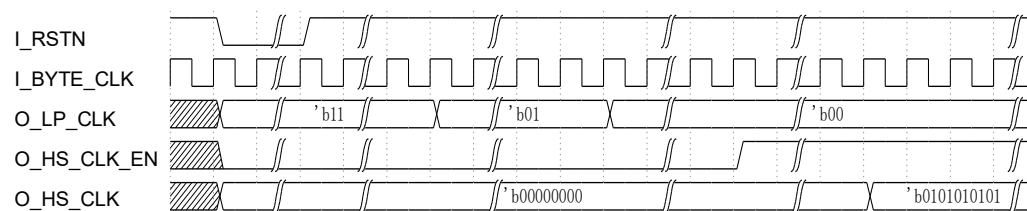


Figure 3-2 shows the sequence of events during the burst transmission of a packet, as described in MIPI Alliance Specification for D-PHY, Version 1.1 November 7, 2011, www.mipi.org.

3.3.2 Reset Timing Diagram

Figure 3-3 Reset Timing Diagram

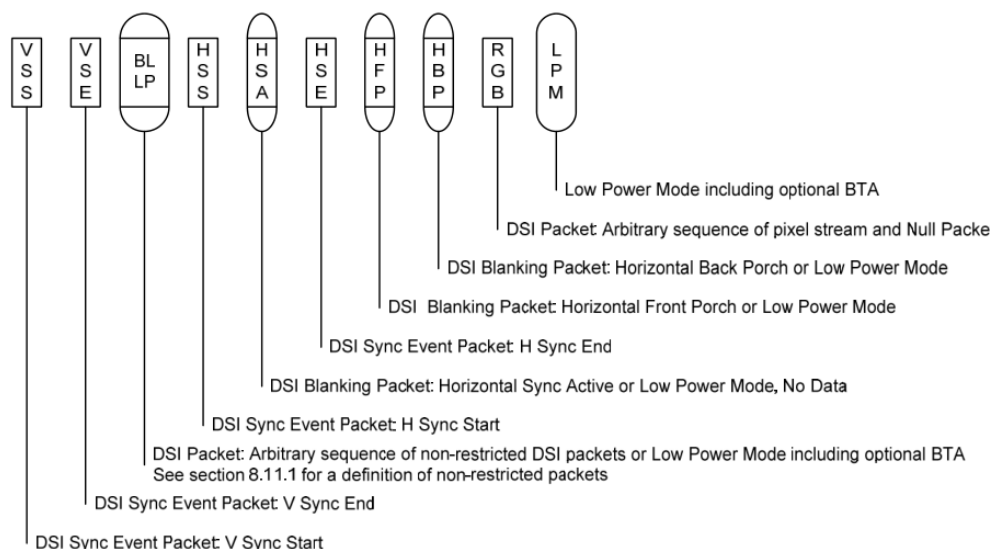


As shown in Figure 3-3, for a period of time after the reset signal is released, O_LP_CLK[1:0] will have an initialization process of outputting '11' → '01' → '00', before enabling O_HS_CLK_EN and outputting O_HS_CLK[...].

3.3.3 DSI Video Interface Mode

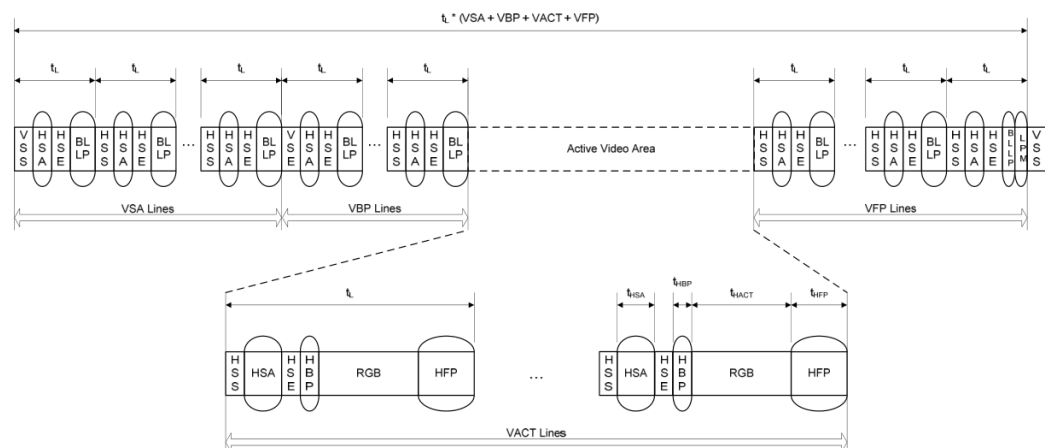
MIPI DSI V1.1 standard defines three video interface modes: Non-Burst Mode with Sync Pulses, Non-Burst Mode with Sync Events, and Burst Mode, and Figure 3-4 is the legend used in the figures from Figure 3-5 to Figure 3-7.

Figure 3-4 Timing Diagram of Video Interface



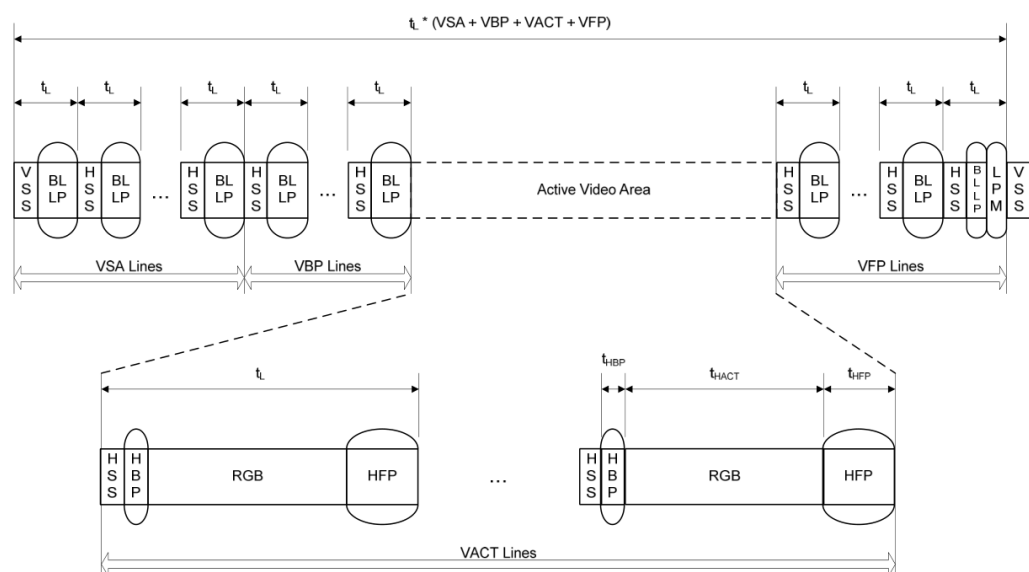
The first mode, Non-Burst Mode with Sync Pulses, is used with the goal of being able to accurately convey the timing of the DPI signal through the DSI line, including matching DPI pixel transfer rates and sync pulse widths. Therefore the synchronization period is determined using the start and end packets of the transmitted sync pulses, as shown in Figure 3-5.

Figure 3-5 Timing Diagram of Video Interface: Non-Burst Mode with Sync Pulses

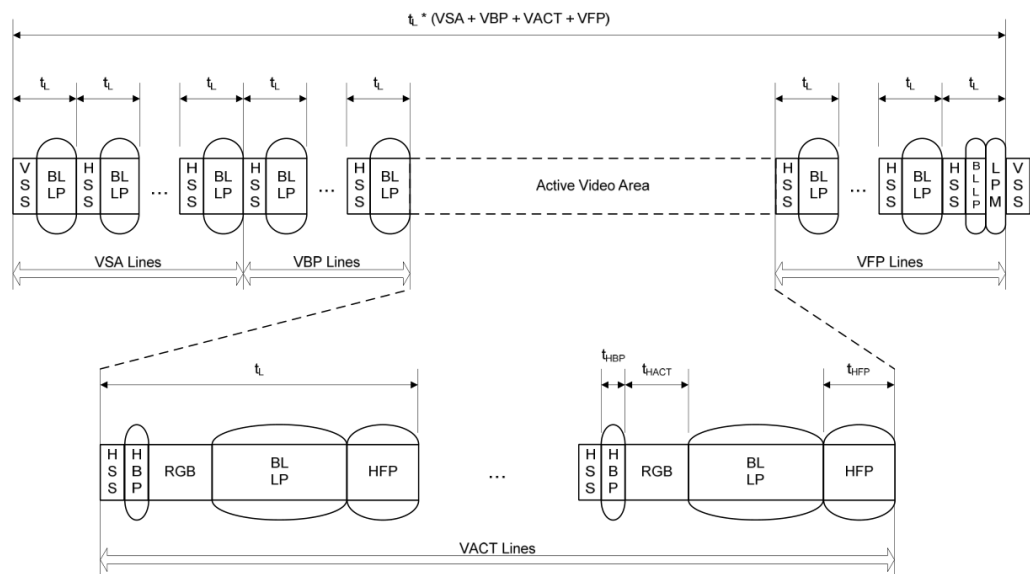


The second mode, Non-Burst Mode with Sync Events, is a simplification of the previous mode. Only the start packet (HSS, VSS) of each sync pulse is transmitted, and the peripheral device regenerates the sync pulse from each received sync event packet as needed, as shown in Figure 3-6.

Figure 3-6 Timing Diagram of Video Interface: Non-Burst Mode with Sync Events



The third mode, Burst Mode, similar to the second mode, also sends only the start packet of the sync pulse, as shown in Figure 3-7.

Figure 3-7 Timing Diagram of Video Interface: Burst Mode

Normally the periods of HSA, HBP, and HFP are filled by blanking packets whose length (including packet overhead) must match the periods specified in the peripheral datasheet. However, the current IP version sends only one short packet or one long packet in a single transmission, so the line blanking in the DPI timing has to be long enough to ensure that it can enter the HS mode and cut back to the LP mode in multiple rounds. The first mode needs to guarantee three rounds, and the other two modes need to guarantee two rounds.

3.3.4 DSI Frame Structure

Figure 3-8 Frame Structure Diagram for DSI Non-burst Mode with Sync Pulses

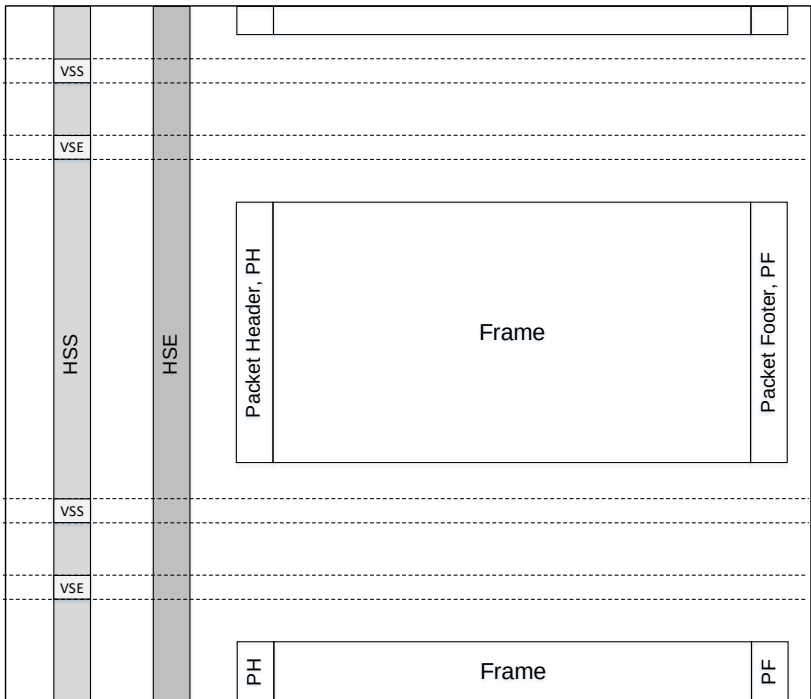
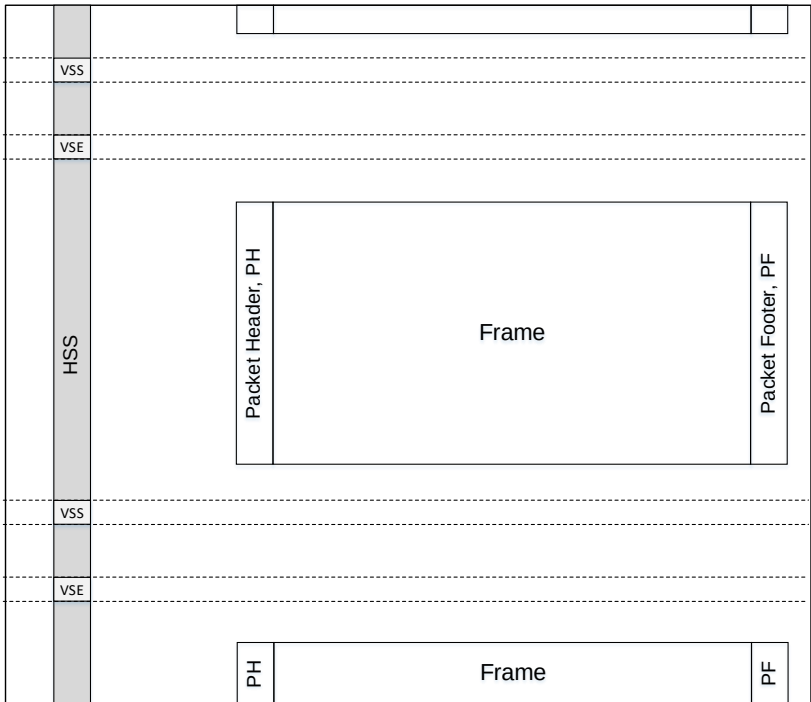
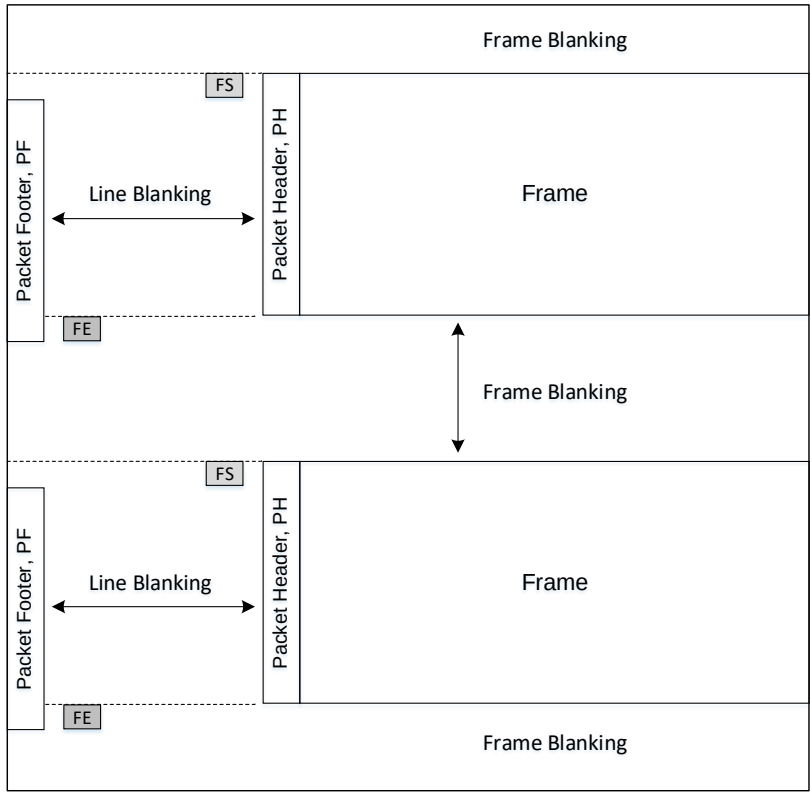


Figure 3-9 Frame Structure Diagram for DSI Non-burst Mode with Sync Events / Burst Mode



3.3.5 CSI-2 Frame Structure

Figure 3-10 CSI-2 Frame Structure Diagram



3.3.6 DSI/CSI-2 TX Timing Diagram

Figure 3-11 DSI/CSI-2 TX Timing Diagram

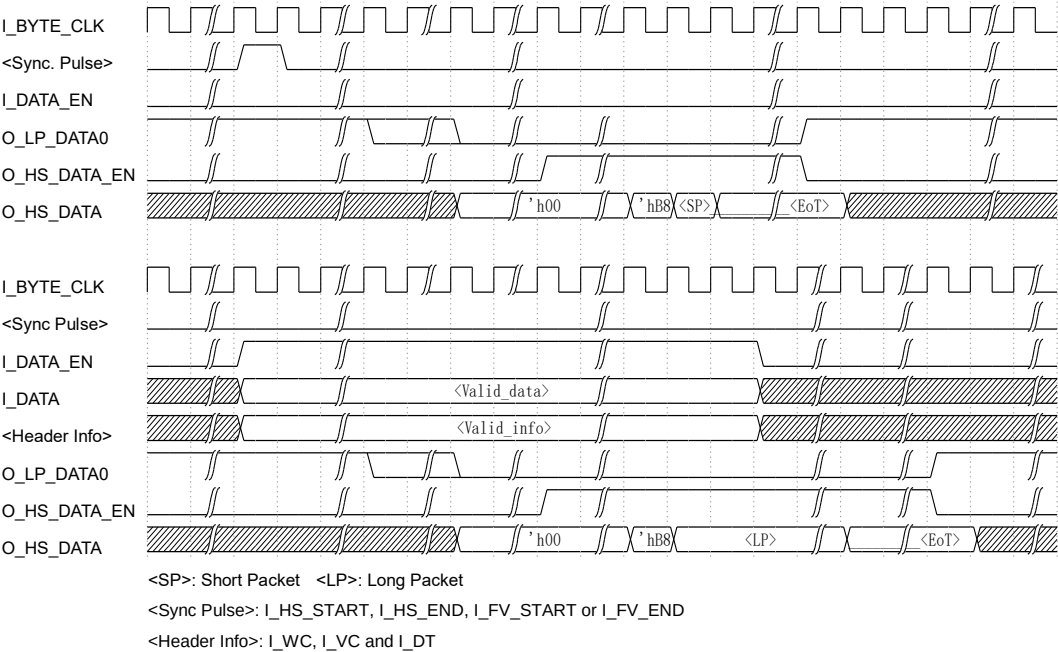
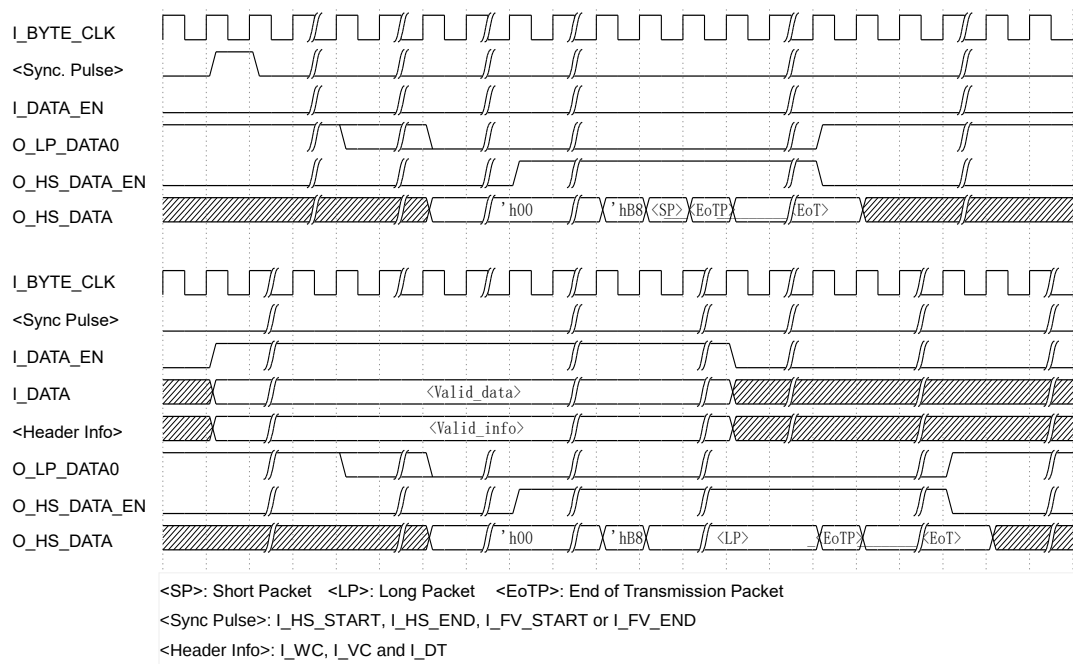
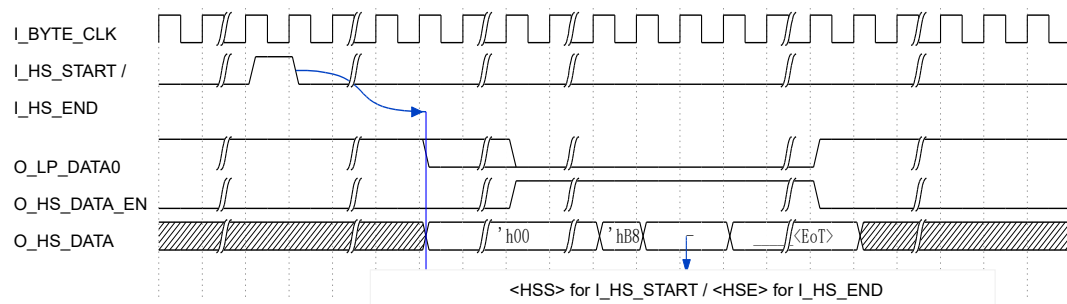
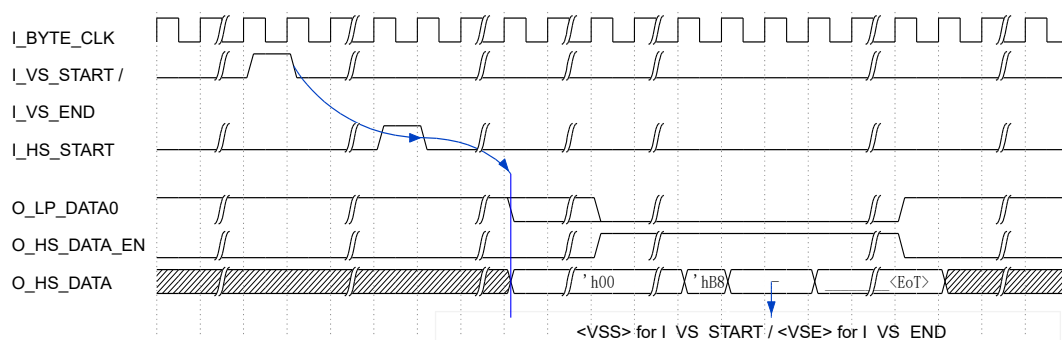


Figure 3-12 Timing Diagram for DSI TX with EoTP

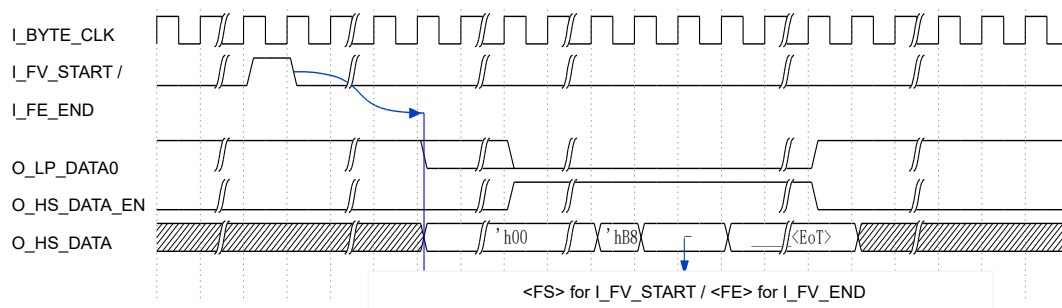
In DSI mode, each I_HS_START pulse triggers an HSS short packet. In Non-burst Mode with Sync Pulses, each I_HS_END pulse triggers an HSE short packet, as shown in Figure 3-13. In Non-burst Mode with Sync Events and Burst Mode, I_HS_END does not trigger any short packet.

Figure 3-13 DSI HSS/HSE Trigger Diagram

After the I_VS_START pulse, the HSS short packet triggered by first I_HS_START pulse is replaced by a VSS short packet. In Non-burst Mode with Sync Pulses, after the I_VS_END pulse, the HSS short packet triggered by first I_HS_START pulse is replaced by a VSE short packet, as shown in Figure 3-14.

Figure 3-14 DSI VSS/VSE Trigger Diagram

In CSI-2 mode, the I_FV_START pulse triggers an FS short packet, and the I_FV_END pulse triggers an FE short packet, as shown in Figure 3-15.

Figure 3-15 CSI-2 FS/FE Trigger Diagram

3.4 Parameter Configuration

Table 3-2 Gowin DSI/CSI-2 TX IP Parameters

Name	Range	Description
MIPI Interface Type	DSI or CSI-2	Specify MIPI interface type
MIPI D-PHY TX Mode	8:1 or 16:1	Specify D-PHY TX data mode
Number of TX Lanes	1, 2, 3, or 4	Number of D-PHY TX lanes
Generate Packet CRC	True / False	Specify whether to generate CRC for long packets; if False is selected, the CRC will be filled with 16'h55AA
DSI Video Mode	Burst Mode / Non-Burst Mode with Sync Pulses / Non-Burst Mode with Sync Events	Valid when MIPI Interface Type is DSI; specify DSI video interface mode
DSI with EoTP	True / False	Valid when MIPI Interface Type is

Name	Range	Description
		DSI; specify whether to use EoTP packets or not
I_BYTE_CLK Frequency	10.0 to 160.0MHz	Reference clock frequency for calculation of later time parameters
T _{LTX}	<value>	Time parameters required for TX D-PHY; for the details, see MIPI D-PHY Spec. V1.1 Section 6.9; These time parameters shall be converted to cycles based on the operating clock (I_BYTE_CLK).
T _{HS-PREPARE}	<value>	
T _{HS-ZERO}	<value>	
T _{HS-TAIL}	<value>	
T _{HS-EXIT}	<value>	
Generation Config	Checked/Unchecked	● If it is selected, the IP will not insert IBUF, OBUF, and IOBUF in the synthesized netlist. ● If it is not selected, the IP will insert IBUF, OBUF, and IOBUF in the synthesized netlist. ● The default setting is checked.

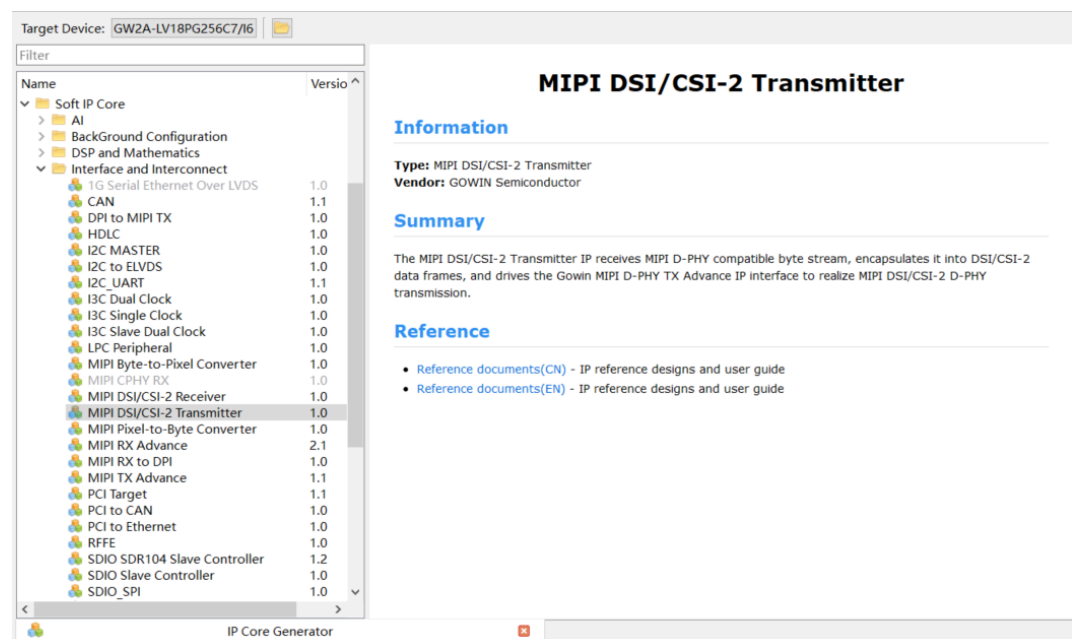
4 Interface Configuration

You can select "Tools" in Gowin Software to start the IP Core Generator to call and configure Gowin MIPI DSI/CSI-2 Transmitter IP.

1. Open IP Core Generator.

After creating the project, click the "Tools" tab in the upper left, click "IP Core Generator" from the drop-down list to open IP Core Generator. Click "Soft IP Core > Interface and Interconnect > MIPI DSI/CSI-2 Transmitter"; or enter "DSI/CSI-2 Transmitter" in the "Filter" search box to locate it quickly.

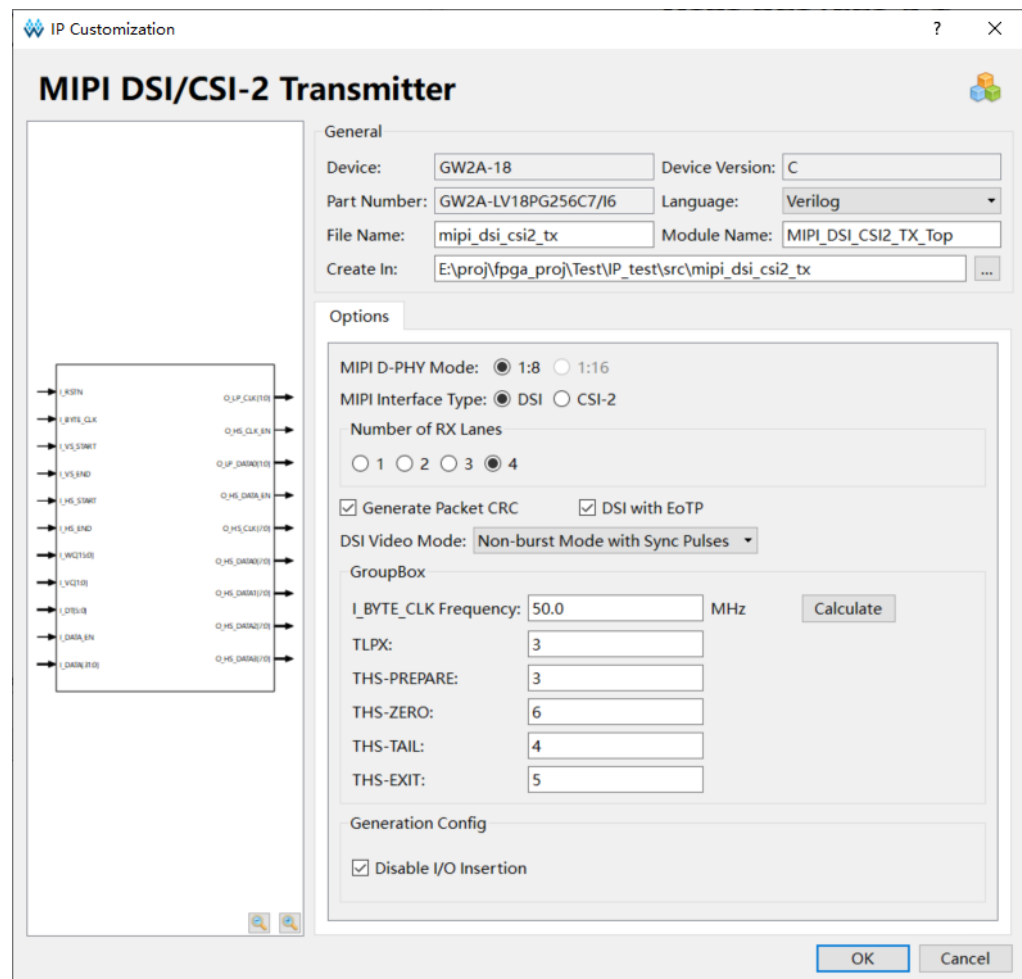
Figure 4-1 IP Core Generator



2. MIPI DSI/CSI-2 Transmitter IP Configuration Interface

Users can open the MIPI DSI/CSI-2 Transmitter IP configuration interface by double clicking the "MIPI DSI/CSI-2 Transmitter" item in the "IP Core Generator" tool interface. The port diagram is on the left, and the parameter configuration options (see [3.4 Parameter Configuration](#) for details) are on the right, as shown in Figure 4-2.

Figure 4-2 MIPI DSI/CSI-2 Transmitter IP Interface Configuration



3. Generation and Instantiation

After configuring the parameters according to requirements, click "OK" to generate MIPI DSI/CSI-2 Transmitter IP. As shown in Figure 4-3, here is an example of IP instantiation in the user's Verilog program.

Figure 4-3 MIPI DSI/CSI-2 Transmitter IP Instantiation

