



Gowin MIPI DSI/CSI-2 Receiver IP

User Guide

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Revision History

Date	Version	Description
10/24/2023	1.0E	Initial version published.
07/31/2024	1.0.1E	1.2 Related Documents updated.
05/30/2025	1.0.2E	Descriptions of "Generation Config" option added.

Contents

Contents	i
List of Figures	ii
List of Tables	iii
1 About This Guide	1
1.1 Purpose	1
1.2 Related Documents	1
1.3 Terminology and Abbreviations	2
1.4 Support and Feedback	2
2 Product Overview	3
2.1 Product Overview	3
2.2 Features	3
2.3 Resource Utilization	4
3 Functional Description	5
3.1 Top Block Diagram	5
3.2 Port Description	6
3.3 Timing Description	7
4 Interface Configuration	10

List of Figures

Figure 3-1 Top Block Diagram of Gowin MIPI DSI/CSI-2 Receiver IP	5
Figure 3-2 Output Timing Diagram.....	7
Figure 3-3 O_PAYLOAD_DV Timing Diagram	8
Figure 3-4 Timing Diagram for Two Sets of Packet Information Output	8
Figure 4-1 IP Core Generator	10
Figure 4-2 MIPI DSI/CSI-2 Receiver IP Interface Configuration.....	11
Figure 4-3 MIPI DSI/CSI-2 Receiver IP Instantiation	12

List of Tables

Table 1-1 Terminology and Abbreviations	2
Table 2-1 Gowin MIPI DSI/CSI-2 Receiver IP Overview.....	3
Table 2-2 Gowin MIPI DSI/CSI-2 Receiver IP Resource Utilization Based on GW2A-18	4
Table 3-1 Gowin MIPI DSI/CSI-2 Receiver IP I/O Ports	6
Table 4-1 Gowin DSI/CSI-2 Receiver IP Parameters	11

1 About This Guide

1.1 Purpose

The purpose of Gowin MIPI DSI/CSI-2 Receiver IP User Guide is to help users learn the features and usage of Gowin MIPI DSI/CSI-2 Receiver IP by providing descriptions of the product overview, functions, GUI, etc.

1.2 Related Documents

1. The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com
 - [IPUG948, Gowin MIPI D-PHY RX TX Advance IP User Guide](#)
 - [DS100, GW1N series of FPGA Products Data Sheet](#)
 - [DS117, GW1NR series of FPGA Products Data Sheet](#)
 - [DS821, GW1NS series of FPGA Products Data Sheet](#)
 - [DS861, GW1NSR series of FPGA Products Data Sheet](#)
 - [DS841, GW1NZ series of FPGA Products Data Sheet](#)
 - [DS102, GW2A series of FPGA Products Data Sheet](#)
 - [DS226, GW2AR series of FPGA Products Data Sheet](#)
 - [DS971, GW2AN-18X & 9X Data Sheet](#)
 - [DS976, GW2AN-55 Data Sheet](#)
 - [DS961, GW2ANR series of FPGA Products Data Sheet](#)
 - [DS1228, Arora V FPGA Products Overview](#)
 - [DS981, Arora V 138K & 75K FPGA Products Data Sheet](#)
 - [DS1225, Arora V 60K FPGA Products Data Sheet](#)
 - [DS1103, Arora V 25K FPGA Products Data Sheet](#)
 - [DS1118, Arora V 15K FPGA Products Data Sheet](#)

- [SUG100, Gowin Software User Guide](#)
- 2. MIPI Alliance Specification for D-PHY, Version 1.1 November 7, 2011, www.mipi.org
- 3. MIPI Alliance Specification for Display Serial Interface, Version 1.1 November 22, 2011, www.mipi.org
- 4. MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2), Version 1.1, July 18, 2012, www.mipi.org

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
CSI	Camera Serial Interface
DSI	Display Serial Interface
ECC	Error Correction Code
EoTP	End of Transmission packet
IP	Intellectual Property
LUT	Look-up Table
MIPI	Mobile Industry Processor Interface
NC	No Connect
WC	Word Count

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Product Overview

2.1 Product Overview

Gowin MIPI DSI/CSI-2 Receiver IP is designed to extract the Packet Header information and payload data from the channel-aligned MIPI byte data stream output from Gowin MIPI D-PHY RX Advance IP. The Packet Header information includes ECC, Data Type, and Word Count.

Table 2-1 Gowin MIPI DSI/CSI-2 Receiver IP Overview

Gowin MIPI DSI/CSI-2 Receiver IP	
Logic Resource	See Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9.Beta-3 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features

- Complies with MIPI DSI V1.1 and MIPI CSI-2 V1.1 standards
- Supports MIPI D-PHY RX input with 1, 2, 3, or 4 data lanes
- Supports MIPI D-PHY RX Mode with 1:8 and 1:16
- Supports four types of synchronous short packets as defined in the MIPI CSI-2 standard
- Supports the data long packet as defined in the MIPI CSI-2 standard

- Supports four types of synchronous short packets as defined in the MIPI DSI standard
- Supports the data long packet as defined in the MIPI DSI standard
- Supports End of Transmission Packet (EoTP) short packet as defined in the MIPI DSI standard
- Supports three video modes as defined in the MIPI DSI standard
 - Non-burst mode with sync pulses
 - Non-burst mode with sync events
 - Burst mode

2.3 Resource Utilization

Taking Gowin GW2A-18 series of FPGA as an instance, the resource utilization of Gowin MIPI DSI/CSI-2 Receiver IP is as shown in Table 2-2. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades.

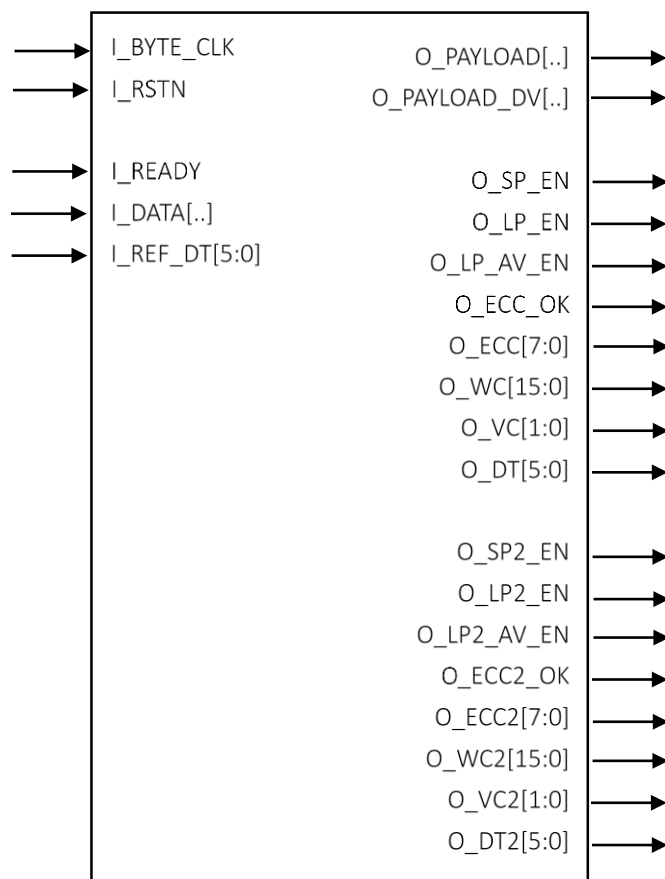
Table 2-2 Gowin MIPI DSI/CSI-2 Receiver IP Resource Utilization Based on GW2A-18

Parameter Configuration	Resource Utilization	
	LUTs	REGs
1:8, 1-Lane	150	149
1:8, 2-Lane	199	175
1:8, 3-Lane	244	201
1:8, 4-Lane	278	227
1:16, 1-Lane	218	184
1:16, 2-Lane	310	244
1:16, 3-Lane	1052	630
1:16, 4-Lane	1328	722

3 Functional Description

3.1 Top Block Diagram

Figure 3-1 Top Block Diagram of Gowin MIPI DSI/CSI-2 Receiver IP



The basic function of the Gowin MIPI DSI/CSI-2 Receiver IP is to extract control signals (Packet Header) and payload data from the D-PHY byte data stream. In the case of a 3-Lane or 4-Lane configuration with a 1:16 data mode, it is possible to extract two sets of control signals in a single clock cycle. Therefore, the output ports include the second set of

control signals. In other cases, the second set of control signals will not appear.

3.2 Port Description

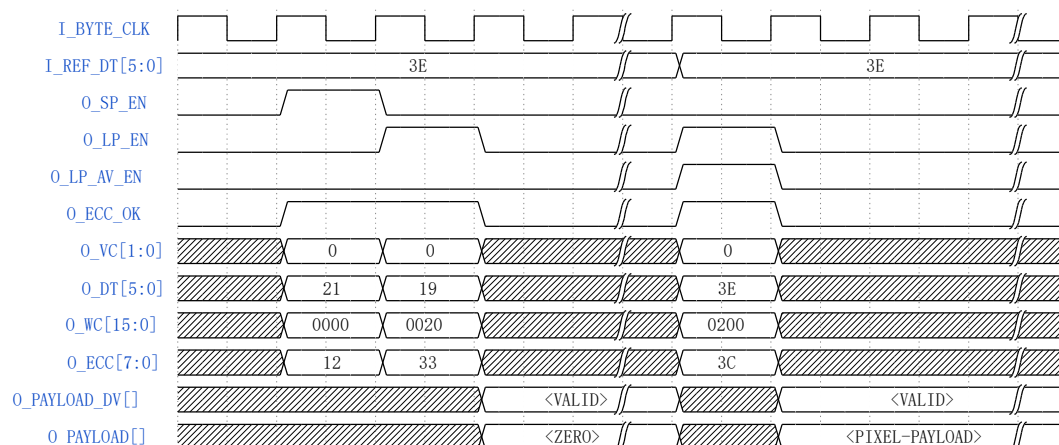
Table 3-1 Gowin MIPI DSI/CSI-2 Receiver IP I/O Ports

Signal	I/O	Description
I_BYTE_CLK	Input	Operating clock
I_RSTN	Input	Asynchronous reset signal, active-low
I_READY	Input	Parallel data alignment indicator signal output by Gowin MIPI D-PHY RX Advance IP
I_DATA0[..]	Input	The parallel data of #n lanes, where $0 \leq n \leq 3$; When "MIPI D-PHY RX Mode" is set to 1:8, the bit width is 8; when set to 1:16, the bit width is 16; When "Number of RX Lanes" is set to 4, I_DATA0~I_DATA3 ports all exist; when set to 3, only I_DATA0~I_DATA2 ports exist; when set to 2, only I_DATA0 and I_DATA1 ports exist; when set to 1, only I_DATA0 port exists.
I_DATA1[..]	Input	
I_DATA2[..]	Input	
I_DATA3[..]	Input	
I_REF_DT[5:0]	Input	Reference data type
O_PAYLOAD[..]	Output	Payload data, and the bit width depending on number of D-PHY lanes and mode (1:8/1:16)
		Number of lanes
		1:8 mode
		1:16 mode
		1
		8
O_PAYLOAD_DV[..]	Output	16
		2
		16
		32
		3
		24
O_SP_EN	Output	48
		4
		32
		64
O_PAYLOAD_DV[..]	Output	Payload data; byte valid indicator with the width of O_PAYLOAD[..] divided by 8
O_SP_EN	Output	Short packet indicator, active-high
O_LP_EN	Output	Long packet indicator, active-high
O_LP_AV_EN	Output	Data type matching indicator, active-high Indicates the current data type matches the reference data type (I_REF_DT)
O_VC[1:0]	Output	Virtual Channel ID, corresponding to Byte0[7:6] in the Packet Header
O_DT[5:0]	Output	Data Type, corresponding to Byte0[5:0] in the Packet Header

Signal	I/O	Description
O_WC[15:0]	Output	Payload byte count, corresponding to Byte1 and Byte2 in the Packet Header
O_ECC[7:0]	Output	Error Correction Code, corresponding to Byte3 in the Packet Header
O_ECC_OK	Output	ECC check passed indicator, active-high
O_SP2_EN	Output	Second set of short packet indicator, active-high
O_LP2_EN	Output	Second set of long packet indicator, active-high
O_LP2_AV_EN	Output	Second set of data type matching indicator, active-high
O_VC2[1:0]	Output	Second set of Virtual Channel ID
O_DT2[5:0]	Output	Second set of data type
O_WC2[15:0]	Output	Second set of payload byte count
O_ECC2[7:0]	Output	Second set of ECC
O_ECC2_OK	Output	Second set of ECC check passed indicator, active-high

3.3 Timing Description

Figure 3-2 Output Timing Diagram



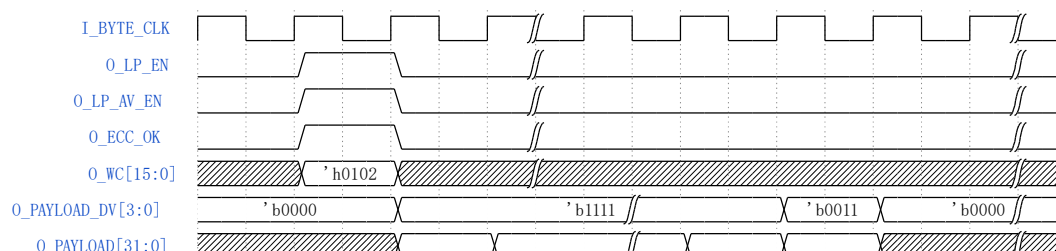
When a valid data type is extracted, **O_SP_EN** or **O_LP_EN** will be asserted, and at the same time, the complete header information will be output, including Virtual Channel ID, Data Type, Word Count, and ECC.

O_LP_AV_EN will only be asserted when the extracted long packet's data type matches the input reference data type (**I_REF_DT[5:0]**), which aims to distinguish the specified video payload data from other long packet data, such as null data or transparent data. If the extracted video payload data type does not match the reference data type, **O_LP_AV_EN** will not

be asserted.

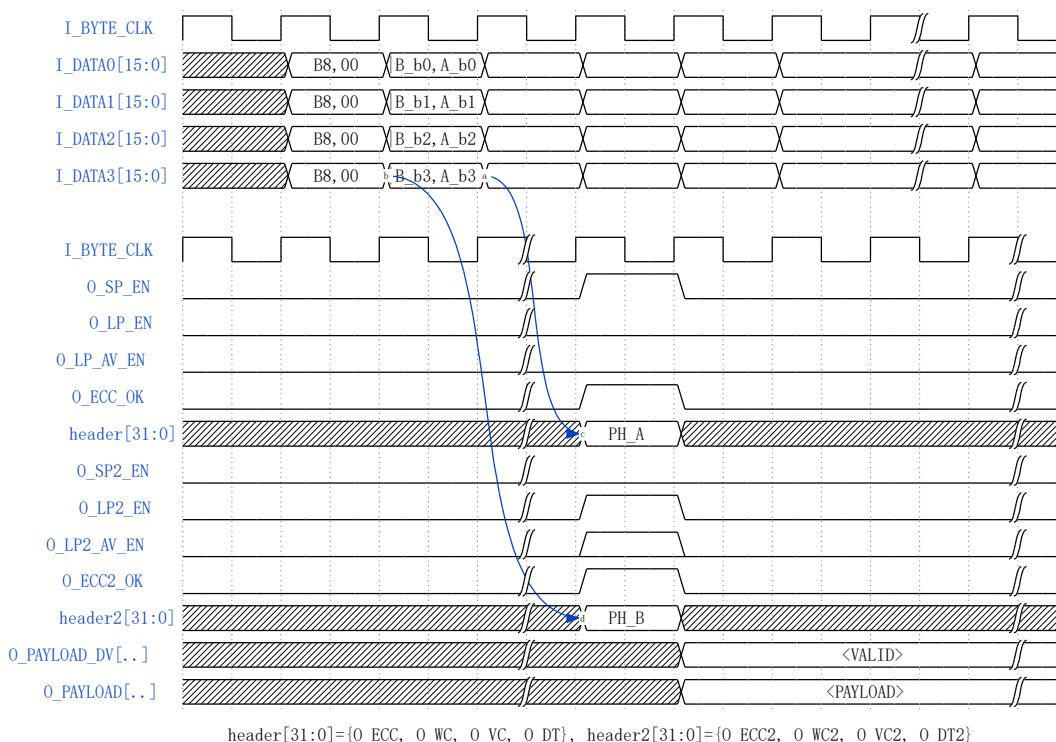
When the calculated ECC based on the {O_WC, O_VC, O_DT} of the extracted header information matches the extracted O_ECC, O_ECC_OK will be asserted. Currently, Error correction for packet headers is not supported.

Figure 3-3 O_PAYLOAD_DV Timing Diagram



O_PAYLOAD_DV outputs payload data byte valid indicator, and each bit corresponds to each byte in O_PAYLOAD. O_PAYLOAD is always aligned forward. Except for the last cycle for valid payload data, all bits of O_PAYLOAD_DV must be '1'; in the last cycle, it is allowed to have consecutive '0's in the high bits and consecutive '1's in the low bits or have all bits as '1'. As shown in Figure 3-3, if the payload byte count is 'h0102', and there are 2 bytes remaining in the last cycle, then O_PAYLOAD_DV would be 'b0011', indicating that the low 2 bytes of O_PAYLOAD are valid.

Figure 3-4 Timing Diagram for Two Sets of Packet Information Output



When configured in DSI mode with input byte data greater than 4 bytes (3-Lane/4-Lane@1:16), the second set of packet header information signals, such as O_SP2_EN as shown in Figure 3-1, in the top block diagram become active. As shown in Figure 3-4, for 4-Lane, 1:16 mode, two sets of packet header information PH_A and PH_B, are output simultaneously. There won't be a scenario where the second set of packet header information is active on its own.

The interval between the packet header information output valid and the input data is not fixed, which depends on the number of lanes and the data mode.

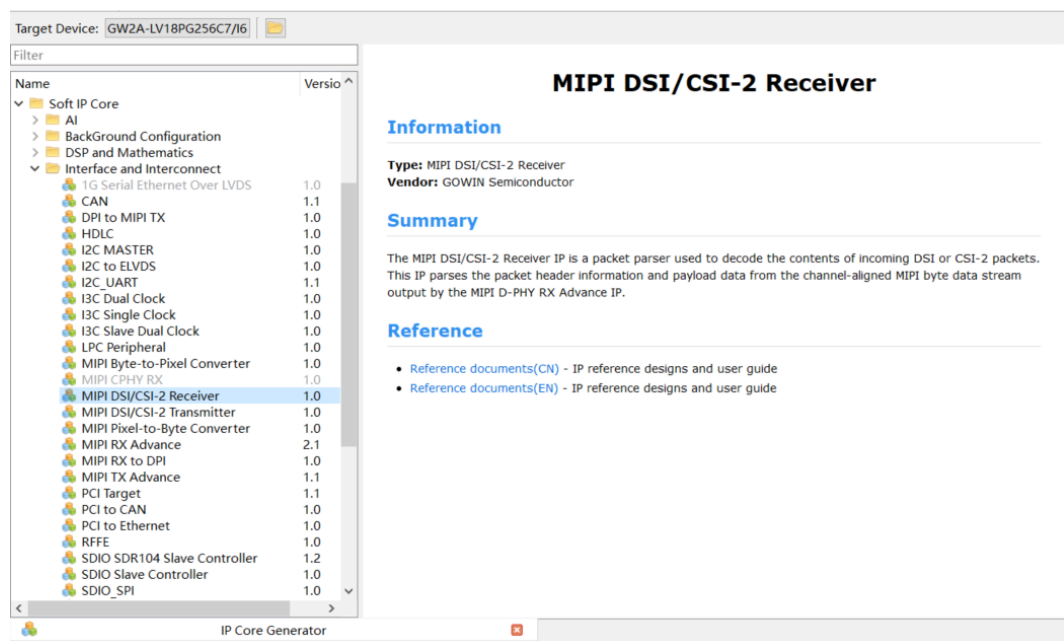
4 Interface Configuration

You can select "Tools" in Gowin Software to start the IP Core Generator to call and configure MIPI DSI/CSI-2 Receiver IP.

1. Open IP Core Generator

After creating the project, click the "Tools" tab in the upper left, click "IP Core Generator" from the drop-down list to open IP Core Generator. Click "Soft IP Core > Interface and Interconnect > MIPI DSI/CSI-2 Receiver"; or enter "DSI/CSI-2 Receiver" in the "Filter" search box to locate it quickly.

Figure 4-1 IP Core Generator



2. MIPI DSI/CSI-2 Receiver IP Configuration Interface

Users can open the MIPI DSI/CSI-2 Receiver IP configuration interface by double clicking the "MIPI DSI/CSI-2 Receiver" item in the "IP Core Generator" tool interface. The port diagram is on the left, and the parameter configuration options are on the right, as shown in Figure 4-2, and the details are shown in Table 4-1.

Figure 4-2 MIPI DSI/CSI-2 Receiver IP Interface Configuration

Table 4-1 Gowin DSI/CSI-2 Receiver IP Parameters

Name	Range	Description
MIPI Interface Type	DSI/CSI-2	Specify MIPI interface type
MIPI D-PHY RX Mode	1:8 or 1:16	D-PHY RX data mode
Number of RX Lanes	1, 2, 3, or 4	Number of D-PHY RX lanes
Generation Config	Checked/Unchecked	- If it is selected, the IP will not insert IBUF, OBUF, and IOBUF in the synthesized netlist. - If it is not selected, the IP will insert IBUF, OBUF, and IOBUF in the synthesized netlist.

Name	Range	Description
		The default setting is checked.

3. Generation and Instantiation

After configuring the parameters according to requirements, click “OK” to generate MIPI DSI/CSI-2 Receiver IP. As shown in Figure 4-3, here is an example of IP instantiation in the user's Verilog program.

Figure 4-3 MIPI DSI/CSI-2 Receiver IP Instantiation

