



Gowin EasyCDR IP

User Guide

IPUG1040-1.4E, 04/24/2026

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Revision History

Date	Version	Description
10/12/2023	1.0E	Initial version published.
02/02/2024	1.1E	8B/10B decoding function added.
04/19/2024	1.2E	● Modify the data order to least significant bit first. ● Modify 8B/10B decoding enable scheme.
05/09/2024	1.3E	● Line rate increased to 2.2 Gbps. ● Descriptions of Section 3.4 GPIO and Section 3.5 Data added. ● Reference design 2 added.
04/24/2026	1.4E	● Added Table 2-2 Line Rate Supported by Each Device. ● Updated descriptions of Delay Step in Table 5-1 IP Configuration Option. ● Updated section 1.2 Related Documents.

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1 About This Guide

1.1 Purpose

The purpose of Gowin EasyCDR IP User Guide is to help you to quickly understand the features and usage of Gowin EasyCDR IP by providing the descriptions of the functions, signal definition, parameters, and reference design. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.9.03. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

You can find the related documents at GOWINSEMI website:
www.gowinsemi.com.

- [SUG100, Gowin Software User Guide](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)
- [DS1118, GW5ART series of FPGA Products Data Sheet](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
ALU	Arithmetic Logic Unit
GPIO	Gowin Programmable Input/Output
HCLK	High-speed Clock

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
IP	Intellectual Property
LUT	Look-up Table
PLL	Phase-locked Loop
PRBS	Pseudo-Random Binary Sequence
REG	Register

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Introduction

The Gowin EasyCDR IP, based on GPIO, provides the functionality of converting high-speed serial data to low-speed parallel data. Users can utilize this IP to extract serial data stream without accompanying clock signals.

Table 2-1 Gowin EasyCDR IP Overview

Gowin EasyCDR IP	
Logic Resource	See Table 2-3 .
Delivered Doc.	
Design Files	Verilog (encryption)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9 Beta-5 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features

- Convert serial data into parallel data
- Receive data without accompanying clock signal
- Output data width of 10/16/20/32 bits
- Input data line rate ranges from 0.1 Gbps to 2.2 Gbps^[1]
- Capable of recognizing or parsing serial data after 8B/10B encoding

Note!

^[1] The supported input data line rate range varies depending on the device. Please refer to Table 2-2 for details.

Table 2-2 Line Rate Supported by Each Device

Device	Line Rate
GW5A-25	0.1 Gbps~2.2 Gbps
GW5AR-25	
GW5AS-25	
GW5ART-15	0.1 Gbps~1.0 Gbps
GW5AT-15	
GW5A-60	
GW5AT-60	
GW5A-138	
GW5AS-138	
GW5AT-138	
GW5AST-138	

2.3 Operating Frequency

When the line rate of the input data stream is not higher than 1 Gbps, the operating frequency of Gowin EasyCDR IP is one-eighth of the line rate of the input data stream.

When the line rate of the input data stream exceeds 1 Gbps, the operating frequency of Gowin EasyCDR IP is one-sixteenth of the line rate of the input data stream.

2.3.1 Frequency Offset Tolerance

At a rate of 1 Gbps, Gowin EasyCDR IP can tolerate a frequency offset of ± 5000 ppm. The frequency offset tolerance varies with the rate and is inversely correlated with the speed.

2.4 Resource Utilization

Gowin EasyCDR IP is implemented with Verilog HDL. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW5A(R)-25 device as an instance, the resource utilization is as shown in . For the resource utilization of other devices, please refer to later release information.

Table 2-3 Resource Utilization

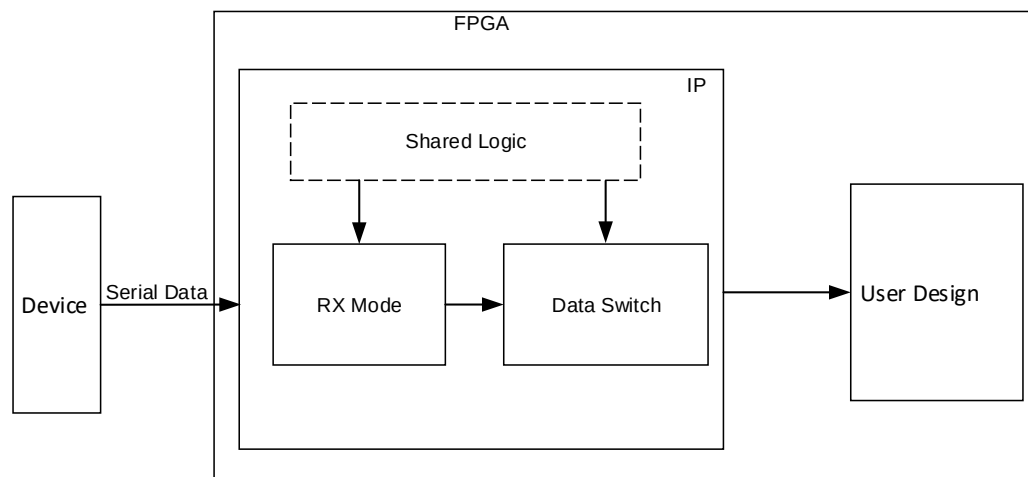
Device	Programming Language	LUTs	REGs
GW5A(R)-25	Verilog HDL	458	294

3 Functional Description

3.1 Structure

Gowin EasyCDR IP primarily consists of RX Mode, Data switch and Shared Logic, as shown in Figure 3-1.

Figure 3-1 Gowin EasyCDR IP Structure Diagram



- RX Mode: Receive and process serial data stream without accompanying clock signals
- Data switch: Parse and convert the processed data into parallel data
- Shared logic: Clock control module, see 3.2 Clocking and 3.3 Resets

3.2 Clocking

The HCLK resource is included in the device as a high speed clock signal to drive GPIO resource. Each 4-channel HCLK is a group, and each HCLK group can drive a specific GPIO resource and be driven by the corresponding PLL resource. The frequency of each HCLK group is determined by the line rate of the input data stream, with phases of 0°, 90°, 180°, and 270° respectively. When the line rate of the input data stream is not higher than 1 Gbps, the frequency of HCLK is half of the line rate; when the line rate of the input data stream exceeds 1 Gbps, the frequency of HCLK is one-fourth of the line rate. For the correspondence

between HCLK, PLL, and GPIO, see the FPGA product data sheets in [1.2 Related Documents](#).

For example, GW5A(R)-25 series of FPGA products contain 16 HCLK resources, divided into 4 HCLK groups, each HCLK group can drive 2 BANK GPIOs. And each HCLK group can be driven by 2 PLLs. Table 3-1 shows the GPIO and PLL for each HCLK group within GW5A(R)-25 series of FPGA products.

Table 3-1 GPIO and PLL for HCLK Group within GW5A(R)-25 series of Products

PLL	BANK
PLL_T/PLL_R[0]	BANK0/BANK1
PLL_R[1]/PLL_B	BANK2/BANK3
PLL_B/PLL_L[1]	BANK4/BANK5
PLL_L[0]/PLL_T	BANK6/BANK7

Since each HCLK group has the corresponding GPIO and PLL, when instantiating Gowin EasyCDR IP, it is necessary to follow the following requirements:

- When instantiating a single IP, the IP receive differential signals (rxp_i/rxn_i) are assigned to the GPIO of the same HCLK group.
- When instantiating multiple IPs, the differential signals of all IPs are assigned to the GPIO of the same HCLK group as far as possible to save HCLK and PLL resources.
- The BANK assigned according to the differential signal of the IP needs to be manually constrained PLL to the corresponding position. For example, if the differential signal of the IP is assigned to BANK0, then constrain PLL to PLL_T, and PLL is instantiated at the project top layer. The instantiation name is u_pll_hclk, the constraint statement is "INS_LOC"u_pll_hclk/PLLA_inst" PLL_T;", and the PLL is written to the .cst file.

3.2.1 Shared logic

Gowin EasyCDR IP requires 4 HCLK resources to build a clock network, and when multiple IPs are instantiated within the same HCLK group, all IPs need to share the clock network.

Shared logic is a clock network built for 4 HCLKs, allowing users to choose whether the IP contains Shared logic based on their design requirements.

The relationship between Gowin EasyCDR IP output data and the clock is as follows:

- When Inside is selected for Shared Logic, the parallel data of IP output is synchronized to share_clk4_o of IP output.
- When Outside is selected for Shared Logic, the parallel data of IP output is synchronized to share_clk4_i of IP input.

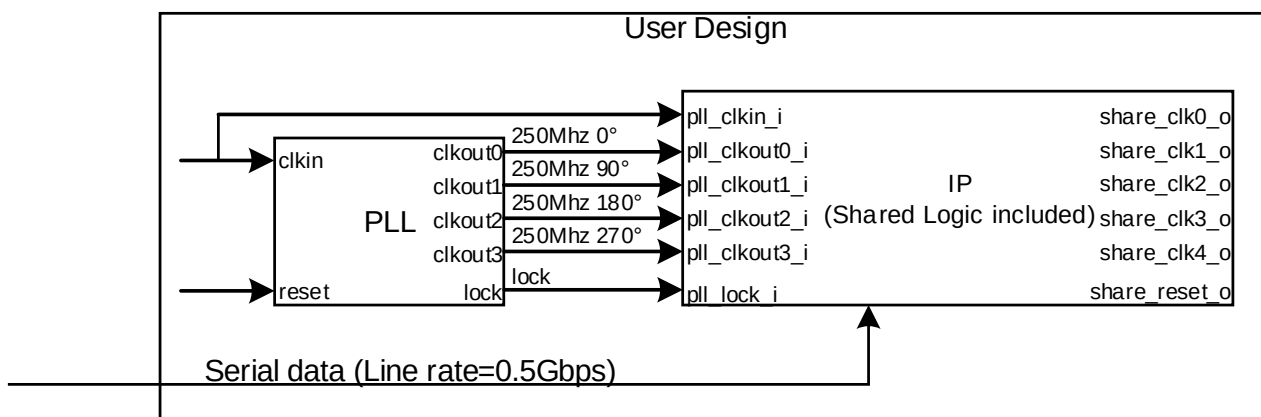
In the user design, the PLL output clock frequency is determined by

the line rate of the input data stream. When the line rate of the input data stream is not higher than 1 Gbps, the frequency of the PLL output clock is half of the line rate; when the line rate of the input data stream exceeds 1 Gbps, the frequency of the PLL output clock is one-fourth of the line rate. As shown in the diagram, when the line rate is 0.5 Gbps, the PLL output clock frequency is 250 MHz. Users can adjust it based on the actual line rate.

Single IP

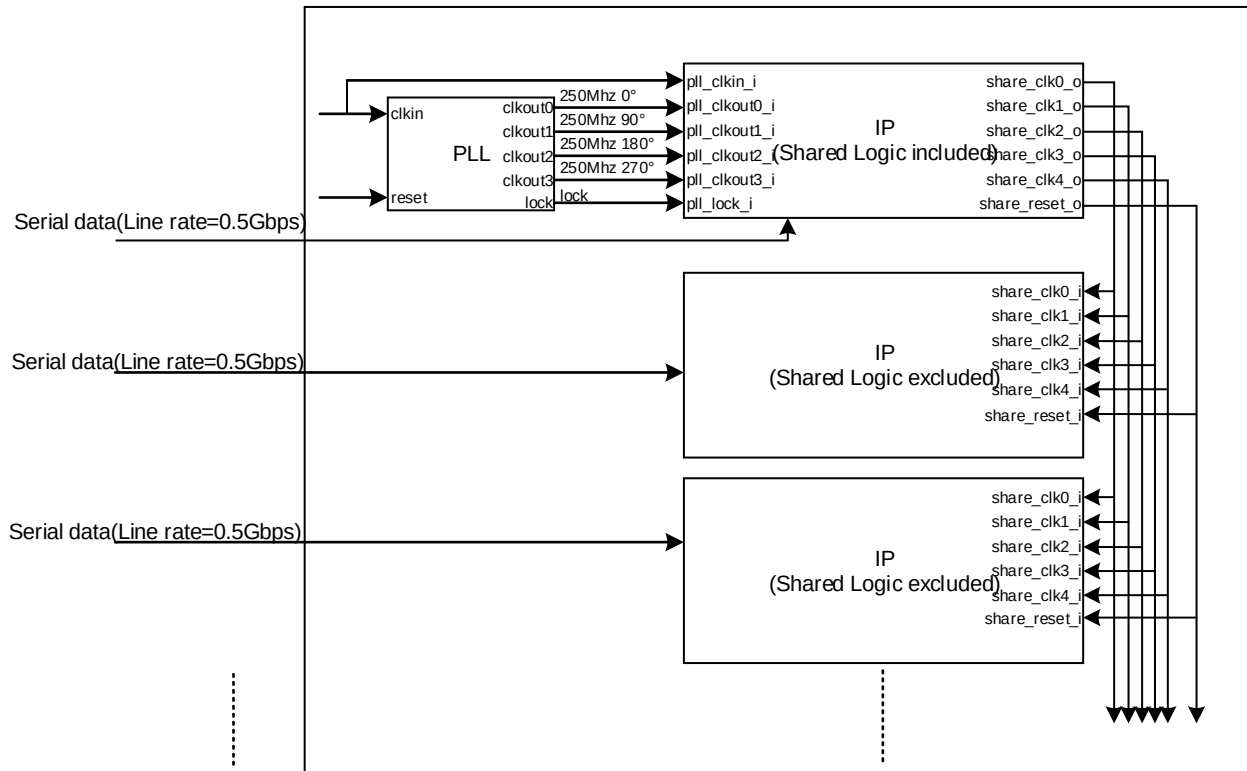
When only a single IP is instantiated in the HCLK group, the IP should contain Shared logic, which is used to build a clock network. Figure 3-2 shows the connection between clock logic and IP in the case of a single IP.

Figure 3-2 Connection between Clock Logic and IP (Single IP)



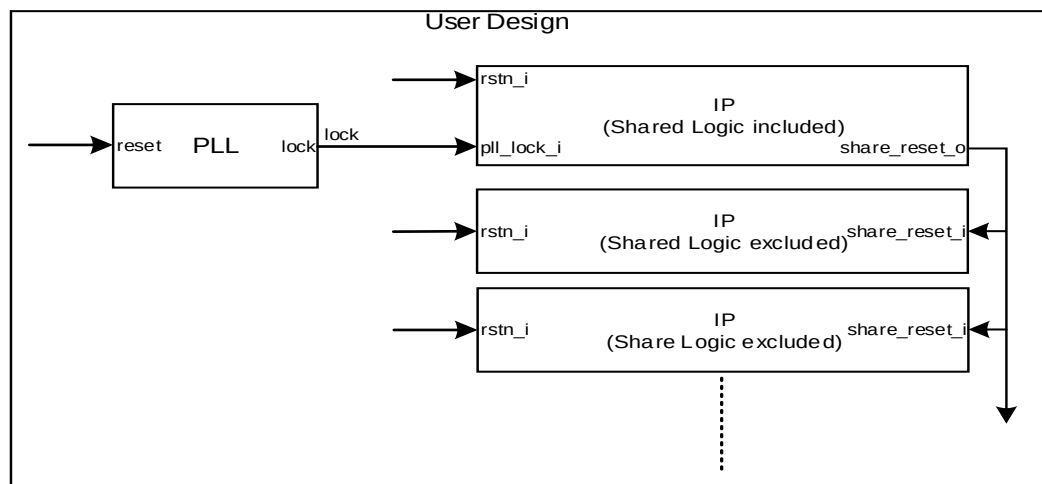
Multiple IPs

When at least two IPs are instantiated in the HCLK group, one IP should contain Shared logic and the remaining IP should not contain Shared logic to enable the sharing of the clock network. Figure 3-3 shows the connection between clock logic and IP in the case of multiple IPs.

Figure 3-3 Connection between Clock Logic and IP (Multiple IPs)

3.3 Resets

Gowin EasyCDR IP supports two reset modes. The first reset mode is used to reset all the IPs within an HCLK group by resetting the PLL to control the Shared logic. The other reset mode is used for individually resetting a single IP by using `rstn_i`. Figure 3-4 shows the logic connections for these two reset modes in the IP.

Figure 3-4 Logic Connections for Two Reset Modes

3.4 GPIO

The differential signals rxp_i and rxn_i of the IP can only be assigned to GPIOs that support LVDS; for the details, you can see [UG985, GW5A-25 Pinout](#).

When the line rate of the input data stream is not higher than 1 Gbps, the IP only utilizes the IODELAY of the allocated GPIOs for data processing. When the line rate of the input data stream exceeds 1 Gbps, the IP will utilize the IODELAY of adjacent GPIOs for data processing. Additionally, the GPIO corresponding to IODELAY can also no longer be pin-assigned. The using rules are described as follows:

- The allocated GPIOs and the borrowed GPIOs belong to the same IOT/IOR/IOB/IOL.
- Borrow the GPIO with a smaller pin number adjacent to the assigned GPIO.
- The borrowed GPIOs must also support LVDS.
- Pins that are not externally bonded out can also be borrowed.

Note !

If there are no available IODELAYs to borrow for a GPIO, the IP cannot be allocated to that location.

Taking GW5A(R)-25 series of FPGA products as an example, there are 13 pairs of GPIOs supporting LVDS in BANK7 (UG324 package). When the line rate of input data stream is not greater than 1 Gbps, the differential signals rxp_i and rxn_i of the IP can be assigned to any of the 13 pairs of GPIOs. When the line rate of input data stream is greater than 1 Gbps, the differential signals rxp_i and rxn_i of the IP can be assigned to any of the 12 pairs of GPIOs except H4 (IOT1A) and H3 (IOT1B).

For example, when the differential signals rxp_i and rxn_i of the IP are assigned to L7 (IOT21A) and K6 (IOT21B), the IP will borrow the IODELAY corresponding to D2 (IOT19A) and D1 (IOT19B); D2 and D1 cannot be pin-assigned. Similarly, when the differential signals rxp_i and rxn_i of the IP are assigned to G3 (IOT7A) and G1 (IOT7B), the IP will borrow the IODELAY corresponding to IOT5A and IOT5B (IOT5A and IOT5B are not bonded out in UG324). Since there are no available GPIOs to borrow in H4 (IOT1A) and H3 (IOT1B), the IP cannot assign the differential signals rxp_i and rxn_i to these locations.

Figure 3 5 shows the 13 pairs of GPIOs support LVDS in BANK7 (UG324 package).

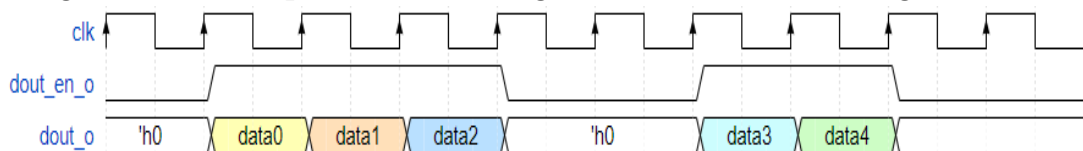
Figure 3-5 13 Pairs of GPIOs supporting LVDS in BANK7 (UG324 package)

Pin Name	Function	BANK	ADC_INPUT	DQS	Configuration Function	Differential Pair	LVDS	UG324
BANK7 True LVDS Pair								
IOT11A	I/O	7	bus0	none		True_of_IOT11B	True	F2
IOT11B	I/O	7	bus0	none		Comp_of_IOT11A	True	F1
IOT13A	I/O	7	bus0	none		True_of_IOT13B	True	J7
IOT13B	I/O	7	bus0	none		Comp_of_IOT13A	True	J6
IOT15A	I/O	7	bus0	none		True_of_IOT15B	True	E3
IOT15B	I/O	7	bus0	none		Comp_of_IOT15A	True	E1
IOT17A	I/O	7	bus0	none		True_of_IOT17B	True	F4
IOT17B	I/O	7	bus0	none		Comp_of_IOT17A	True	F3
IOT19A	I/O	7	bus0	none		True_of_IOT19B	True	D2
IOT19B	I/O	7	bus0	none		Comp_of_IOT19A	True	D1
IOT1A/GCLKT_15/LPLL0_T_IN0	I/O	7	bus0	none	GCLKT_15/LPLL0_T_IN0	True_of_IOT1B	True	H4
IOT1B/GCLKC_15/LPLL0_C_IN0	I/O	7	bus0	none	GCLKC_15/LPLL0_C_IN0	Comp_of_IOT1A	True	H3
IOT21A	I/O	7	bus0	none		True_of_IOT21B	True	L7
IOT21B	I/O	7	bus0	none		Comp_of_IOT21A	True	K6
IOT23A	I/O	7	bus0	none		True_of_IOT23B	True	E4
IOT23B	I/O	7	bus0	none		Comp_of_IOT23A	True	D3
IOT25A	I/O	7	bus0	none		True_of_IOT25B	True	F6
IOT25B	I/O	7	bus0	none		Comp_of_IOT25A	True	F5
IOT27A	I/O	7	bus0	none		True_of_IOT27B	True	C2
IOT27B	I/O	7	bus0	none		Comp_of_IOT27A	True	C1
IOT3A/GCLKT_16	I/O	7		none	GCLKT_16	True_of_IOT3B	True	L5
IOT3B/GCLKC_16	I/O	7		none	GCLKC_16	Comp_of_IOT3A	True	K5
IOT7A	I/O	7	bus0	none		True_of_IOT7B	True	G3
IOT7B	I/O	7	bus0	none		Comp_of_IOT7A	True	G1
IOT9A	I/O	7	bus0	none		True_of_IOT9B	True	H7
IOT9B	I/O	7	bus0	none		Comp_of_IOT9A	True	G6

3.5 Data

The IP converts serial signals into parallel data for output while reducing the clock frequency for subsequent data processing.

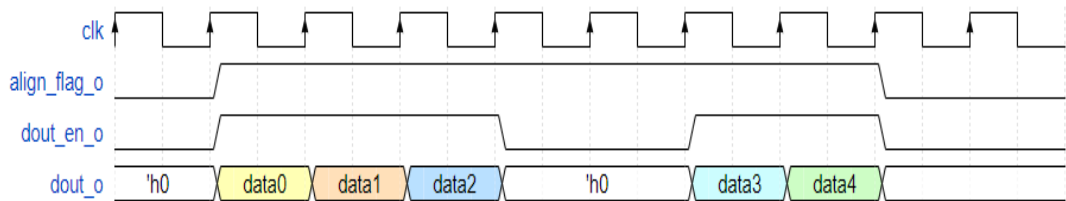
When the Word Alignment and 8B/10B Decoding are not enabled, the IP outputs the received data through dout_en_o and dout_o. When dout_en_o is 1, dout_o outputs the received data, with the earlier received serial data placed at the lower bits. Figure 3-6 illustrates the data output when Word Alignment and 8B/10B Decoding disabled.

Figure 3-6 Data Output when Word Alignment and 8B/10B Decoding Disabled

3.5.1 Word Alignment

When Word Alignment enabled, the IP aligns the received data according to the set K character, and outputs the aligned data. Word Alignment can only be selected when the line rate of input data stream is not higher than 1Gbps and dout_o is 10 bits.

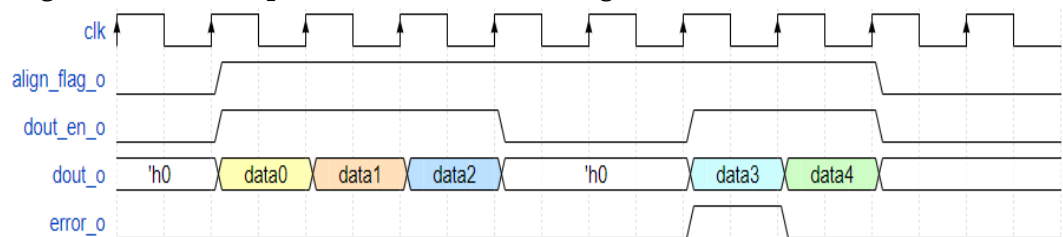
When align_flag_o is 1, it indicates successful alignment of the received data. If dout_en_o is also 1 at this time, dout_o outputs the aligned data, with the earlier received serial data placed at the lower bits. When align_flag_o is 0, it indicates failed alignment of the received data, and the IP does not output any data. Figure 3-7 illustrates the data output when Word Alignment enabled.

Figure 3-7 Data Output when Word Alignment Enabled

3.5.2 8B/10B Decoding

When 8B/10B Decoding enabled, the IP will process the received data for 8B/10B decoding to its original encoded form. 8B/10B Decoding can only be selected when the line rate of input data stream is not higher than 1 Gbps and dout_o is 10 bits.

When align_flag_o is 1, it indicates successful alignment of the received data. If dout_en_o is also 1 at this time, dout_o outputs the data after 8B/10B decoding. When align_flag_o is 0, it indicates failed alignment of the received data, and the IP does not output any data. When dout_en_o is 1, if error_o is 0, dout_o decodes the data without anomalies. If error_o is 1, dout_o encounters inconsistencies or data anomalies during decoding. Figure 3-8 illustrates the data output when 8B/10B Decoding enabled.

Figure 3-8 Data Output when 8B/10B Decoding Enabled

The decoded data dout_o consists of two parts: K character and data. K character of 1 indicates that the data is a K character; K character of 0 indicates that the data is a D character. dout_o is arranged from high to low bits in the following order: 1 bit for 0, 1 bit for the K character, and 8 bits for the data. Table 3-2 illustrates the data format of dout_o when 8B/10B Decoding enabled.

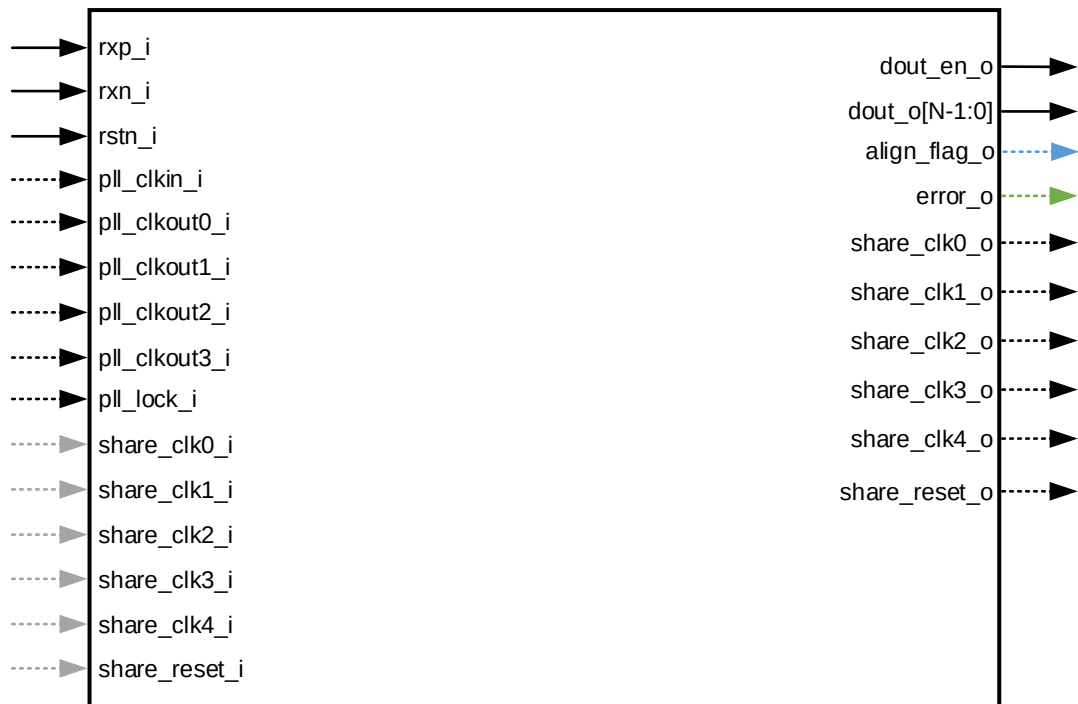
Table 3-2 Data Format of dout_o when 8B/10B Decoding Enabled

Bit	9	8	7:0
Meaning	0 in most cases	K Character	Data

4 Port Description

The connection diagram of Gowin EasyCDR IP is shown in Figure 4-1.

Figure 4-1 Gowin EasyCDR IP Port Diagram



Note!

- indicates that the port is available when "Inside" is selected for Shared logic.
- indicates that the port is available when "Outside" is selected for Share logic.
- indicates that the port is available when "Word Alignment" is checked.
- indicates that the port is available When "Word Alignment" and "Enable 8B/10B Decoding" are selected.

Signal Definition

Table 4-1 Gowin EasyCDR IP Port Signal

No.	Signal	Type	Data Width	Description
1	rxp_i	Input	1	Receive differential signal, positive-side
2	rxn_i	Input	1	Receive differential signal, negative-side
3	rstn_i	Input	1	Reset signal, active-low

No.	Signal	Type	Data Width	Description	
4	pll_clkkin_i	Input	1	PLL reference clock	
5	pll_clkout0_i	Input	1	0-channel clock signal of the PLL with phase of 0°	
6	pll_clkout1_i	Input	1	1-channel clock signal of the PLL with phase of 90°	
7	pll_clkout2_i	Input	1	2-channel clock signal of the PLL with phase of 180°	
8	pll_clkout3_i	Input	1	3-channel clock signal of the PLL with phase of 270°	
9	pll_lock_i	Input	1	PLL lock signal, active-high	
10	share_clk0_o	Output	1	Share clock 1 output with the phase of 0°	
11	share_clk1_o	Output	1	Share clock 2 output with the phase of 90°	
12	share_clk2_o	Output	1	Share clock 3 output with the phase of 180°	
13	share_clk3_o	Output	1	Share clock 4 output with the phase of 270°	
14	share_clk4_o	Output	1	Share clock 5 output	
15	share_reset_o	Output	1	Shared reset output, active-high	
16	share_clk0_i	Input	1	Share clock 1 input with the phase offset of 0°	
17	share_clk1_i	Input	1	Share clock 2 input with the phase offset of 90°	
18	share_clk2_i	Input	1	Share clock 3 input with the phase offset of 180°	
19	share_clk3_i	Input	1	Share clock 4 input with the phase offset of 270°	
20	share_clk4_i	Input	1	Share clock 5 input	
21	share_reset_i	Input	1	Shared reset input, active-high	
22	dout_en_o	Output	1	Parallel data valid indicator, active-high	Synchronized to share_clk4_o when Inside is selected for Shared Logic; Synchronized to share_clk4_i when Outside is selected for Shared Logic.
23	dout_o	Output	32/20/16/10	Parallel data output with least significant bit first	
24	align_flag_o	Output	1	Data alignment indicator, active-high	
25	error_o	Output	1	Output error indicator, active-high	

5 Call and Configure

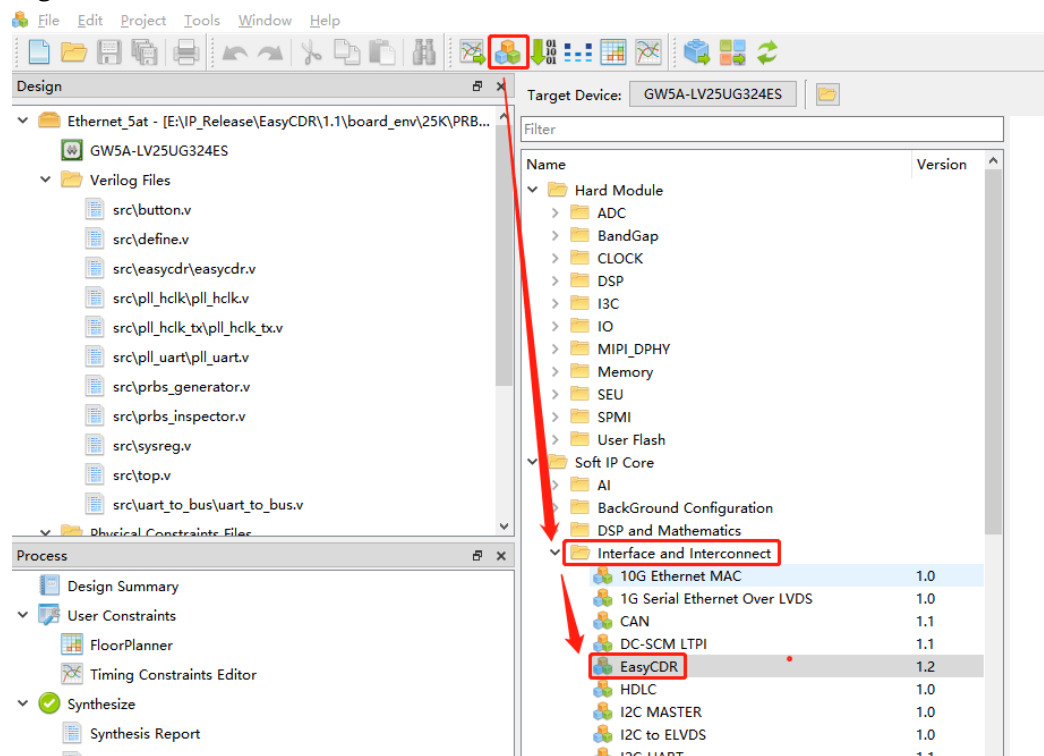
5.1 IP Generation

Click " " in the quickbar or "Tools > IP Core Generator" in the menu bar in Gowin Software to call and configure Gowin EasyCDR IP.

1. Open IP Core Generator.

After creating a new project, click "IP Core Generator" to open the IP Core Generator, as shown in Figure 5-1.

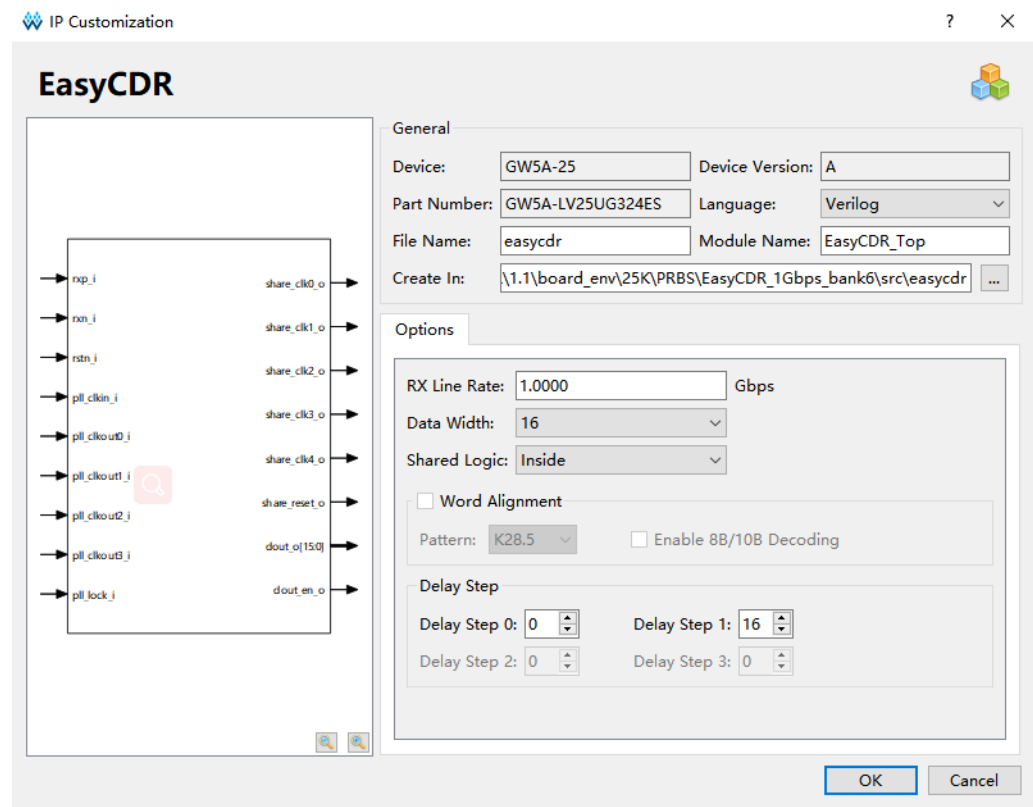
Figure 5-1 IP Core Generator Interface



2. Open Gowin EasyCDR IP.

Double-click "Soft IP Core > Interface and Interconnect > EasyCDR", open the EasyCDR IP Interface, as shown in Figure 5-2.

Figure 5-2 Gowin EasyCDR IP Configuration Interface



- You can configure the generated file name by modifying "File Name".
- You can configure the top module name in "Module Name".
- You can configure other options by modifying "Options".

5.2 IP Configuration

Table 5-1 IP Configuration Option

Options	Description
RX Line Rate	Receive signal line rate with range from 0.1~2.2 Gbps
Data Width	Output parallel data bit width: ● When the RX Line Rate is not higher than 1Gbps, 10 or 16 can be selected. ● When the RX Line Rate exceeds 1Gbps, 20 and 32 can be selected.
Shared logic	Shared clock logic, depending on the application ● Select "Inside" to output a share clock that serves other instantiated IPs. ● Select "Outside" to receive a share clock and do not output.
Word Alignment	When it is enabled, port align_flag_o is high, indicating successful alignment. When the RX Line Rate is not higher than 1Gbps and the Data Width is 10, it can be selected.
Pattern	K character for 8B/10B decoding, a total of 12 types. It is available when Word Alignment is checked.
Enable 8B/10B Decoding	When it is selected, the decoded data is output. It is available when Word Alignment is checked.
Delay Step 0	IODELAY delay value 0, automatically generated by the software and cannot

Options	Description
	be modified.
Delay Step 1	IODELAY delay value 1, automatically generated by the software and cannot be modified.
Delay Step 2	IODELAY delay value 2, automatically generated by the software and cannot be modified.
Delay Step 3	IODELAY delay value 3, automatically generated by the software and cannot be modified.

6 Reference Design

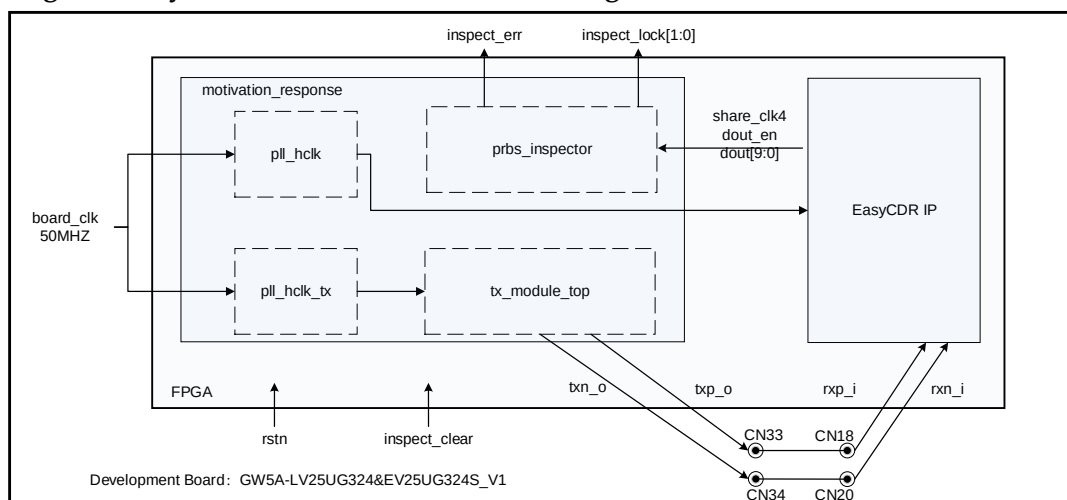
For more details, you can see Gowin EasyCDR IP [reference design](#) at Gowinsemi website.

6.1 Reference Design 1

6.1.1 Hardware Platform

This section introduces the IP implementation example using GW5A(R)-LV25UG324&EV25UG324S_V1, namely Gowin EasyCDR RefDesign. The system structure is shown in Figure 6-1.

Figure 6-1 System Structure of Reference Design 1



1. All internal clocks in the FPGA are generated by the onboard crystal oscillator, with a frequency of 50MHz.
2. Switch SW2 (rstn) allows resetting internal modules of the FPGA, active-low.
3. Switch SW3 (inspect_clear) enables clearing the data inspection, active-low.
4. LED D8 (inspect_lock[0]) indicates the stability of the current data reception. A high level indicates stable data reception.

5. LED D9 (inspect_lock[1]) indicates the stability of data reception. A high level indicates that unstable conditions have occurred during data reception.
6. LED D11 (inspect_err) indicates the occurrence of errors during data reception. A high level indicates errors during the data reception.
7. sma interface CN33 and CN34 are the differential pairs of the transmitting, with a line rate of 1 Gbps.
8. sma interface CN18 and CN20 are the differential pairs of the receiving.

6.1.2 Working Principle

The system clock is generated by the on-board crystal oscillator and works as follows:

1. pll_hclk and pll_hclk_tx generate the clocks required by the system.
2. The tx_module_top generates pseudo-random differential serial data stream, and they are output to the on-board sma interfaces CN33 and CN34.
3. CN33 and CN34 are connected to CN18 and CN20 via RF cables, providing channels for the data stream to the IP.
4. The IP decodes the input data stream and transfers the decoded data to the prbs_inspector for testing. The test results are output to inspect_err and inspect_lock, which users can view through Gowin Logic Analyzer () .

6.1.3 Parameter Configuration

On-board crystal oscillator input clock is 50 MHz, users can modify the PLL as required to obtain the clock at the desired frequency (the currently designed hardware platform supports serial line rate ranging from 0.1~1 Gbps).

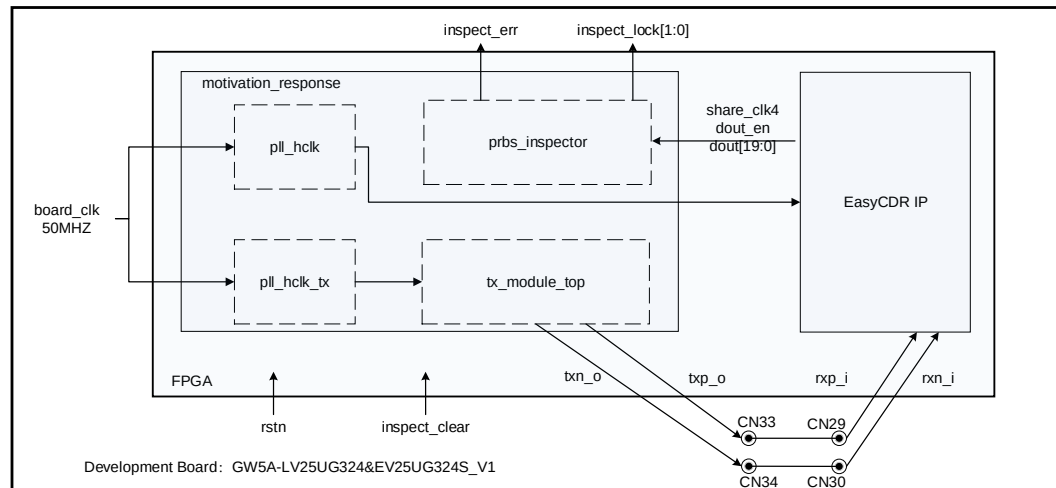
6.1.4 Operating Flow

1. Open Gowin Software (V1.9.9.03 and above) > Open routine project and set top layer file > Compile routine > Download the generated bitstream file (ao.fs) to the board.
2. Click Gowin Analyzer Oscilloscope (icon ) > Run on the toolbar, and observe the results.

6.2 Reference Design 2

6.2.1 Hardware Platform

This section introduces the IP implementation example using GW5A(R)-LV25UG324&EV25UG324S_V1, namely Gowin EasyCDR RefDesign. The system structure is shown in Figure 6-2.

Figure 6-2 System Structure of Reference Design 2

1. All internal clocks in the FPGA are generated by the onboard crystal oscillator, with a frequency of 50MHz.
2. Switch SW2 (rstn) allows resetting internal modules of the FPGA, active-low.
3. Switch SW3 (inspect_clear) enables clearing the data inspection, active-low.
4. LED D8 (inspect_lock[0]) indicates the stability of the current data reception. A high level indicates stable data reception.
5. LED D9 (inspect_lock[1]) indicates the stability of data reception. A high level indicates that unstable conditions have occurred during data reception.
6. LED D11 (inspect_err) indicates the occurrence of errors during data reception. A high level indicates errors during the data reception.
7. sma interface CN33 and CN34 are the differential pairs of the transmitting, with a line rate of 1.2 Gbps.
8. sma interface CN29 and CN30 are the differential pairs of the receiving.

6.2.2 Working Principle

The system clock is generated by the on-board crystal oscillator and works as follows:

1. pll_hclk and pll_hclk_tx generate the clocks required by the system.
2. The tx_module_top generates pseudo-random differential serial data stream, and they are output to the on-board sma interfaces CN33 and CN34.
3. CN33 and CN34 are connected to CN29 and CN30 via RF cables, providing channels for the data stream to the IP.
4. The IP decodes the input data stream and transfers the decoded data to the prbs_inspector for testing. The test results are output to

inspect_err and inspect_lock, which users can view through Gowin Logic Analyzer ()

6.2.3 Parameter Configuration

On-board crystal oscillator input clock is 50 MHz, users can modify the PLL as required to obtain the clock at the desired frequency (the currently designed hardware platform supports serial line rate ranging from 1.0001~2.2 Gbps).

6.2.4 Operating Flow

1. Open Gowin Software (V1.9.9.03 and above) > Open routine project and set top layer file > Compile routine > Download the generated bitstream file (ao.fs) to the board.
2. Click Gowin Analyzer Oscilloscope (icon ) > Run on the toolbar, and observe the results.

7 File Delivery

The delivery file of Gowin EasyCDR IP includes documentation and reference design.

7.1 Documentation

The folder mainly contains the user guide in PDF version.

Table 7-1 Documents List

Name	Description
IPUG1040, Gowin EasyCDR IP User Guide	Gowin EasyCDR IP User guide

7.2 Reference Design

Table 7-2 Reference Design File List

File Name	Description
top.v	The top-level file of the IP routine, which provides interface information, unencrypted
easycdr	EasyCDR IP folder, containing files related to EasyCDR IP, encrypted
pll_hclk	PLL folder, using onboard 50MHz clock as reference clock, and generating the clock required for EasyCDR IP, unencrypted
pll_hclk_tx	PLL folder, using onboard 50MHz clock as reference clock, and generating the clock required for tx_module_top, unencrypted
motivation_response.v	Motivation and detection files, unencrypted
fpga_project.cst	Physical constraint file, unencrypted (user-configurable)
fpga_project.sdc	Timing constraint file, unencrypted (user-configurable)
fpga_project.rao	gao file, unencrypted (user-configurable)

