



Gowin LVDS 7:1 RX LVDS 4:1 TX Reference Design **User Guide**

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Revision History

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1 About This Guide

1.1 Purpose

This guide presents the LVDS 7:1 RX LVDS 4:1 TX Reference Design and documents its functions and features, ports and timing, etc., It is designed to help users quickly understand the main features and usage of the Gowin LVDS 71 RX LVDS 41 TX Reference Design.

1.2 Supported Products

The information that is presented in this guide applies to the following products:

GW2A series of FPGA products: GW2A-18

1.3 Related Documents

The latest user guides are available on the Gowin website. Refer to the related documents at www.gowinsemi.com:

GW2A series of FPGA Products Data Sheet

1.4 Abbreviations and Terminology

The abbreviations and terminology used in this manual are presented in Table 1-1.

Table 1-1: Abbreviations and Terminology

Abbreviations and Terminology	Full Name	Meaning
FPGA	Field Programmable Gate Array	Field Programmable Gate Array
LVDS	Low-Voltage Differential Signaling	Low-Voltage Differential Signaling
I/O	Input/Output	Input/Output
PLL	Phase Locked Loop	PLL

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information presented below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

Tel: +86 755 8262 0391

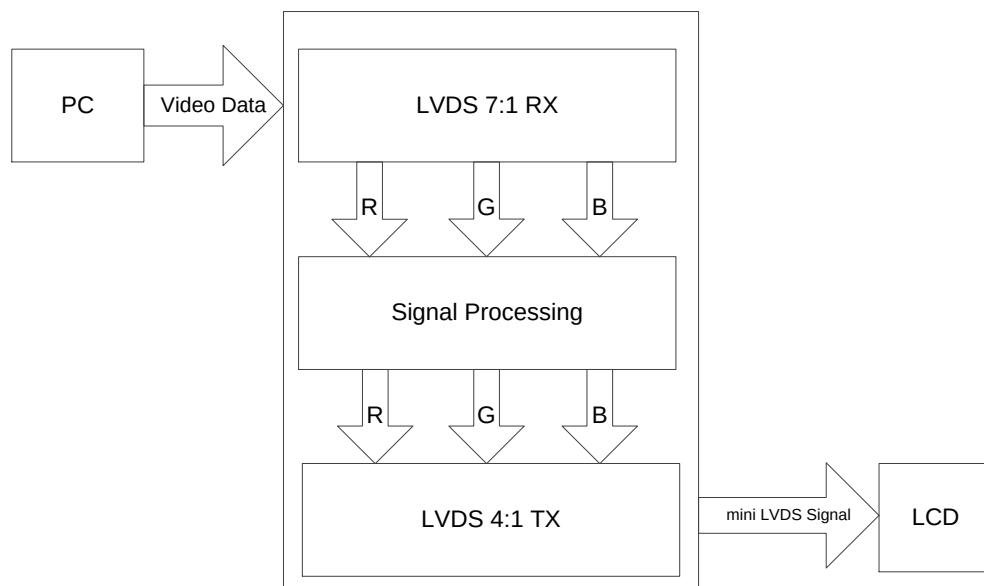
2Overview

2.1 Introduction

The LVDS 7:1 RX LVDS 4:1 TX Reference Design is mainly related to the TCON board, which can convert LVDS video signals to the LVDS data signals the data driving circuit uses to realize 1080P MB drivers 4 k2k LCD screen.

The data port of the LVDS 7:1 RX LVDS 4:1 TX Reference Design converts the video image data received from PC to a low-speed video signal via the VDS7:1 RX module using a LVDS I/O. It subsequently converts the low-speed video signal to the RGB signal needed for the LCD screen using the signal processing module before converting the RGB signal to a mini-LVDS signal and sending it to the LVDS RX chip. The structure diagram is shown in Figure 2-1.

Figure 2-1: Structure Diagram of LVDS 7:1 RX LVDS 4:1 TX Reference Design



3Features and Performance

3.1 Key Features

- Complies with LVDS and mini LVDS port standard.
- Adopts low-voltage differential signaling.
- Supports high-speed, low-noise, long-distance, and high-accuracy data transmission.

3.2 Max. Frequency

The timing interface rate can be up to 800 Mbps.

3.3 Resource Utilization

The LVDS 7:1 RX LVDS 4:1 TX Reference Design can be realized via Verilog, which is applied to the GW2A-18-LQFP144 FPGA. The resource utilization is as shown in Table 3-1.

Table 3-1: Resource Utilization

Package Information	Speed Grade	Name	Resource Utilization	Remarks
GW2A-18-LQFP144	-6	LUT	1452	Contains word alignment and bit alignment modules
		ALU	61	
		PLL	2	
		CLKDIV	5	
		REG	790	

4Functional Description

4.1 Functions

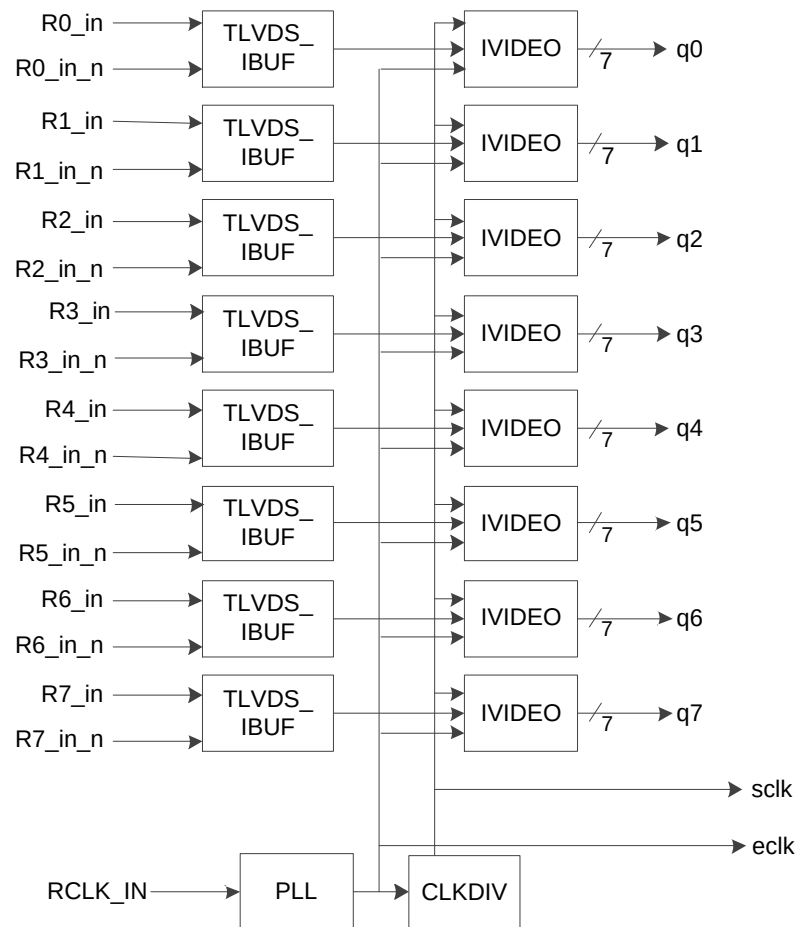
The LVDS 7:1 RX LVDS 4:1 TX Reference Design includes three modules:

- LVDS 7:1 RX module
- DSP
- LVDS 4:1 TX module

The LVDS 7:1 RX module receives the video signal from the PC (or DVD, etc.) and converts it to a 7:1 source sync signal. The signal processing module processes and converts the data signal to the RGB signal required by the LCD. The LVDS 4:1 TX module converts the RGB signal to a mini-LVDS signal that can drive the LCD screen.

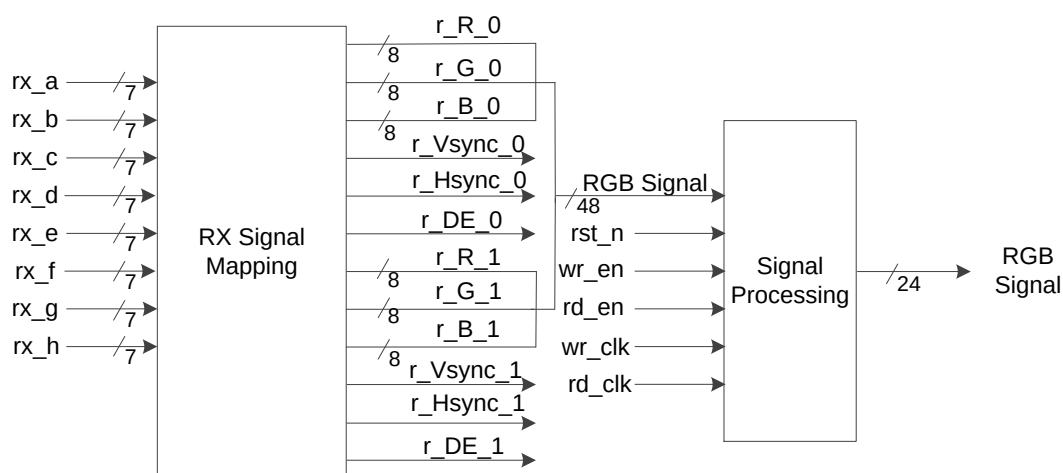
4.2 LVDS 7:1 RX Module

The LVDS 7:1 RX module receives the video signal via the LVDS differential interface. It parallel processes the differential signal and converts it to a 7:1 low-speed data signal. It then generates 3.5 times and 1.75 times clocks based on the input clock signal using PLL and CLKDIV and handles the wobble and deflection of the clock using the alignment module. Figure 4-1 contains the function diagram of the LVDS 7:1 RX module.

Figure 4-1: Function Diagram of LVDS 7:1 Rx Module

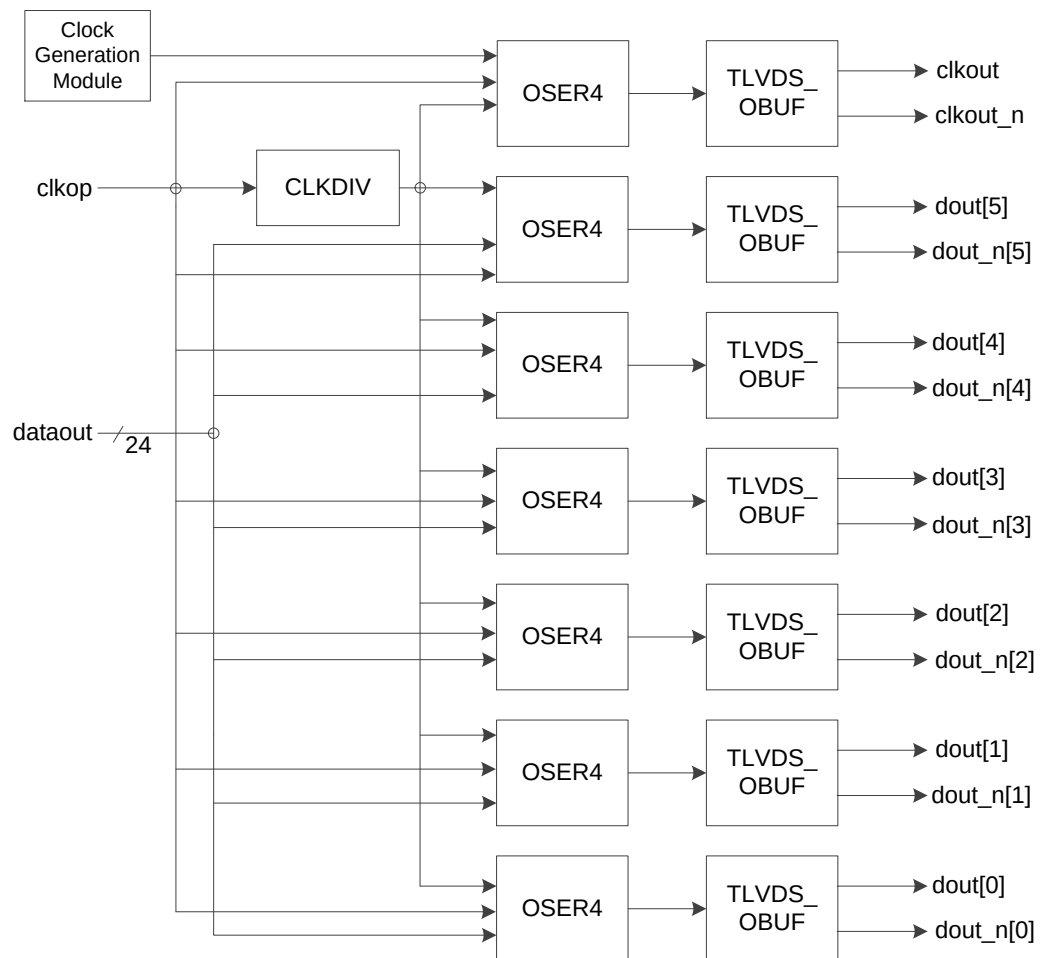
4.3 DSP

DSP supports signal mapping processing for the data signal transmitted by the LVDS 7:1 RX module to receive two-channel RGB signals, line/field signal, and enable the control signal to synchronously transmit with the pixel clock. Four-channel 24-bit RGB signals will be achieved by adjusting the two-channel 8-bit RGB signals. Figure 4-2 shows the function diagram of one 24-bit RGB signal conversion.

Figure 4-2: Function Diagram of the 24-Bit RGB Signal Conversion

4.4 LVDS 4:1 TX Module

Based on the sampling clock of the clock signal outputted by the LVDS 7:1 RX module, the LVDS 4:1 TX module converts the 24-bit data signal outputted by the signal processing module to 6-bit mini-LVDS signal and generates the clock signal required to drive the LCD screen. The function diagram of one LVDS 4:1 RX module is as shown in Figure 4-3.

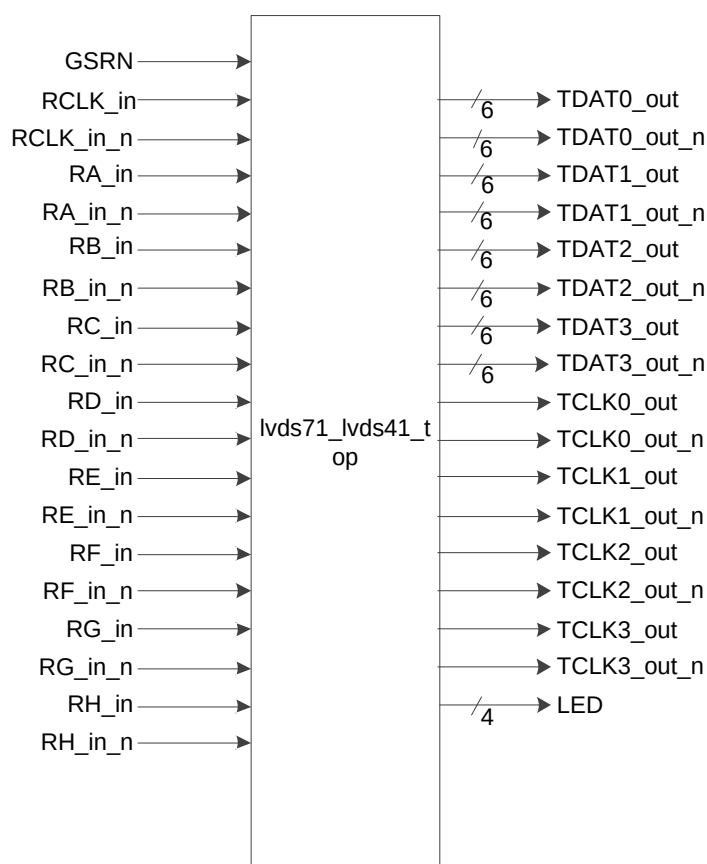
Figure 4-3: Function Diagram of LVDS 7:1 TX Module

5 Description of Ports

5.1 Diagram of Ports

The port diagram of the LVDS 7:1 RX LVDS 4:1 TX Reference Design is shown in Figure 5-1.

Figure 5-1: LVDS 7:1 RX LVDS 4:1 TX Reference Design Ports



5.2 Port Signals

The port signals of the LVDS 7:1 RX LVDS 4:1 TX Reference Design are shown in Table 5-2.

Table 5:2 LVDS 7:1 RX LVDS 4:1 TX Reference Design Port Signal

Port Name	Port Type	Description
GSRN	input	Reset signal
RCLK_in	input	Clock differential signal
RCLK_in_n	input	Clock differential signal
RA_in	input	Differential signal of data Channel A
RA_in_n	input	Differential signal of data Channel A
RB_in	input	Differential signal of data Channel B
RB_in_n	input	Differential signal of data channel B
RC_in	input	Differential signal of data Channel C
RC_in_n	input	Differential signal of data channel C
RD_in	input	Differential signal of data channel D
RD_in_n	input	Differential signal of data Channel D
RE_in	input	Differential signal of data Channel E
RE_in_n	input	Differential signal of data Channel E
RF_in	input	Differential signal of data Channel F
RF_in_n	input	Differential signal of data Channel F
RG_in	input	Differential signal of data Channel G
RG_in_n	input	Differential signal of data Channel G
RH_in	input	Differential signal of data Channel H
RH_in_n	input	Differential signal of data Channel H
TCLK0_out	output	Synchronous clock source CLK0
TCLK0_out_n	output	Synchronous clock source CLK0
TCLK1_out	output	Synchronous clock source CLK1
TCLK1_out_n	output	Synchronous clock source CLK1
TCLK2_out	output	Synchronous clock source CLK2
TCLK2_out_n	output	Synchronous clock source CLK2

Port Name	Port Type	Description
TCLK3_out	output	Synchronous clock source CLK3
TCLK3_out_n	output	Synchronous clock source CLK3
TDAT0_out[5:0]	output	Output serial data at port TX of 0-channel
TDAT0_out_n[5:0]	output	Output serial data at port TX of 0-channel
TDAT1_out[5:0]	output	Output serial data at port TX of 1-channel
TDAT1_out_n[5:0]	output	Output serial data at port TX of 1-channel
TDAT2_out[5:0]	output	Output serial data at port TX of 2-channel
TDAT2_out_n[5:0]	output	Output serial data at port TX of 2-channel
TDAT3_out[5:0]	output	Output serial data at port TX of 3-channel
TDAT3_out_n[5:0]	output	Output serial data at port TX of 3-channel
LED[3:0]	output	Status/debug port

6Timing Description

This chapter introduces the input signal timing of the LVDS 7:1 RX LVDS 4:1 TX Reference Design.

6.1 Input Signal Timing

The LVDS 7:1 RX LVDS 4:1 TX Reference Design is used to receive the video signals sent by the PC, including one clock channel RCLK_in, 8 data channels (RA_in, RB_in, RC_in, RD_in, RE_in, RF_in, RG_in and RH_in), and a pair of differential data lines, which can transmit 7-bit data and signal timing, as shown in Figure 6-1.

Figure 6-1: Input Signal Timing of LVDS 7:1 RX LVDS 4:1 TX Reference Design

