



# Gowin RAM Based Shift Register Reference Design

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# 1 About This Manual

## 1.1 Manual Content

Main content of Gowin RAM Based Shift Register IP reference design includes port description, configuration call, and reference design and so on. It is mainly used to help users quickly understand the product features and usage of Gowin RAM Based Shift Register IP.

## 1.2 Applicable Products

The information described in this manual applies to the following products:

1. GW1N Series of FPGA Products
2. GW1NR Series of FPGA Products
3. GW2A Series of FPGA Products
4. GW2AR Series of FPGA Products

## 1.3 Related Documents

The latest user guides are available on the Gowin website. Refer to the related documents at [www.gowinsemi.com](http://www.gowinsemi.com):

1. GW1N Series of FPGA Product Data Sheet
2. GW1NR Series of FPGA Product Data Sheet
3. GW2A Series of FPGA Product Data Sheet
4. GW2AR Series of FPGA Product Data Sheet
5. Gowin YunYuan Software User Guide

## 1.4 Terms and Abbreviations

The abbreviations and terminology used in this manual are as shown in  
错误!未找到引用源。 below.

**Table 1-1 Terms and Abbreviations**

| Terms and abbreviations | Full name                          |
|-------------------------|------------------------------------|
| FIFO                    | First Input First Output           |
| IP                      | Intellectual Property              |
| RAM                     | Random Access Memory               |
| BSRAM                   | Block Static Random Access Memory  |
| SSRAM                   | Shadow Static Random Access Memory |
| OSC                     | Oscillator                         |
| LUT                     | Look-up Table                      |
| GSR                     | Global System Reset                |

## 1.5 Technical Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

URL: [www.gowinsemi.com](http://www.gowinsemi.com)

E-mail: [support@gowinsemi.com](mailto:support@gowinsemi.com)

Tel: +86 755 8262 0391

# 2Reference Design

This reference design can be used to simply verify the functionality of the Gowin RAM Based Shift Register IP, or to learn and familiarize with the Gowin RAM Based Shift Register IP.

The reference design described in this document includes three shift types of Gowin RAM Based Shift Register IP. The reference designs are:

- Fixed shift Fixed\_ex
- Lossy variable shift Lossy\_ex
- Lossless variable shift Lossless\_ex

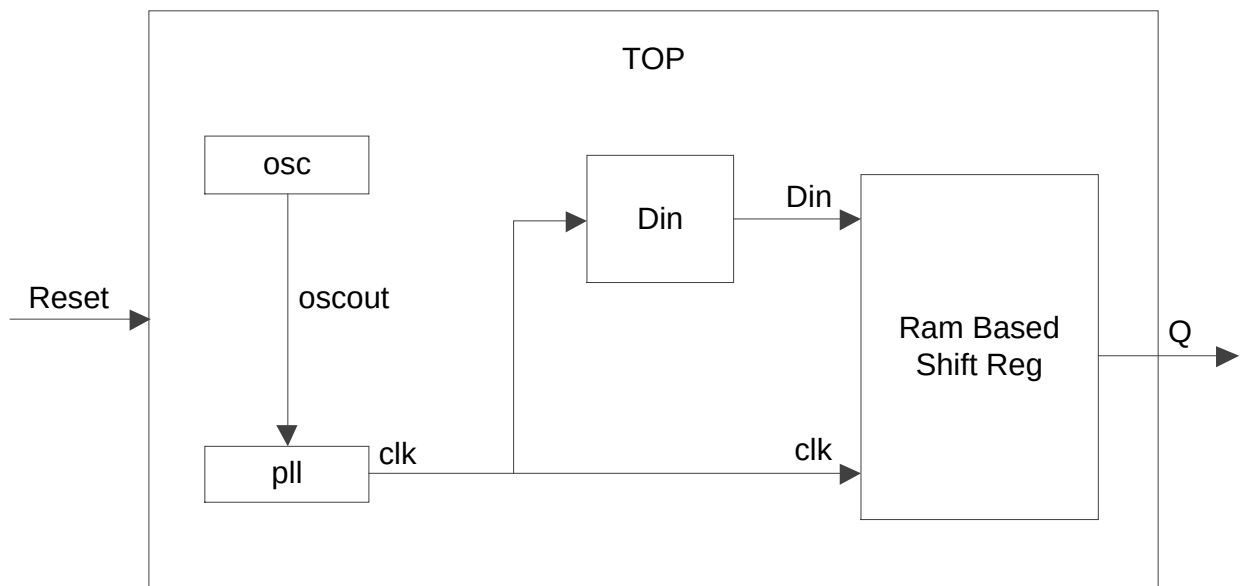
## 2.1 Reference Design Fixed\_ex

In this design example, Gowin RAM Based Shift Register IP selects the fixed shift mode, the basic structure of which is shown in Figure 2-1. The selection device for the reference design is GW2A-55, packaged as PBGA484, with a speed class of 8.

The "TOP" generates the shift value and the data for input, and "Example RAM Based Shift Register" module is implemented by the IP core generator, and the data is output after corresponding shift processing..

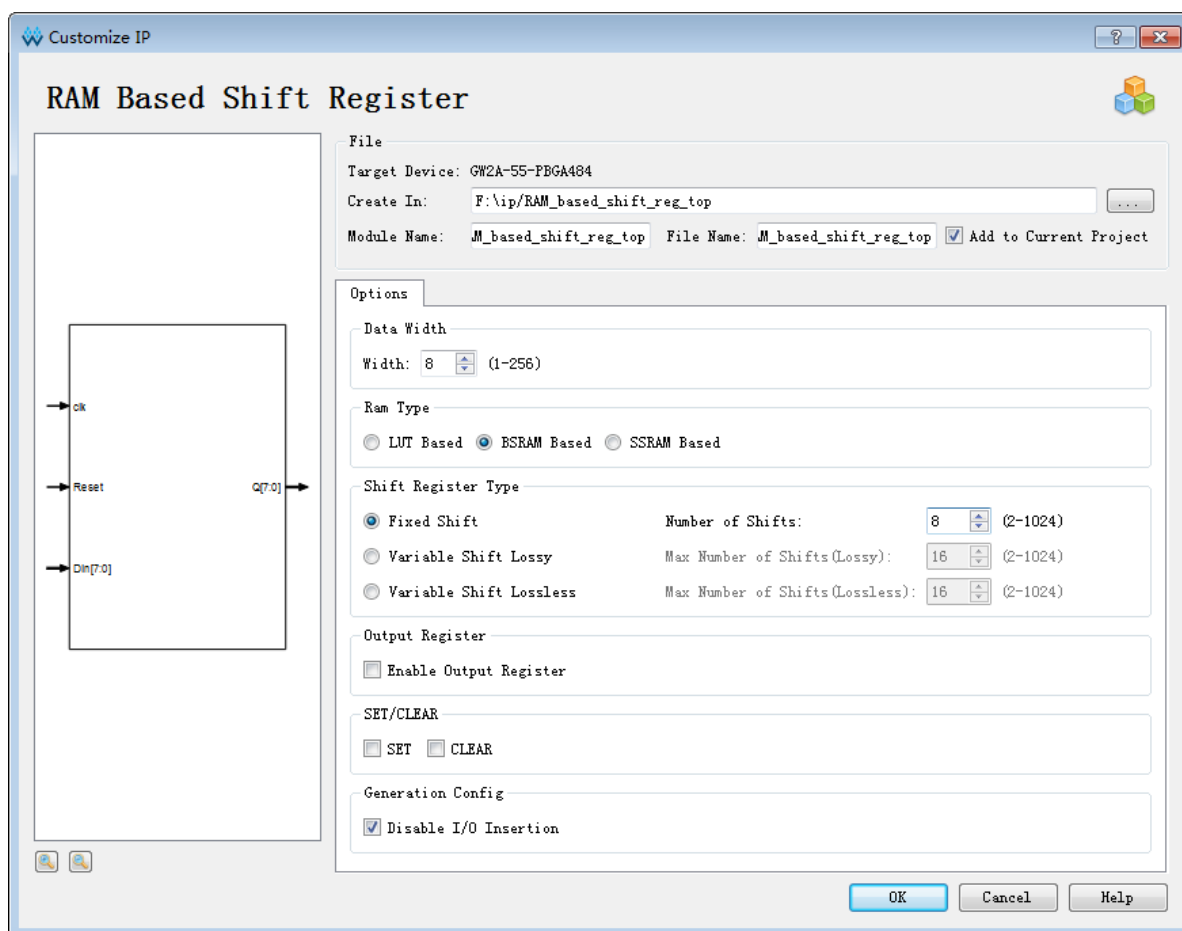
The configuration shift length (Number of Shifts) is 8, and the input data will be output after 8 clock cycles. The clock is generated by the "OSC" module and the input data "Din" changes with the clock.

**Figure 2-1 Basic Structure of the RAM Based Shift Register IP Fixed Shift Example Design**



In this reference design, the corresponding shift length (Number of Shifts) will be set in the IP core settings interface. An example of the IP core configuration is shown in Figure 2-2. As shown in the figure, the input data will be output after 8 clock cycles.

Figure 2-2 Fixed Shift IP Core Configuration Example



Related settings are completed; synthesis, place and route are correct; use the online logic analyzer to view the results.

The input is output after (12-4) 8 cycles as shown in Figure 2-3.

Figure 2-3 Example Results



## 2.2 Reference Design Lossy\_ex

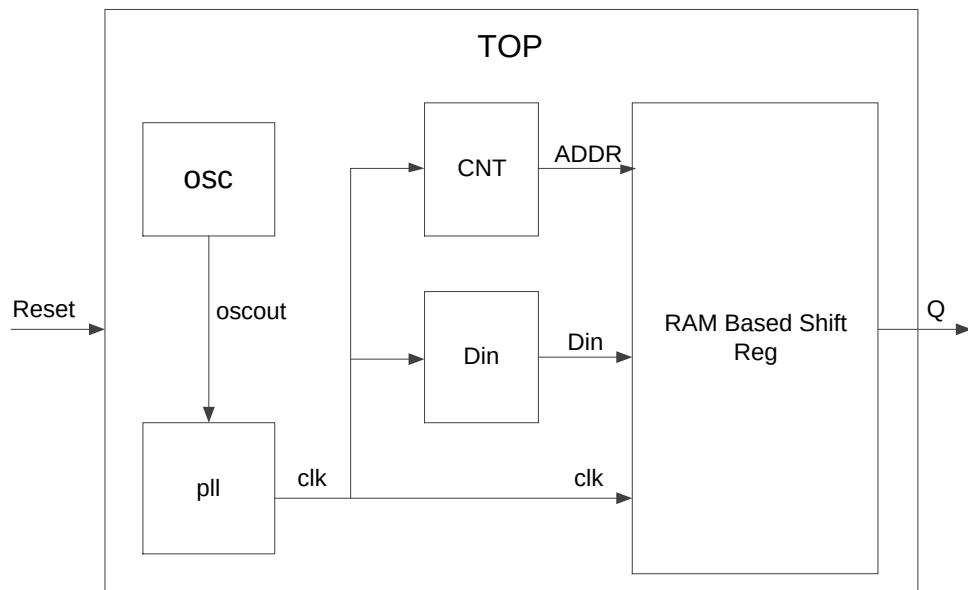
In this design example, Gowin RAM Based Shift Register IP selects the lossy variable shift mode, the basic structure of which is shown in Figure 2-4. The selection device for the reference design is GW2A-55, packaged as PBGA484, with a speed class of 8.

The "TOP" generates the shift value and the data for input, and

"Example RAM Based Shift Register" module is implemented by the IP core generator, and the data is output after corresponding shift processing..

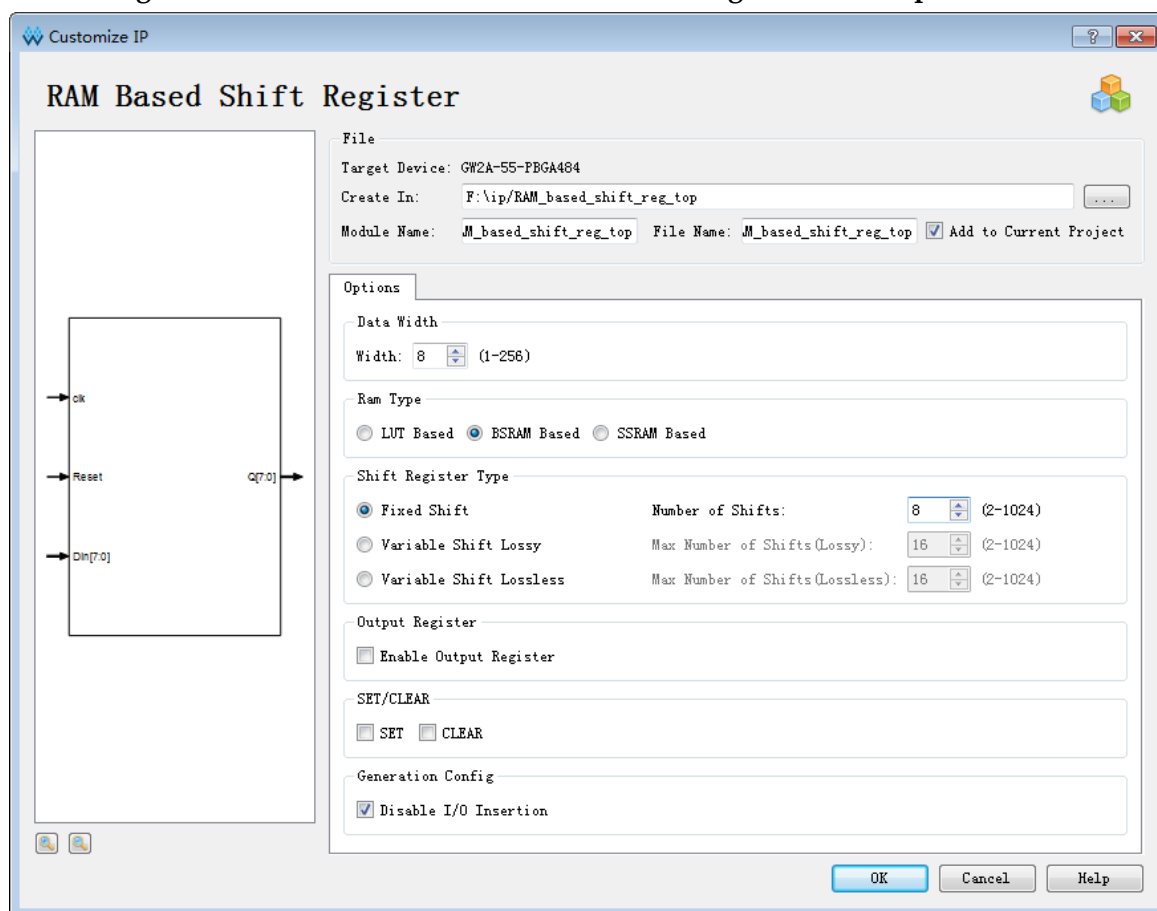
The clock is generated by the "OSC" module and the input data "Din" changes with the clock. The shift length "ADDR" is configured by the counter module "CNT". When the counter satisfies certain conditions, the shift length "ADDR" changes, the counter is set to 0, and the count is re-counted.

**Figure 2-4 Basic Structure of the RAM Based Shift Register IP Variable Shift Example Design**



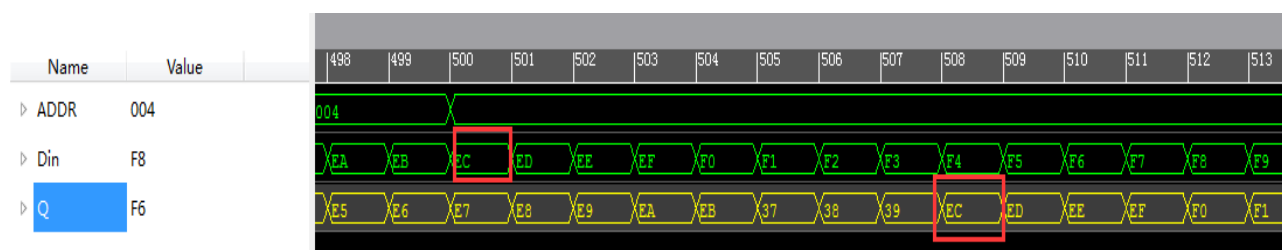
An example of the IP core configuration of this reference design is shown in Figure 2-5.

Figure 2-5 Lossable Variable Shift IP Core Configuration Example



After the related settings are completed and the synthesis, place and route are correct, the online logic analyzer can be used to view the results. As shown in Fig. 26, "ADDR" is changed from 4 to 7 and the input data "EC" is output after 8 (ADDR + 1) clock cycles.

Figure 2-6 Example Results



## 2.3 Reference Design Lossless\_ex

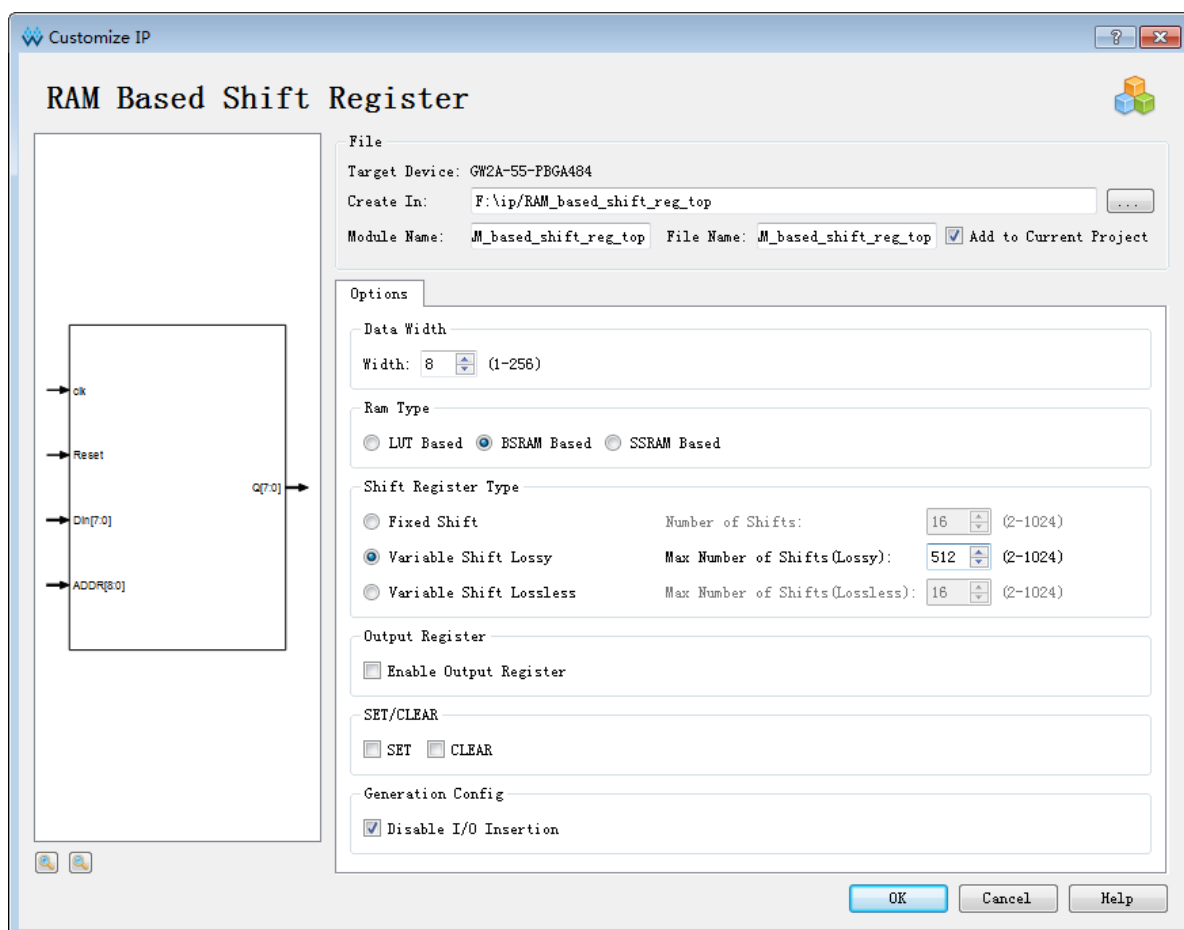
In this design example, Gowin RAM Based Shift Register IP selects the lossless variable shift mode. Its structure and data configuration are similar to the reference design Lossy\_ex. The structure is shown in Figure 2-4.

The clock is generated by the "OSC" module, and the input data "Din"

changes with the clock. The shift length "ADDR" is configured by the counter module "CNT". When the counter satisfies certain conditions, the shift value "ADDR" changes, the counter is set to 0, and the count is re-counted.

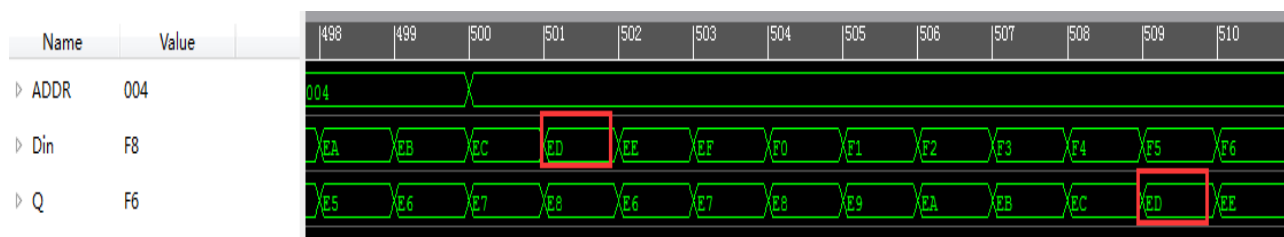
An example of the IP core configuration for this reference design is shown in Figure 2-7.

**Figure 2-7 Lossless Variable Shift IP Core Configuration Example**



After the related settings are completed and the synthesis, place and route are correct, the online logic analyzer can be used to view the results. As shown in Fig. 2-8, "ADDR" is changed from 4 to 7, and the output value "ED" is the data input before "ADDR+1" clock cycles.

**Figure 2-8 Example Results**



# 3Port Description

This chapter mainly introduces the IO port of the reference design. The reference design is relatively simple. The user only needs to configure the Reset signal. The IO ports of the three reference designs are the same, as shown in Table 3-1.

**Table 3-1 IO Port of the Sample Program**

| Name  | I/O    | Bit width | Comment                                       |
|-------|--------|-----------|-----------------------------------------------|
| Reset | Input  | 1         | Reset signal, high reset;                     |
| Q     | Output | Variable  | Output Data;<br>The bit width is [DSIZE-1:0]; |

**Note!**

In this example design, clk is generated by using an oscillator.

# 4Delivery Documents

The delivery documents for the RAM Based Shift Register reference design are shown in Table 4-1.

**Table 4-1 Delivery Documents**

| Delivery document           | Document content                          | File path                              |
|-----------------------------|-------------------------------------------|----------------------------------------|
| RAM_Based_Shift_Register_IP | User Manual and Reference Design Document | RAM_Based_Shift_Register_IP/doc        |
|                             | Reference design example project          | RAM_Based_Shift_Register_IP/project    |
|                             | Simulation related files                  | RAM_Based_Shift_Register_IP/simulation |

