



Gowin FIFO

Release Note

RN105-1.1E, 03/28/2019

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Revision History

Date	Version	Description
03/1/2019	1.0E	FIFO/FIFO_SC supported by IP Core Generator.
03/28/2019	1.1E	Supported products updated.

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About This Release

This release includes FIFO/FIFO_SC IP. The soft core of FIFO/FIFO_SC can be generated by IP Core Generator.

Overview

Gowin FIFO/FIFO_SC IP provides users a first-in-first-out queue to exchange data.

Table 1 FIFO/ FIFO_SC Overview

PSRAM Memory Interface	
IP Core Application	
Supported Devices	● GW1N Series; ● GW1NR Series; ● GW1NS Series; ● GW1NSR Series; ● GW1NZ Series; ● GW2A Series; ● GW2AR Series;
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	Synplify_Pro
Application Software	GowinYunYuan

Documents

The file released together with this IP contains Gowin FIFO User Guide, which is listed below:

Documents	
Gowin FIFO User Guide.pdf	PDF
Gowin FIFO Release Note.pdf	PDF

IP Support

For the customized IP design and support, please contact Gowin sales and support line.

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