



Gowin Serial RapidIO IP

User Guide

IPUG1023-1.1E, 10/25/2024

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Revision History

Date	Version	Description
08/18/2023	1.0E	Initial version published.
12/08/2023	1.0.1E	Table 4-1 Serial RapidIO IP Parameter Configuration updated.
10/25/2024	1.1E	● CTC function added. ● "AFE" configuration option added.

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1 About This Guide

1.1 Purpose

Gowin Serial RapidIO IP User Guide is to help you learn the features and usage of Gowin Serial RapidIO IP by providing descriptions of functions, GUI, and reference design, etc. The software screenshots in this manual are based on 1.9.10.03. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com.

- [SUG100, Gowin Software User Guide](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1104, GW5AST series of FPGA Products Data Sheet](#)

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
ackID	acknowledgement identifier
CAR	Capability Register
Control Symbol	A quantum of information transmitted between two linked devices to manage packet flow between the devices
CRC	Cyclic Redundancy Code
CRF	Critical Request Flow
CSR	Command and Status Register
Destination	The termination point of a packet on the RapidIO interconnect, also referred to as a target
Device	A generic participant on the RapidIO

Terminology and Abbreviations	Meaning
	interconnect that sends or receives RapidIO transactions, also called a processing element
Device ID	The identifier of an end point processing element connected to the RapidIO interconnect.
Doorbell	A port on a device that is capable of generating an interrupt to a processor
Double-word	An eight byte quantity, aligned on eight byte boundaries.
End point	A processing element which is the source or destination of transactions through a RapidIO fabric
FPGA	Field Programmable Gate Array
Ftype	Format Type
IP	Intellectual Property
Mailbox	Dedicated hardware that receives messages
Operation	A set of transactions between end point devices in a RapidIO system (requests and associated responses) such as a read or a write
Packet	A set of information transmitted between devices in a RapidIO system
PCS	Physical Coding Sublayer
PMA	Physical Media Attachment
Priority	The relative importance of a transaction or packet; in most systems a higher priority transaction or packet will be serviced or transmitted before one of lower priority
rdsiz	Read Size
srcTID	The Packet's Transaction ID
Transaction	A specific request or response packet transmitted between end point devices in a RapidIO system
Ttype	Transaction Type
wdptr	Word Pointer
wrsiz	Write Size

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Function

2.1 Overview

Gowin Serial RapidIO IP is designed in accordance with RapidIO protocol V2.1 and is applied to Endpoint Device in RapidIO system. The IP contains the Logical Layer, Transport Layer, and Physical Layer as defined in the protocol, and provides user independent TX/RX Request Transaction interfaces, TX/RX Response Transaction interfaces, and Maintenance Transaction interface.

Table 2-1 Gowin Serial RapidIO IP Overview

Gowin Serial RapidIO IP	
Logic Resource	See Table 2-2
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9 Beta-2 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features

General Feature

- Designed in accordance with RapidIO protocol V2.1

Logic Layer Features

- Supports RX/TX for read transactions (NREAD), write transactions (NWRITE), write transactions with response (NWRITE_R), streaming write transactions (SWRITE), response transactions (RESPONSE), message transactions (MESSAGE), doorbell transactions (DOORBELL), Atomic transactions, and maintenance transactions (MAINTENANCE).
- Can select fixed priority or round robin mode for Arbiter

Transport Layer Features

- Supports device ID (DeviceID) with 8-bit and 16-bit width

Physical Layer

- Supports x1, 2x, x4 lanes
- Supports line rates: 1.25Gbps, 2.5Gbps, 3.125Gbps, and 5.0Gbps
- Supports receiver flow control
- Supports IDLE1
- Supports buffer depth with 8/16/32
- Supports dynamic release of packet buffer resources
- Supports packet retransmission
- Supports packet error recovery

Note!

- It does not support falling back from 2x/4x to 1x, or from 4x to 2x currently.
- 5Gbps 2x mode and 2.5Gbps/3.125Gbps/5Gbps 4x mode are not supported currently.
- Transmitter flow control is not supported currently.
- Critical request flow is not supported currently.

2.3 Resource Utilization

Gowin Serial RapidIO IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different density, speed, or grade. Taking Gowin GW5AT series of FPGA as an instance, the resource utilization of Serial RapidIO IP is as shown in Table 2-2.

Table 2-2 Gowin Serial RapidIO IP Resource Utilization

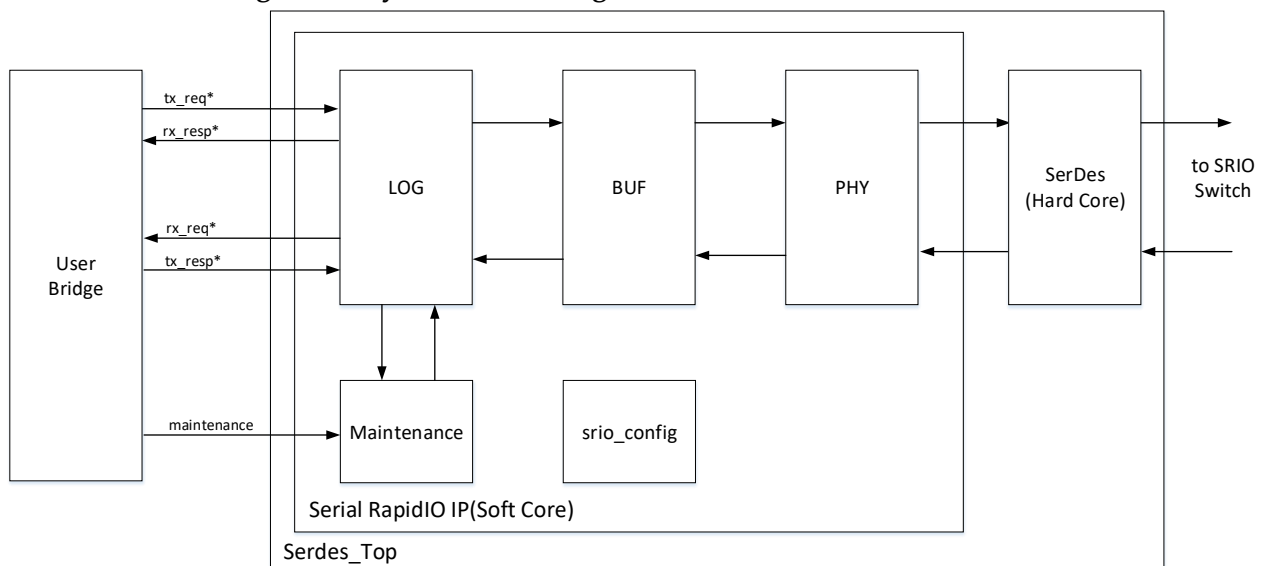
Lane Width	Buffer Depth	Resource Utilization				
		Register	LUT	ALU	BSRAM	SSRAM
1x	8	7069	6506	610	20	0
	16	7141	6543	631	24	0
	32	7233	6722	680	32	0
2x	8	7369	6662	628	20	0
	16	7441	6793	649	24	0
	32	7533	6933	698	32	0
4x	8	8668	7021	670	20	0
	16	8740	7235	691	24	0
	32	8832	7215	740	32	0

3 Functional Description

3.1 System Block Diagram

The system block diagram of Gowin Serial RapidIO IP is shown in Figure 3-1. The IP contains the logical layer, transport layer, and physical layer as defined by the RapidIO protocol, Buffer mechanism, Capability Registers (CAR) and Command and Status Registers(CSR) specified by the protocol. The IP provides user interfaces for RX/TX Request Transaction, TX/RX Response Transaction, and Maintenance Transaction.

Figure 3-1 System Block Diagram



Note!

The system block diagram interface is described as follows:

- tx_req*: Transmit request transaction interface
- rx_resp*: Receive response transaction interface
- rx_req*: Receive request transaction interface
- tx_resp*: Transmit response transaction interface
- maintenance: Maintain transaction access interface

3.2 Module Functions

This section describes the functions of each submodule of Gowin Serial RapidIO IP.

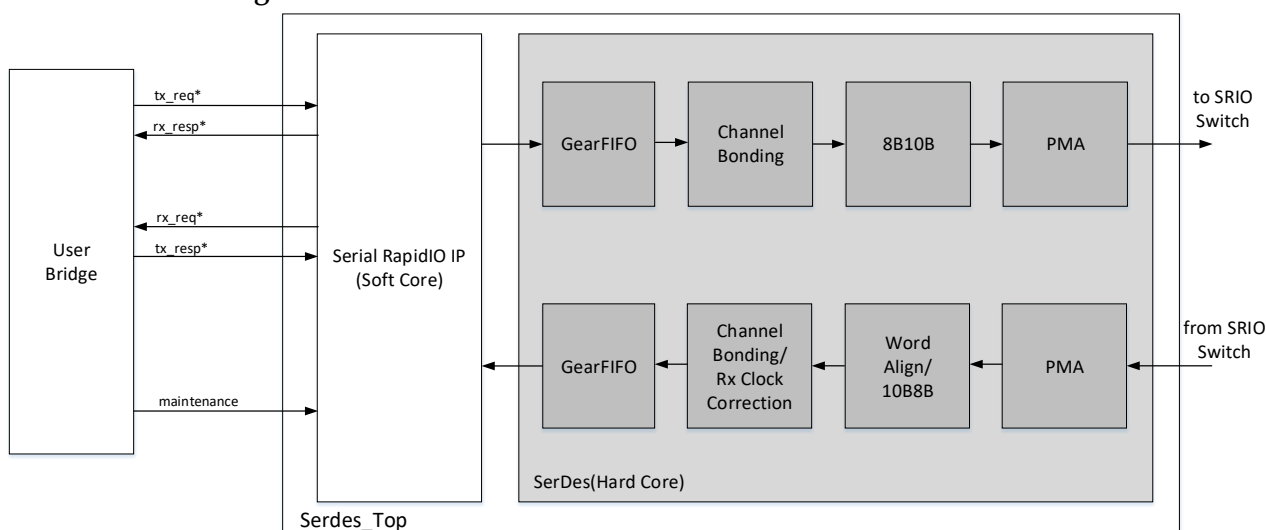
3.2.1 SerDes Module

SerDes Module: Uses Gowin FPGA's internal SerDes Hard Core, and supports 8B10B encoding/decoding, Channel Bonding, and RX Clock Correction.

The PCS clock frequency corresponding to the output data of the SerDes module is related to the line rate, and the PCS clock is used on the Fabric side of the SerDes GearFIFO, and the PCS clock is also used in part of the PHY module.

- When the line rate is 1.25Gbps, the PCS clock is 31.25M.
- When the line rate is 2.5Gbps, the PCS clock is 62.5M.
- When the line rate is 3.125Gbps, the PCS clock is 78.125M.
- When the line rate is 5Gbps, the PCS clock is 125M.

Figure 3-2 SerDes Module



3.2.2 LOG Module

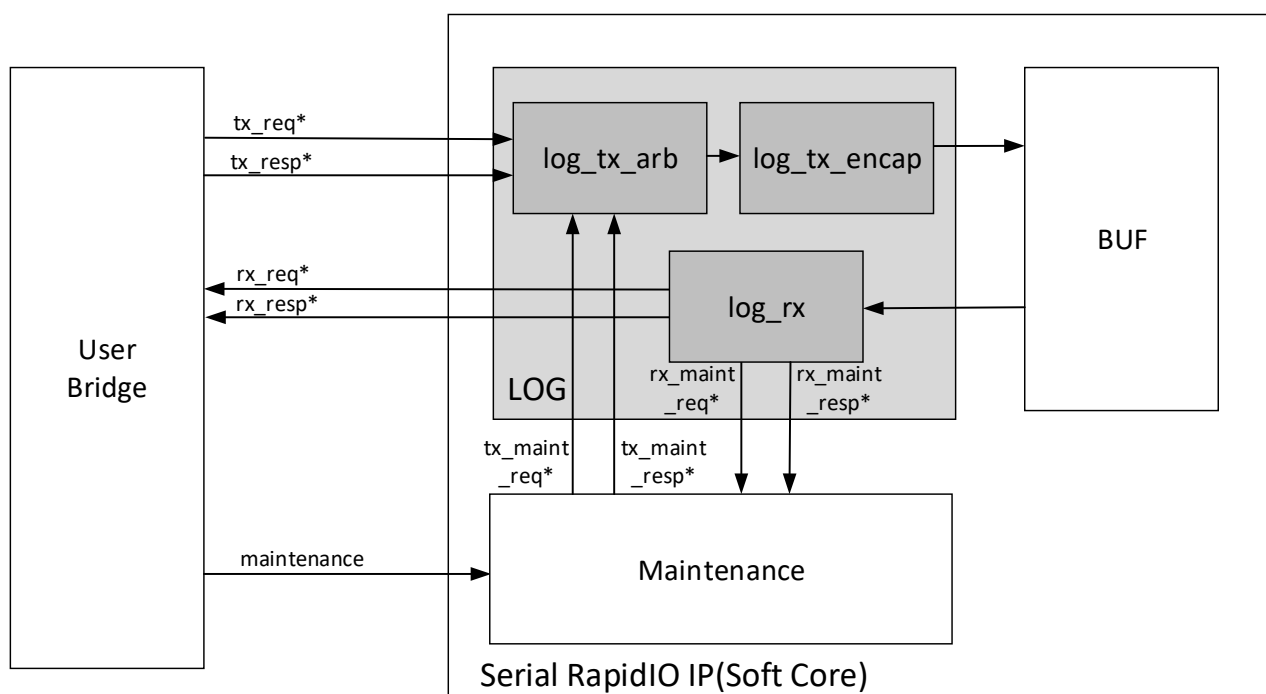
LOG module: Corresponds to the logic and transport layers of the RapidIO protocol, containing the TX and RX.

- TX: The sub-module log_tx_arb arbitrates the four sets of signals input, which are TX maintenance request transaction, TX maintenance response transaction, TX request transaction, and TX response transaction. The sub-module log_tx_encap encapsulates the data according to the protocol and transmits it to the next-level BUF module.
- RX: The submodule "log_rx" parses the data according to the protocol and extracts four sets of signals, which are RX maintenance request transaction, RX maintenance response transaction, RX request transaction, and RX response transaction, and independent interfaces

are provided.

- Request transactions include read transactions (NREAD), write transactions (NWRITE), write transactions with response (NWRITE_R), streaming write transactions (SWRITE), Atomic transactions, message transactions (MESSAGE), doorbell transactions (DOORBELL).
- The Response transaction (Response) represents the response to the request transaction.
- Maintenance request transactions are used to operate on protocol-defined registers, including write register or read register operations.
- The Maintenance response transaction represents a response to a maintenance request transaction.

Figure 3-3 LOG Module Block Diagram



3.2.3 BUF Module

BUF module: Corresponds to the Buffer mechanism in RapidIO protocol and includes RX/TX buffers; there are three depths of 8/16/32 on the GUI.

- In the TX direction, the transaction packets are put into different queues according to their priority, and there is a separate queue for each of the four priority levels. In the TX direction, when the physical layer is idle and ready to transmit packets, it prioritizes transmitting transactions with higher priority first. An acknowledgement identifier (ackID) is added to each transmitted transaction packet. The corresponding transaction packet is released in the queue only if the counterpart device returns the transaction packet is correctly received, otherwise it will re-transmit the transaction packet that encountered an error during the previous transmission.

- In the RX direction, data packets from the physical layer are sequentially placed into a FIFO, and the data is then transferred to the LOG module.

3.2.4 PHY Module

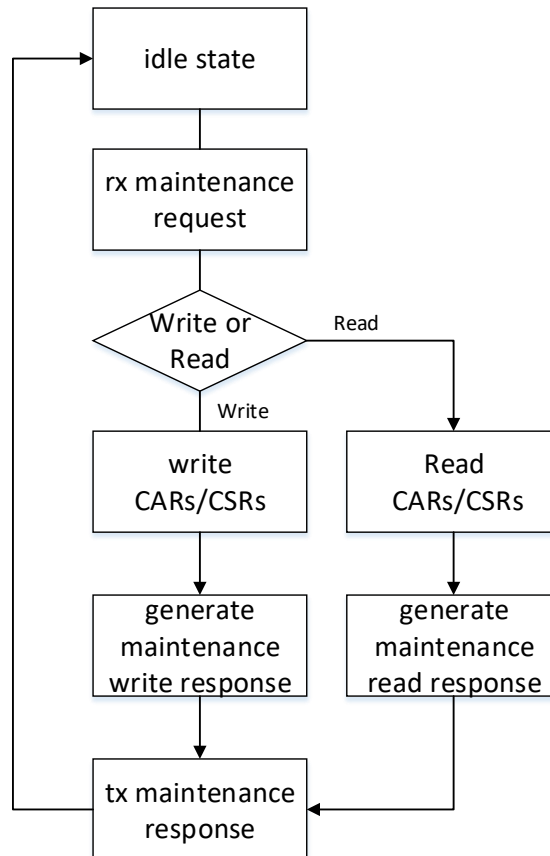
PHY module: Corresponds to the physical layer in RapidIO protocol, including TX/RX.

- In the TX direction, it includes adding a CRC to the transaction packet, generating the Control Symbol, merging the Control Symbol and the transaction packet, performing clock domain crossing on the merged data, and filling IDLE sequence between the packets.
- In the RX direction, it includes port initialization, link initialization, clock domain crossing on the data, extraction of transaction packets and control symbols from the received data, and CRC, and corresponding operations based on the received control symbols.

3.2.5 Maintenance Module

Maintenance module: Handles maintenance transactions and contains three functions; one is to handle maintenance operations initiated by remote devices to access local registers; one is to handle maintenance operations initiated by local devices to access remote registers, and the last one is the local device accessing the local register.

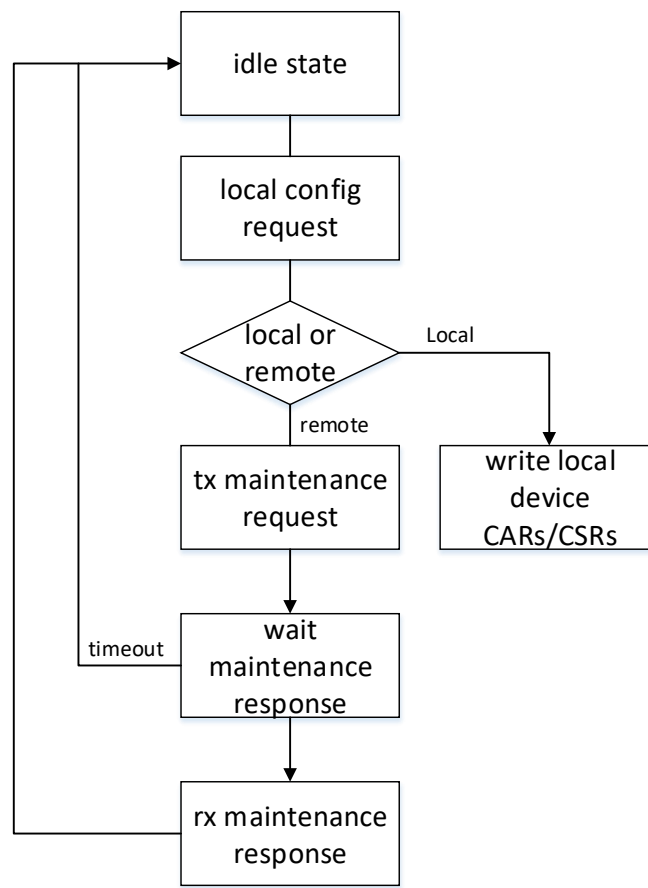
- Maintenance operations initiated by remote devices to access local registers: Receives maintenance request transactions from the LOG layer, determines whether they are read or write operations, and then operates the registers maintained by the IP; a corresponding response transaction is generated after completion, and the response transaction is transmitted to the LOG layer.

Figure 3-4 Maintenance Flowchart of Remote Device Operating Local Device

- Maintenance operations initiated by local devices to access remote registers: Receives register read/write operations initiated by the local device through the configuration interface, determines whether the operation is to access a local or remote register; if it's accessing a remote register, transmit a maintenance request transaction to the LOG layer and wait for the LOG layer to receive the maintenance response transaction. If the response transaction is correctly received, return the result through the local configuration interface. If it is timeout, a response is not received, return the error and set the maintenance_timeout_o signal.

Note!

For each maintenance transaction operation initiated by the local device to the remote device, you need to operate register 0x10100 and register 0x10104 and properly configure the request information (srcTID, prio, crf, Destination ID and hop count) of the maintenance transaction packet before initiating the request through the configuration interface.

Figure 3-5 Maintenance Flowchart of Local Device Operating Remote Device

- Local device accessing local registers: Receives register read/write operations initiated by the local device through the configuration interface, determines whether the operation is to access the local device or the remote device; if the local device is accessed, initiate register read/write to the Srio_config module and return the result to the configuration interface.

3.2.6 Srio_config Module

Srio_config module: Defines the capability registers and command status registers of the local device according to the RapidIO protocol. The srio_config module can be accessed by the remote device or the local device to perform read/write register operations.

3.3 User Interface

The user interfaces provided by Gowin Serial RapidIO are described below:

- Clock interface: The user inputs the operating clock of IP Core
- Reset interface: The user resets IP Core
- Transmit request transaction interface: I/O request transaction bus interface initiated by the user
- Transmit response transaction interface: I/O response transaction bus interface initiated by the user
- Receive request transaction interface: I/O request transaction bus interface received by the user
- Receive response transaction interface: I/O response transaction bus interface received by the user
- Maintenance interface: The maintenance transaction interface operated by user for accessing internal registers of local IP or accessing remote device registers
- Status interface: Port initialization status, link status and other debug-friendly port status
- SerDes-related interfaces: SerDes reset and SerDes status interfaces

3.4 Port List

The I/O port of Gowin Serial RapidIO IP is shown in Figure 3-6.

Figure 3-6 Gowin Serial RapidIO IP Port Diagram

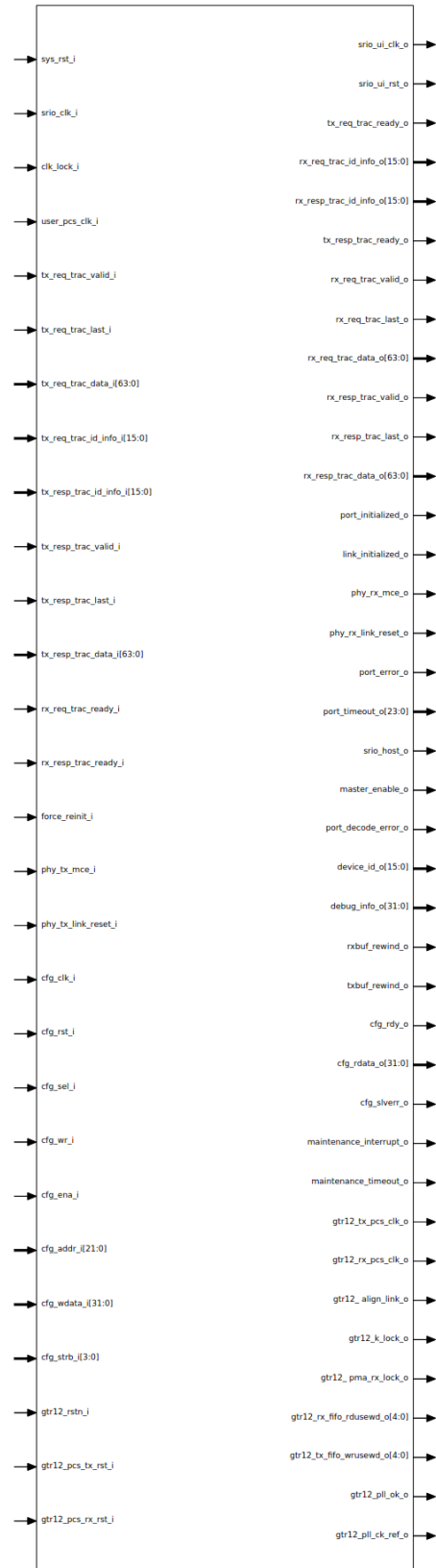


Table 3-1 I/O List of Gowin Serial RapidIO IP

Port Name	I/O	Data Width	Description
Clock and Reset			
sys_rst_i	input	1	Reset signal, active-high
srio_clk_i	input	1	Operating clock for LOG, BUF and some PHY; clock frequency is related to the configuration module. ● 1.25G 1x, 15.625M ● 1.25G 2x, 31.25M ● 1.25G 4x, 62.5M ● 2.5G 1x, 31.25M ● 2.5G 2x, 62.5M ● 3.125G 1x, 39.0625M ● 3.125G 2x, 78.125M ● 5G 1x, 62.5M Note! The operating clock frequency of another part of the PHY is the SerDes PCS layer operating clock frequency, see section 3.2.1 SerDes Module for details.
clk_lock_i	input	1	Operating clock PLL lock indicator; high indicates PLL lock.
user_pcs_clk_i	input	1	Input SerDes PCS layer operating clock, and need to be the same source as srio_clk_i: ● 1.25Gbps, 31.25M ● 2.5Gbps, 62.5M ● 3.125Gbps, 78.125M ● 5Gbps, 125M
srio_ui_clk_o	output	1	The output operating clock; the input srio_clk_i can be directly output; it can be used directly by the user side.
srio_ui_rst_o	output	1	Output reset signal, active-high; it can be used directly by the user side.
cfg_rst_i	input	1	Synchronous reset signal of configuration module, active-high.
cfg_clk_i	input	1	Operating clock of configuration module
Transmit Request Transaction Interface			
tx_req_trac_valid_i	input	1	Data valid indicator for the transmit request transaction interface, active-high.
tx_req_trac_ready_o	output	1	Handshake signal of the transmit request transaction interface. When tx_req_trac_ready_o and tx_req_trac_valid_i are high, the data on the bus is valid.
tx_req_trac_last_i	input	1	The end-of-packet indication signal of the transmit request transaction interface. When tx_req_trac_last_i ,

Port Name	I/O	Data Width	Description
			tx_req_trac_valid_i, and tx_req_trac_ready_o are high, indicating the last clock cycle of the transaction packet.
tx_req_trac_data_i	input	[63:0]	The data of the transmit request transaction interface, including the header and data of the transaction packet.
tx_req_trac_id_info_i	input	[N-1:0]	The ID information corresponding to the packet of the transmit request transaction interface; the bit width is related to the GUI option "Device ID Width". - When the GUI option "Device ID Width" is 8 bits, N is 16, where [7:0] corresponds to the Destination ID and [15:8] corresponds to the Source ID. - When the GUI option "Device ID Width" is 16 bits, N is 32, where [15:0] corresponds to the Destination ID and [31:16] corresponds to the Source ID.
Transmit Response Transaction Interface			
tx_resp_trac_valid_i	input	1	TX data valid indicator for the transmit response transaction interface, active-high.
tx_resp_trac_ready_o	output	1	Handshake signal of the transmit response interface. When tx_resp_trac_ready_o and tx_resp_trac_valid_i are high, the data on the bus is valid.
tx_resp_trac_last_i	input	1	The end-of-packet indication signal of the transmit response transaction interface. When tx_resp_trac_last_i, tx_resp_trac_valid_i, and tx_resp_trac_ready_o are high, indicating the last clock cycle of the transaction packet.
tx_resp_trac_data_i	input	[63:0]	The data of the transmit response transaction interface, including the header and data of the transaction packet.
tx_resp_trac_id_info_i	input	[N-1:0]	The ID information corresponding to the transmit response transaction interface packet, and the bit width is related to the GUI option "Device ID Width". When the GUI option "Device ID Width" is 8 bits, N is 16, where [7:0] corresponds to the Destination ID and [15:8]

Port Name	I/O	Data Width	Description
			corresponds to the Source ID. When the GUI option "Device ID Width" is 16 bits, N is 32, where [15:0] corresponds to the Destination ID and [31:16] corresponds to the Source ID.
Receive Request Transaction Interface			
rx_req_trac_ready_i	input	1	Handshake signal of the receive request transaction interface. When rx_req_trac_ready_i and rx_req_trac_valid_o are high, the data on the bus is valid.
rx_req_trac_valid_o	output	1	Data valid indicator for the receive request transaction interface, active-high.
rx_req_trac_last_o	output	1	The end-of-packet indication signal of the receive request transaction interface. When rx_req_trac_ready_i, rx_req_trac_valid_o, and rx_req_trac_last_o are high, indicating the last clock cycle of the transaction packet.
rx_req_trac_data_o	output	[63:0]	The data of receive request transaction interface, including the header and data of the transaction packet.
rx_req_trac_id_info_o	output	[N-1:0]	The ID information corresponding to the packet of the receive request transaction interface; the bit width is related to the GUI option "Device ID Width". - When the GUI option "Device ID Width" is 8 bits, N is 16, where [7:0] corresponds to the Destination ID and [15:8] corresponds to the Source ID. - When the GUI option "Device ID Width" is 16 bits, N is 32, where [15:0] corresponds to the Destination ID and [31:16] corresponds to the Source ID.
Receive Response Transaction Interface			
rx_resp_trac_ready_i	input	1	Handshake signal of the receive response transaction interface. When rx_resp_trac_ready_i and rx_resp_trac_valid_o are high, the data on the bus is valid.
rx_resp_trac_valid_o	output	1	Data valid indicator for the receive response transaction interface, active-high.
rx_resp_trac_last_o	output	1	The end-of-packet indication signal of the receive response transaction interface. When rx_resp_trac_ready_i,

Port Name	I/O	Data Width	Description
			rx_resp_trac_valid_o, and rx_resp_trac_last_o are high, indicating the last clock cycle of the transaction packet.
rx_resp_trac_data_o	output	[63:0]	The data of receive response transaction interface, including the header and data of the transaction packet.
rx_resp_trac_id_info_o	output	[N-1:0]	The ID information corresponding to the packet of the receive response transaction interface; the bit width is related to the GUI option "Device ID Width". - When the GUI option "Device ID Width" is 8 bits, N is 16, where [7:0] corresponds to the Destination ID and [15:8] corresponds to the Source ID. - When the GUI option "Device ID Width" is 16 bits, N is 32, where [15:0] corresponds to the Destination ID and [31:16] corresponds to the Source ID.
IP Core Control Interface			
force_reinit_i	input	1	Triggers the PHY layer to be re-initialized, active-high; for at least 2 clock cycles in the srio_ui_clk_o clock domain.
phy_tx_mce_i	input	1	Triggers the PHY layer to transmit the Multicast-event Control Symbol, active-high; for at least one clock cycle in the srio_ui_clk_o clock domain.
phy_tx_link_reset_i	input	1	Triggers the PHY layer to send the link-reset (link-request/reset-device) control symbol (Control Symbol), active high. The phy_tx_link_reset_i is set high in the srio_ui_clk_o clock domain to perform the link-reset operation. It is necessary to wait for the port_initialized_o to be pulled down to make sure that the counterpart has completed the reset, and then reset the phy_tx_link_reset_i to low again.
IP Core Status Signals			
port_initialized_o	output	1	Port initialization completion signal, active-high.
link_initialized_o	output	1	Link initialization completion signal, active-high.
phy_rx_mce_o	output	1	Multicast-event control symbol receive indicator for PHY layer, active-high. Every 1 clock cycle in the srio_ui_clk_o clock domain indicates the reception of

Port Name	I/O	Data Width	Description
			a Multicast-event control symbol.
phy_rx_link_reset_o	output	1	The PHY layer receives at least 4 consecutive link-reset control symbols, active-high. When at least 4 consecutive link reset control symbols are received, the IP performs a reset operation.
port_error_o	output	1	Port error indicator, active-high.
port_timeout_o	output	[23:0]	The port response timeout value, controlled by the Port Response Timeout Control register in the CSRs.
srio_host_o	output	1	Indicates that the system is a Host device, active-high, and controlled by the Port General Control register in the CSRs.
master_enable_o	output	1	Master enable signal, active-high, controlled by the Port General Control register in the CSRs.
port_decode_error_o	output	1	Port decoding error indicator, indicating that the logic layer has received an unsupported transaction type, active-high.
device_id_o	output	[15:0]	The ID information of the local device, controlled by the Base Device ID register in the CSRs.
debug_info_o	output	[31:0]	Debug information for PHY layer ● bit0~15, rsv ● bit16~20, the value of the ackID field expected in the next packet the port receives. ● bit21~23, rsv ● bit24~28, port status: - 5'd2 means the port has encountered an unrecoverable error and is unable to accept packets. - 5'd4 means the port has retried a packet and is waiting in the input retry-stopped state to be restarted. - 5'd5 means the port has encountered a transmission error and is waiting in the input error-stopped state to be restarted. - 5'd16 means the port is accepting packets. - 5'd0 means reset status. ● bit29~30, rsv

Port Name	I/O	Data Width	Description
			bit31: link multi-channel alignment indicator, active-high.
rxbuf_rewind_o	output	1	The retransmission indicator for the receive direction, active-high.
txbuf_rewind_o	output	1	The retransmission indicator for the transmit direction, active-high.
Configuration Interface			
cfg_sel_i	input	1	Chip selected enable signal and the clock domain is cfg_clk_i.
cfg_wr_i	input	1	Write control signal; High indicates that current operation is a write operation, and the clock domain is cfg_clk_i.
cfg_ena_i	input	1	Transmission enable signal; High indicates that current transmission is valid, and the clock domain is cfg_clk_i.
cfg_addr_i	input	[21:0]	Address line, byte address, and the clock domain is cfg_clk_i.
cfg_wdata_i	input	[31:0]	Write data bus, and the clock domain is cfg_clk_i.
cfg_strb_i	input	[3:0]	Byte valid indicator, reserved, and the clock domain is cfg_clk_i.
cfg_rdy_o	output	1	Ready signal, and the clock domain is cfg_clk_i. and the clock domain is cfg_clk_i.
cfg_rdata_o	output	[31:0]	Read data bus, and the clock domain is cfg_clk_i.
cfg_slvrr_o	output	1	Bus error indicator, active when cfg_rdy_o is high, and the clock domain is cfg_clk_i.
maintenance_interrupt_o	output	1	Maintenance transaction interrupt indicator, reserved, and the clock domain is cfg_clk_i.
maintenance_timeout_o	output	1	Maintenance transaction timeout indicator, active-high, indicating that the transaction timeout requested by the configuration interface did not receive a correct acknowledge, and the clock domain is cfg_clk_i.
User-side Control of SerDes-related Interfaces			
gtr12_rstn_i	input	1	SerDes channel reset signal, active-low; reset all lanes for the IP at the same time.
gtr12_pcs_tx_rst_i	input	1	SerDes PCS layer TX reset, active-high; reset all lanes for the IP at the same time.
gtr12_pcs_rx_rst_i	input	1	SerDes PCS layer RX reset, active-high; reset all lanes for the IP at the same time.

Port Name	I/O	Data Width	Description
gtr12_align_link_o	output	[N-1:0]	SerDes channel alignment status; high means the link is normal, the bit width corresponds to the number of lanes selected by the option Lane Width, 1 bit for x1, 2 bits for x2 and 4 bits for x4.
gtr12_k_lock_o	output	[N-1:0]	SerDes channel K character lock status; high means the link is normal, the bit width corresponds to the number of lanes selected by the option Lane Width, 1 bit for x1, 2 bits for x2 and 4 bits for x4.
gtr12_pma_rx_lock_o	output	[N-1:0]	SerDes channel RX PMA layer lock status; high means the link is normal, the bit width corresponds to the number of lanes selected by the option Lane Width, 1 bit for x1, 2 bits for x2 and 4 bits for x4.
gtr12_pll_ok_o	output	[N-1:0]	SerDes PLL lock status; High indicates clock lock. ● When QPLL1 or QPLL0 is selected for option PLL_Selection on the configuration interface, the bit width is 1 bit. ● When CPLL is selected for the option PLL_Selection on the configuration interface, the bit width corresponds to the number of lanes selected by the option Lane Width, which is 1 bit for x1, 2 bits for x2, and 4 bits for x4.
gtr12_pll_ck_ref_o	output	1	SerDes PLL reference clock output; The user uses this clock as the reference clock for the system PLL to regenerate the operating clock of the IP, refer to the reference design for details.
gtr12_rx_fifo_rdusewd_o	output	[N-1:0]	The difference between the read and write pointers of the SerDes channel RX FIFO; the bit width corresponds to the number of lanes selected by the option Lane Width. ● For x1, the width is 5 bits ● For x2, the width is 10 bits ● For x4, the width is 20 bits
gtr12_tx_fifo_wrusewd_o	output	[N-1:0]	The difference between the read and write pointers of the SerDes channel TX FIFO; the bit width corresponds to the number of lanes selected by the option Lane Width. ● For x1, the width is 5 bits ● For x2, the width is 10 bits ● For x4, the width is 20 bits

Port Name	I/O	Data Width	Description
gtr12_tx_pcs_clk_o	output	1	Clock for SerDes TX PCS layer
gtr12_rx_pcs_clk_o	output	1	Clock for SerDes RX PCS layer
SerDes Hard-core Interface			
SerDes_*	—	—	The signal with the beginning of SerDes_ is the connection signal of Serial RapidIO IP with SerDes hardcore; the user Users may not need to pay attention to it, the EDA tool will automatically complete the connection.

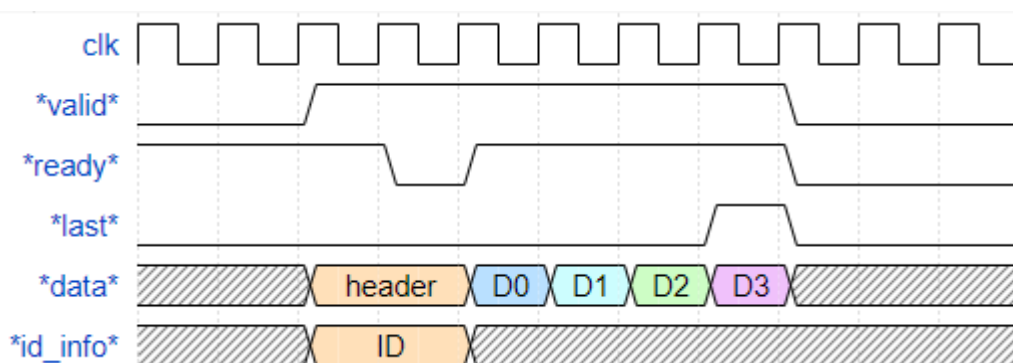
3.5 User Interface Timing

3.5.1 I/O Transaction Interface Timing Diagram

Gowin Serial RapidIO IP provides a valid & ready handshake interface for I/O transactions. I/O transactions include read transactions (NREAD), write transactions (NWRITE), write with response transactions (NWRITE_R), streaming write transactions (SWRITE), message transactions (MESSAGE), doorbell transactions (DOORBELL), and response transactions (RESPONSE) other than maintenance transactions.

The interface transaction is shown in Figure 3-7, and the first valid clock cycle of the bus is agreed as the Header information, and the remaining clock cycles are used as the data load. When **valid** and **ready** are high at the same time, the current data is valid; the first valid clock cycle corresponds to the Header information, which contains the current transaction packet type, transaction packet length, priority, etc. From the second valid clock cycle to the valid **last** signal, the transaction packet load is transmitted. It should be noted that some transaction packet types do not require a load, and here the **last** signal appears at the first valid clock cycle. The bit width of **data** is 64 bits, and the bit width of **id_info** is related to the Device ID Width option on the GUI. I/O transaction interfaces correspond to the Transmit Request Transaction Interface, Transmit Response Transaction Interface, Receive Request Transaction Interface, and Receive Response Transaction Interface in the Port List.

Figure 3-7 I/O Transaction Interface Timing Diagram



Header information is defined as shown in Figure 3-8. Header bit width is fixed at 64 bits and is passed in the first valid clock cycle of each transaction packet. R means reserved field (Reserved); E means error (Error); FTYPE means the packet format type; SrcTID means the source device transaction ID; Ttype means the transaction type; FTYPE and TTYPE are combined to be the unique identification of transaction format; prio means priority; crf means Critical Request Flow; addr means address; size means byte length; msglen means the number of packets comprising the MESSAGE sequence; msgseg means the message segment represented by the current transaction packet, and mailbox means the mailbox corresponding to the current transaction packet.

Figure 3-8 Header Definition

Packet Type	[63:56]		[55:48]		[47:40]			[39:32]			[31:24]		[23:16]		[15:08]		[07:00]			
NREAD	SrcTID 8		FTYPE2 4	TTYPE 4	R 1	prio 2	crf 1	Size-1 8	R 1	R 1	addr 34									
NWRITE	SrcTID 8		FTYPE5 4	TTYPE 4	R 1	prio 2	crf 1	Size-1 8	R 1	R 1	addr 34									
SWRITE	R 8		FTYPE6 4	R 4	R 1	prio 2	crf 1	R 8	R 1	R 1	addr 34									
DOORBELL	SrcTID 8		FTYPE10 4	R 4	R 1	prio 2	crf 1	R 8	R 1	R 1	R 2	Info MSB 8		Info LSB 8		R 16				
MESSAGE	msglen 4	msgseg 4	FTYPE11 4	R 4	R 1	prio 2	crf 1	Size-1 8	R 1	R 1	R 2	R 24					mailbox 6	R 2	letter 2	
RESPONSE	Target info 8		FTYPE13 4	TTYPE 4	R 1	prio 2	crf 1	R 8	E 1	R 1	R 34									
	Target TID 8																			

3.5.2 Configuration Interface Timing Diagram

Gowin Serial RapidIO IP provides configuration interface, through which users can access internal registers of the local IP or access the registers of remote devices. The configuration interface read timing is as shown in Figure 3-9, and the write timing is as shown in Figure 3-10. If the internal registers of local IP are accessed, there will be a response generated after a few clock cycles upon initiating the configuration request. However, if the registers of the remote device are accessed, it requires waiting for a long time before receiving the response. If the response is not received within the timeout value set for the local registers, the `maintenance_timeout_o` port will be pulled high to indicate that the request transaction has timed out.

Figure 3-9 Read Timing Diagram of cfg Interface

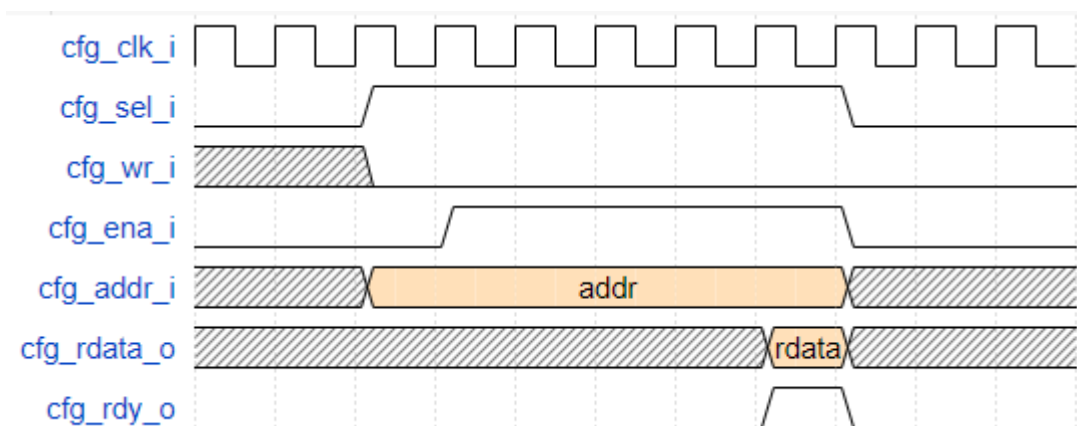
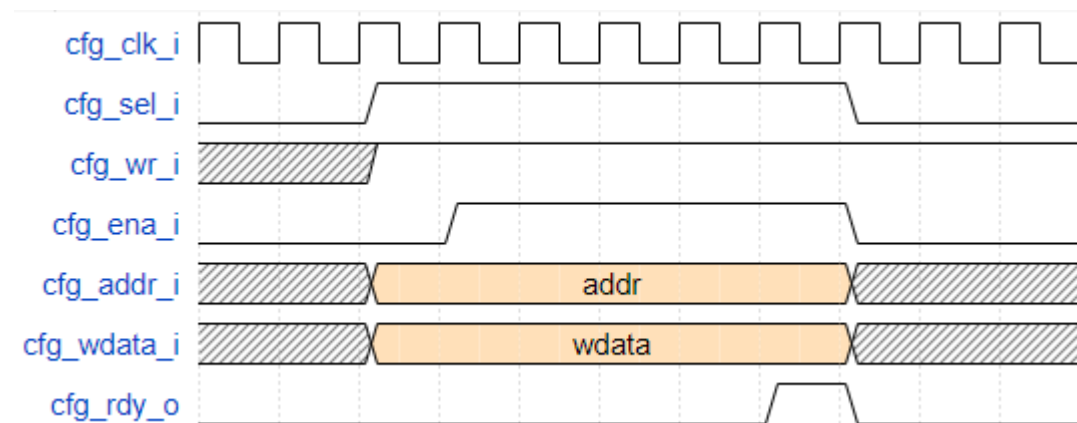


Figure 3-10 Write Timing Diagram of cfg Interface



3.6 Register Interface

Table 3-2 Register Address Space

Address Space (Byte)	Device Accessed	Description
0x200000~0x3ffffc	Remote devices	To access the register address space of the remote device, you can see the register definition of the remote device. bit21 is only used to distinguish whether to access the local device or the remote device. If bit21 is high, it will access the remote device, and the address (cfg_offset) transmitted to the remote device is low 21 bits (bit0~bit20).
0x000000~0x1ffffc	Local devices	To access the register address space of the local device, you can see the the following descriptions for the register definition. bit21 is only used to distinguish whether to access the local device or the remote device. If bit21 is low, it will access to the local device, and the actual access to the local device IP srio_config module is only low 21bit (bit0~20).

Table 3-3 Local Device Register List Overview

Address (Byte)	Name	Type	Description
0x00~0x3c CARs			
0x0	Device Identity CAR	RO	You can configure it on the GUI, and you can see the RapidIO protocol for details.
0x4	Device Information CAR	RO	You can configure it on the GUI, and you can see the RapidIO protocol for details.
0x8	Assembly Identity CAR	RO	You can configure it on the GUI, and you can see the RapidIO protocol for details.
0xc	Assembly Information CAR	RO	You can configure it on the GUI, and you can see the RapidIO protocol for details.
0x10	Processing Element Features CAR	RO	You can configure it on the GUI, and you can see the RapidIO protocol for details.
0x14	Switch Port Information CAR	RO	rsv
0x18	Source Operations CAR	RO	The type of operation supported by the source, currently fixed to the initial value; if needed, it will be open on the GUI for users later.
0x1c	Destination Operations CAR	RO	The type of operation supported by the destination, currently fixed to the initial value; if needed, it will be open on the GUI for users later.
0x20~0x3c	Reserved	—	—
0x40~0xfc CSRs			
0x40~0x48	Reserved	—	—
0x4c	Processing Element Logical Layer Control CSR	RO	The supported address bit width
0x50~0x54	Reserved	—	—
0x58	Local Configuration Space Base Address 0 CSR	RO	Address space configuration
0x5c	Local Configuration Space Base Address 1 CSR	RW	Address space configuration
0x60	Base Device ID CSR	RW	Used for setting device ID, and you can configure it on the GUI.
0x64	Reserved	—	—
0x68	Host Base Device ID Lock CSR	RW	Used for initialization
0x6c	Component Tag CSR	RW	The component tag value

Address (Byte)	Name	Type	Description
0x70~0xfc	Reserved	—	—
0x0100~0xffff Extension Address			
0x100	LP-Serial Register Block Header	RO	Address space configuration
0x104~0x11c	Reserved	—	—
0x120	Port Link Timeout Control CSR	RW	Port linking timeout register
0x124	Port Response Timeout Control CSR	RW	Port response timeout register
0x128~0x138	Reserved	—	—
0x13c	Port General Control CSR	RW	You can configure it on the GUI.
0x140	Port n Link Maintenance Request CSR	RO	rsv
0x144	Port n Link Maintenance Response CSR	RO	rsv
0x148	Port n Local ackID CSR	RO	rsv
0x14c~0x1508	Reserved	—	—
0x154	Port n Control 2 CSR	RO	Port control
0x158	Port n Error and Status CSR	RO	Port error and status
0x15c	Port n Control CSR	RW	Port control status
0x160~0x3fc	Reserved	—	—
0x400	LP-Serial Lane Command and Status Registers	RO	Extension space indication
0x410/0x430/0x450/0x470	Lane n Status 0 CSRs	—	Lane status
0x414/0x434/0x454/0x474	Lane n Status 1 CSRs	RO	rsv
0x010000~0x1ffff Custom Address			
0x10000	Watermarks CSR	RW	rsv
0x10004	Buffer Control CSR	RO	Buffer control register
0x10100	Maintenance Request Information Register	RW	Maintenance request information register
0x10104	Maintenance Request HopCount Register	RW	Maintenance request hopCount register
0x10108	Maintenance Response Time-out Scale Register	RW	Maintenance response time-out scale register

Note!

Register read/write definition:

- RC indicates read-clear

- RO indicates read-only
- RW indicates read-write

3.6.1 Device Identity CAR (0x0)

Table 3-4 The Meanings of Each Bit in Device Identity CAR

Name	Bit(s)	Type	Description	Default
DeviceIdentity	31:16	RO	Set through the option "Device Identity for Endpoint" on the GUI, assigned and managed by the device vendor.	0x0
DeviceVendorIdentity	15:0	RO	Set through the option "Device Vendor Identity" on the GUI, assigned to the device vendor by the RapidIO Trade Federation.	0x0

3.6.2 Device Information CAR (0x4)

Table 3-5 The Meanings of Each Bit in Device Information CAR

Name	Bit(s)	Type	Description	Default
rsv	31:12	RO	N/A	0x0
Major version	11:8	RO	Major Version	0x0
Minor Revision	7:4	RO	Minor Version	0x0
Patch	3:0	RO	Bug fix identifier	0x0

3.6.3 Assembly Identity CAR (0x8)

Table 3-6 The Meanings of Each Bit in Assembly Identity CAR

Name	Bit(s)	Type	Description	Default
AssylIdentity	31:16	RO	Set through the option "Assembly Identifier" on the GUI, assigned to the device vendor by the RapidIO Trade Federation.	0x0
AssyVendorIdentity	15:0	RO	Set through the option "Assembly Vendor Identifier" on the GUI, assigned and managed by the device vendor.	0x0

3.6.4 Assembly Information CAR (0xc)

Table 3-7 The Meanings of Each Bit in Assembly Information CAR

Name	Bit(s)	Type	Description	Default
AssyRev	31:16	RO	Set through the option "Assembly Revision Level" on the GUI, assigned and managed by the device vendor.	0x0
ExtendedFeaturesPtr	15:0	RO	The start address of the extended function	0x100

3.6.5 Processing Element Features CAR (0x10)

Table 3-8 The Meanings of Each Bit in Processing Element Features CAR

Name	Bit(s)	Type	Description	Default
Bridge	31	RO	Set through the option "Processing Element Features" on the GUI, the current endpoint is used as a Bridge.	0x0
Memory	30	RO	Set through the option "Processing Element Features" on the GUI, the current endpoint is used as a Memory.	0x0
Processor	29	RO	Set through the option "Processing Element Features" on the GUI, the current endpoint is used as a Processor.	0x0
rsv	28	RO	N/A	0x0
rsv	27	RO	N/A	0x0
rsv	26:7	RO	N/A	0x0
rsv	6	RO	N/A	0x0
rsv	5	RO	N/A	0x0
common_trans_large_support	4	RO	Can be set on the GUI If the option "Device ID Width" is set to 8 bits, the value is 1'b0. If the option "Device ID Width" is set to 16 bits, the value is 1'b1.	0x0
Extended_features	3	RO	The extend function supported with a fixed value of 1'b1.	0x1
Extended_addressing_support	2:0	RO	Only 34-bit address mode supported	0x1

3.6.6 Switch Port Information CAR (0x14)

Table 3-9 The Meanings of Each Bit in Switch Port Information CAR

Name	Bit(s)	Type	Description	Default
rsv	31:0	RO	N/A	0x0

3.6.7 Source Operations CAR (0x18)

Table 3-10 The Meanings of Each Bit in Source Operations CAR

Name	Bit(s)	Type	Description	Default
rsv	31:16	RO	N/A	0x0
Source_Read	15	RO	Set high, and it will be open to users on the GUI later.	0x1
Source_Write	14	RO	Set high, and it will be open to users on the GUI later.	0x1
Source_Streaming_write	13	RO	Set high, and it will be open to users on the GUI later.	0x1
Source_Write_with_response	12	RO	Set high, and it will be open to users on the GUI later.	0x1

Name	Bit(s)	Type	Description	Default
Source_Message	11	RO	Set high, and it will be open to users on the GUI later.	0x1
Source_Doorbell	10	RO	Set high, and it will be open to users on the GUI later.	0x1
Source_Atomic_compare_and_swap	9	RO	Set high, and it will be open to users on the GUI later.	0x1
Source_Atomic_test_and_swap	8	RO	Set high, and it will be open to users on the GUI later.	0x1
Source_Atomic_increment	7	RO	Set high, and it will be open to users on the GUI later.	0x1
Source_Atomic_decrement	6	RO	Set high, and it will be open to users on the GUI later.	0x1
Source_Atomic_set	5	RO	Set high, and it will be open to users on the GUI later.	0x1
Source_Atomic_clear	4	RO	Set high, and it will be open to users on the GUI later.	0x1
Source_Atomic_swap	3	RO	Set high, and it will be open to users on the GUI later.	0x1
rsv	2:0	RO	N/A	–

3.6.8 Destination Operations CAR (0x1c)

Table 3-11 The Meanings of Each Bit in Destination Operations CAR

Name	Bit(s)	Type	Description	Default
rsv	31:16	RO	N/A	0x0
Destination_Read	15	RO	Set high, and it will be open to users on the GUI later.	0x1
Destination_Write	14	RO	Set high, and it will be open to users on the GUI later.	0x1
Destination_Streaming_write	13	RO	Set high, and it will be open to users on the GUI later.	0x1
Destination_Write_with_response	12	RO	Set high, and it will be open to users on the GUI later.	0x1
Destination_Message	11	RO	Set high, and it will be open to users on the GUI later.	0x1
Destination_Doorbell	10	RO	Set high, and it will be open to users on the GUI later.	0x1
Destination_Atomic_compare_and_swap	9	RO	Set high, and it will be open to users on the GUI later.	0x1
Destination_Atomic_test_and_swap	8	RO	Set high, and it will be open to users on the GUI later.	0x1
Destination_Atomic_increment	7	RO	Set high, and it will be open to users on the GUI later.	0x1
Destination_Atomic_decrement	6	RO	Set high, and it will be open to users on the GUI later.	0x1
Destination_Atomic_set	5	RO	Set high, and it will be open to users on the GUI later.	0x1
Destination_Atomic_clear	4	RO	Set high, and it will be open to users on the GUI later.	0x1

Name	Bit(s)	Type	Description	Default
ear			users on the GUI later.	
Destination_Atomic_swap	3	RO	Set high, and it will be open to users on the GUI later.	0x1
rsv	2:0	RO	N/A	–

3.6.9 Processing Element Logical Layer Control CSR (0x4c)

Table 3-12 The Meanings of Each Bit in Processing Element Logical Layer Control CSR

Name	Bit(s)	Type	Description	Default
rsv	31:3	RO	N/A	0x0
Extended_addressing_control	2:0	RO	34-Bit address supported	0x1

3.6.10 Local Configuration Space Base Address 0 CSR (0x58)

Table 3-13 The Meanings of Each Bit in Local Configuration Space Base Address 0 CSR

Name	Bit(s)	Type	Description	Default
rsv	31:3	RO	N/A	0x0

3.6.11 Local Configuration Space Base Address 1 CSR (0x5c)

Table 3-14 The Meanings of Each Bit in Local Configuration Space Base Address 1 CSR

Name	Bit(s)	Type	Description	Default
rsv	31	RO	N/A	0x0
LCSBA_ADDR1	30:21	RW	0x3ff by default	0x3ff
rsv	20:0	RO	N/A	0x0

3.6.12 Base Device ID CSR (0x60)

Table 3-15 The Meanings of Each Bit in Base Device ID CSR

Name	Bit(s)	Type	Description	Default
rsv	31:24	RO	N/A	0x0
Base_deviceID	23:16	RW	Set through the option "Local Device ID" on the GUI, valid when Device ID Width is 8 bits.	0xff
Large_base_deviceID	15:0	RW	Set through the option "Local Device ID" on the GUI, valid when Device ID Width is 16 bits.	0x00ff

3.6.13 Host Base Device ID Lock CSR (0x68)

Table 3-16 The Meanings of Each Bit in Host Base Device ID Lock CSR

Name	Bit(s)	Type	Description	Default
rsv	31:16	RO	N/A	0x0
Host_base_deviceID	15:0	RW	Used for initialization	0xffff

3.6.14 Component Tag CSR (0x6c)

Table 3-17 The Meanings of Each Bit in Component Tag CSR

Name	Bit(s)	Type	Description	Default
component_tag	31:0	RW	The component tag value	0x0

3.6.15 LP-Serial Register Block Header (0x100)

Table 3-18 The Meanings of Each Bit in LP-Serial Register Block

Name	Bit(s)	Type	Description	Default
Extended_Features_Pointer	31:0	RO	The start address of the next extended space	0x400
Extended_Features_ID	15:0	RO	Hard-wired extended features ID.	0x1

3.6.16 Port Link Timeout Control CSR (0x120)

Table 3-19 The Meanings of Each Bit in Port Link Timeout Control CSR

Name	Bit(s)	Type	Description	Default
Port_Link_Timeout_Value	31:8	RW	Port linking timeout Set through the option "Port Link Time-out Control" on the GUI	0xffff
Rsv	7:0	RO	N/A	0x0

3.6.17 Port Response Timeout Control CSR (0x124)

Table 3-20 The Meanings of Each Bit in Port Response Timeout Control CSR

Name	Bit(s)	Type	Description	Default
Port_Response_Timeout_Value	31:8	RW	Port response timeout Set through the option "Port Response Time-out Control" on the GUI	0xffff
Rsv	7:0	RO	N/A	0x0

3.6.18 Port General Control CSR (0x13c)

Table 3-21 The Meanings of Each Bit in Port General Control CSR

Name	Bit(s)	Type	Description	Default
Host	31	RW	Set through the option "Port General Control" on the GUI	0xffff
Master_Enable	30	RW	Set through the option "Port General Control" on the GUI	–
Discovered	29	RW	Set through the option "Port General Control" on the GUI	–
rsv	28:0	RO	N/A	0x0

3.6.19 Port n Link Maintenance Request CSR (0x140)

Table 3-22 The Meanings of Each Bit in Port n Link Maintenance Request CSR

Name	Bit(s)	Type	Description	Default
rsv	31:0	RO	N/A	0x0

3.6.20 Port n Link Maintenance Response CSR (0x144)

Table 3-23 The Meanings of Each Bit in Port n Link Maintenance Response CSR

Name	Bit(s)	Type	Description	Default
rsv	31:0	RO	N/A	0x0

3.6.21 Port n Local ackID CSR (0x148)

Table 3-24 The Meanings of Each Bit in Port n Local ackID CSR

Name	Bit(s)	Type	Description	Default
rsv	31:0	RO	N/A	0x0

3.6.22 Port n Control 2 CSR (0x154)

Table 3-25 The Meanings of Each Bit in Port n Control 2 CSR

Name	Bit(s)	Type	Description	Default
rsv	31:16	RO	N/A	0x0
Gbaud_Support_and_Enable	15:6	RO	You can select the rate on the GUI: ● 1.25Gbps – 10'b0001010111 ● 2.5Gbps – 10'b0001011101 ● 3.125Gbps – 10'b0001110101 ● 5Gbps – 10'b0011010101	N/A
rsv	5:4	RO	N/A	0x0
Select_Baudrate	3:0	RO	You can select the rate on the GUI: ● 4'b0000 - no rate selected ● 4'b0001 - 1.25 Gbps ● 4'b0010 - 2.5 Gbps ● 4'b0011 - 3.125 Gbps ● 4'b0100 - 5.0 Gbps ● 4'b0101 - 6.25 Gbps ● 4'b0110 – 4'b1111 - Reserved	–

3.6.23 Port n Error and Status CSR (0x158)

Table 3-26 The Meanings of Each Bit in Port n Error and Status CSR

Name	Bit(s)	Type	Description	Default
rsv	31:21	RO	N/A	0x0
Output_Retry_encountered	20	RC	Output Retry-Stopped encountered , active high	0x0
output_port_retry_2d	19	RO	Indicates that Output Retry-Stopped is the last response packet , active high	0x0
output_port_retry_sto	18	RO	In Output Retry-Stopped	0x0

Name	Bit(s)	Type	Description	Default
pped_2d			status , active high	
Output_Error_encountered	17	RC	output error encountered , active high	0x0
output_port_error_2d	16	RO	In output error status , active high	0x0
rsv	15:11	RO	N/A	0x0
Input_Retry_Stopped_2d	10	RO	In Input Retry-Stopped status , active high	0x0
Input_Error_encountered	9	RC	Input Error-Stopped encountered , active high	0x0
Input_Error_Stopped_2d	8	RO	In Input Error-Stopped status , active high	0x0
rsv	7:3	RO	N/A	0x0
Port_Error_encountered	2	RC	Port error encountered , active high	0x0
Port_OK_2d	1	RO	The linking completed , active high	0x0
Port_un_initialized_2d	0	RO	The linking not completed , active high	0x0

3.6.24 Port n Control CSR (0x15c)

Table 3-27 The Meanings of Each Bit in Port n Control CSR

Name	Bit(s)	Type	Description	Default
Port_Width	31:30	RO	Port Width ● 2'b00 – 1x ● 2'b01 – 4x ● 2'b10 – 2x ● 2'b11 – rsv	0x0
Initialized_Port_Width	29:27	RO	Initialized port width ● 3'b000 – 1x, lane0 ● 3'b001 – 4x, lane R ● 3'b010 – 4x ● 3'b011 – 2x ● 3'b100 – 3'b111 – rsv	0x0
rsv	26:24	RO	N/A	0x0
Port_Disable	23	RW	Port disabled	0x0
Output_Port_Enable	22	RW	Output port enabled	0x1
Input_Port_Enable	21	RW	Input port enabled	0x1
Error_Checking_Disable	20	RW	Error checking disabled	0x0
Multi_cast_Event_Participant	19	RO	Can receive multi-cast packets	0x1
rsv	18:1	RO	N/A	0x0
Port_Type	0	RO	Fixed to Serial Port	0x1

3.6.25 LP-Serial Lane Command and Status Registers (0x400)

Table 3-28 The Meanings of Each Bit in LP-Serial Lane Command and Status Registers

Name	Bit(s)	Type	Description	Default
Next_Extended_Features_Pointer	31:16	RO	The start address of next extended function	0x900
Next_Extended_Features_ID	15:0	RO	The ID of next extended function	0xd

3.6.26 Lane n Status 0 CSRs (0x410/0x430/0x450/0x470)

Table 3-29 The Meanings of Each Bit in Lane n Status 0 CSRs

Name	Bit(s)	Type	Description	Default
Lane#_Port_Number	31:24	RO	Lane port No.	0x0
Lane#_Lane_Number	23:20	RO	Lane No.	0x0
rsv	19:15	RO	N/A	0x0
Lane#_Receiver_Trained	14	RO	Indicates that the RX lane has completed equalizer adaption (rcvr_trained) , active high	0x0
Lane#_Receiver_Lane_Sync	13	RO	Indicates that the RX lane has completed synchronization , active high	0x0
Lane#_Receiver_Lane_Ready	12	RO	Indicates that the RX lane is ready to receive data , active high	0x0
Lane#_decoding_8b10b_errors_async_cfg_2d	11:8	RC	Indicates the decoding error statistics for RX lane	0x0
Lane#_sync_State_Change	7	RC	Indicates that RX lane lane_sync state has changed	0x0
Lane#_rcvr_trained_State_Changed	6	RC	Indicates that RX lane rcvr_trained state has changed	-
Rsv	5:0	RO	N/A	0x0

3.6.27 Lane n Status 1 CSRs (0x414/0x434/0x454/0x474)

Table 3-30 The Meanings of Each Bit in Lane n Status 1 CSRs

Name	Bit(s)	Type	Description	Default
rsv	31:0	RO	N/A	0x0

3.6.28 Watermarks CSR (0x10000)

Table 3-31 The Meanings of Each Bit in Watermarks CSR

Name	Bit(s)	Type	Description	Default
rsv	31:0	RO	N/A	0x0

3.6.29 Buffer Control CSR (0x10004)

Table 3-32 The Meanings of Each Bit in Buffer Control CSR

Name	Bit(s)	Type	Description	Default
rx_flow_control_only	31	RO	RX flow control supported	0x1
rsv	30	RO	N/A	0x0
tx_flow_control	29	RO	Not supported for the time being	0x0
tx_request_reorder	28	RO	Not supported for the time being	0x0
rsv	27	RO	N/A	0x0
tx_buffer_size	26:16	RO	Set through the option "TX Buffer Depth" on the GUI	0x10
force_rx_flow_control	15	RO	Not supported for the time being	0x0
rsv	14:8	RO	N/A	0x0
rx_buffer_size	7:0	RO	Set through the option "RX Buffer Depth" on the GUI	0x10

3.6.30 Maintenance Request Information Register (0x10100)

Table 3-33 The Meanings of Each Bit in Maintenance Request Information Register

Name	Bit(s)	Type	Description	Default
o_maint_req_tid	31:24	RW	Transmit the srcTID field in the Maintenance transaction packet	0x0
rsv	23:19	RO	N/A	0x0
o_maint_req_prio	18:17	RW	Transmit the prio field in the Maintenance transaction packet	0x1
o_maint_req_crf	16	RW	Transmit the crf field in the Maintenance transaction packet	0x0
o_maint_req_destid	15:0	RW	Transmit the Destination ID in the Maintenance transaction packet	0x0

3.6.31 Maintenance Request HopCount Register (0x10104)

Table 3-34 The Meanings of Each Bit in Maintenance Request HopCount Register

Name	Bit(s)	Type	Description	Default
rsv	31:8	RO	N/A	0x0
o_maint_hop_count	7:0	RW	Transmit the hop count field in the Maintenance transaction packet	0x0

3.6.32 Maintenance Response Time-out Scale Register (0x10108)

Table 3-35 The Meanings of Each Bit in Maintenance Response Time-out Scale Register

Name	Bit(s)	Type	Description	Default
rsv	31:8	RO	N/A	0x0
maint_resp_timeout_scale	7:0	RW	Transmit the timeout scale of maintenance transaction packet, used in conjunction with register 0x124. 0x124 register corresponds to a timeout value of M, and 0x10108 register corresponds to a scale of N. The number of clocks that are determined to have timed out in the cfg_clk_i clock domain is $M \times N$. For example, if the configuration clock domain is 10M, the corresponding value of 0x124 register is 0xfffff, and 0x10108 value is 0x2, then the corresponding response timeout is $16777216 \times 2 \times 100\text{ns} = 3355443200\text{ns} \approx 3.35\text{second}$.	0x2

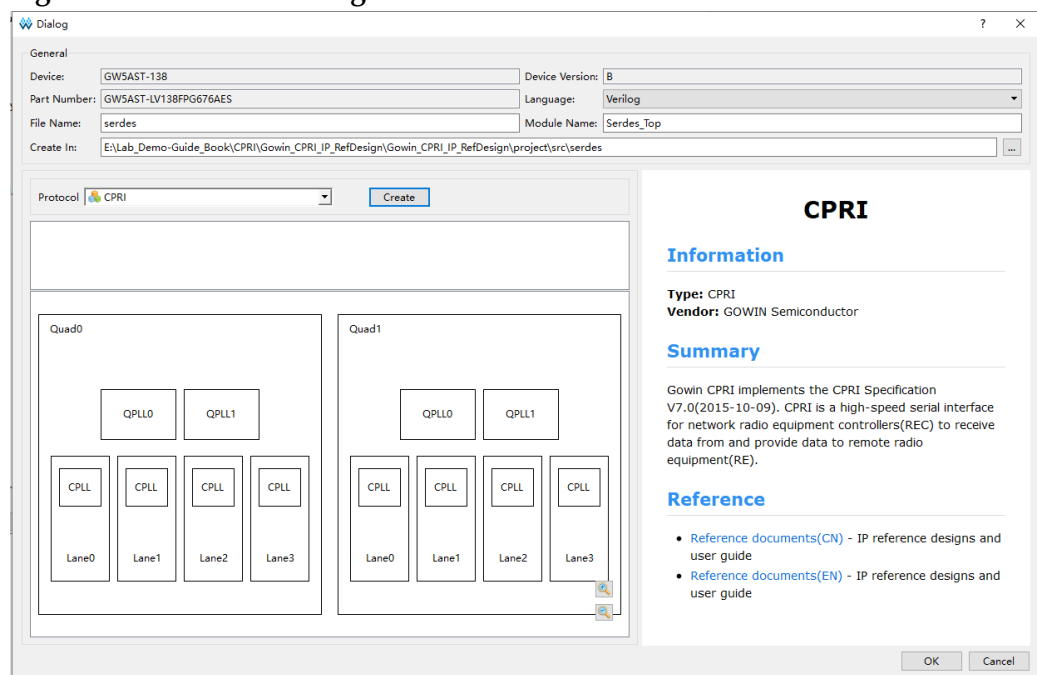
4 Interface Configuration

You can call and configure Gowin Serial RapidIO IP using the IP core generator tool in the IDE.

1. Open SerDes IP

After creating the project, click the "Tools" tab in the upper left interface, click "IP Core Generator" from the drop-down list to open Gowin IP Core Generator. Then find SerDes under the Soft IP Core directory, and double-click it to open SerDes IP.

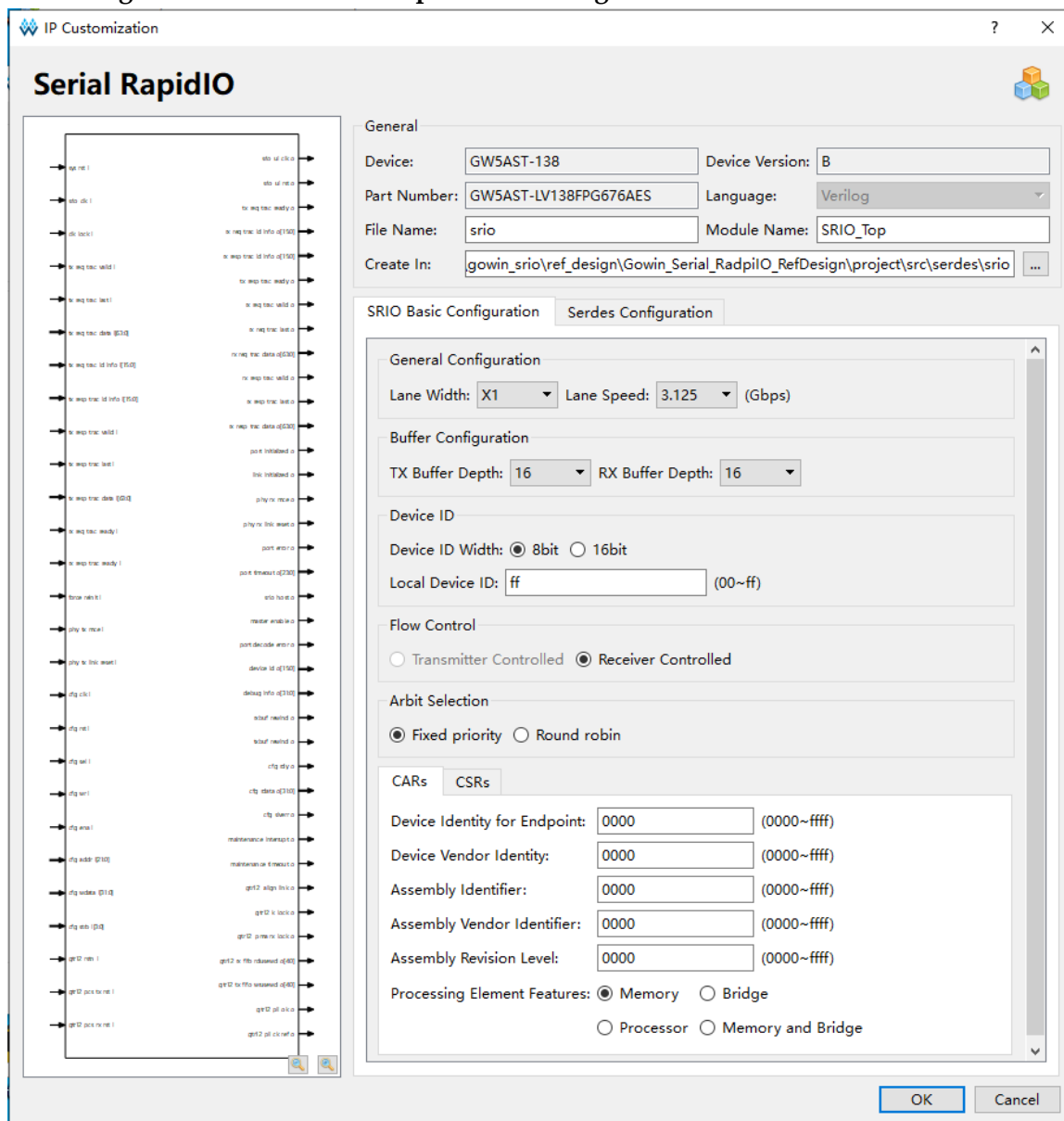
Figure 4-1 SerDes IP Configuration Interface



2. Open Serial RapidIO IP

After opening SerDes IP, find Serial RapidIO in the "Protocol" drop-down list and click "Create" to open Serial RapidIO IP protocol configuration interface.

Figure 4-2 Gowin Serial RapidIO IP Configuration Interface



3. Configure Serial RapidIO IP Protocol

The Serial RapidIO IP configuration interface includes "SRIO Basic Configuration", "SerDes Configuration", "AFE", and "Optional Ports Configuration" options, as shown in Figure 4-3, Figure 4-4, Figure 4-5, Figure 4-6, and Figure 4-7. The descriptions of parameters are shown in Table 4-1. When you have selected the Serial RapidIO IP parameters, click the "OK" button to generate the configuration associated with Serial RapidIO IP protocol.

4. Complete SerDes IP configuration

On the SerDes IP interface, the user completes the configuration of all protocols and then clicks the "OK" button to generate the SerDes IP. In the SerDes IP top-level file, the signal with srio_ prefix is the signal associated with Serial RapidIO IP.

Figure 4-3 IP Protocol GUI 1

The screenshot displays the 'Serdes Configuration' tab of the 'SRIO Basic Configuration' window. The interface is organized into several sections:

- General Configuration:** Includes 'Lane Width' set to 'X1' and 'Lane Speed' set to '3.125' Gbps.
- Buffer Configuration:** Includes 'TX Buffer Depth' and 'RX Buffer Depth', both set to '16'.
- Device ID:** Includes 'Device ID Width' with radio buttons for '8bit' (selected) and '16bit', and a 'Local Device ID' text field containing 'ff' with a range of '(00~ff)'.
- Flow Control:** Includes radio buttons for 'Transmitter Controlled' and 'Receiver Controlled' (selected).
- Arbit Selection:** Includes radio buttons for 'Fixed priority' (selected) and 'Round robin'.
- CARs / CSRs:** A sub-tabbed section containing:
 - Five text fields for 'Device Identity for Endpoint', 'Device Vendor Identity', 'Assembly Identifier', 'Assembly Vendor Identifier', and 'Assembly Revision Level', all containing '0000' and having a range of '(0000~ffff)'.
 - 'Processing Element Features' with radio buttons for 'Memory' (selected), 'Bridge', 'Processor', and 'Memory and Bridge'.

Figure 4-4 IP Protocol GUI 2

SRIO Basic Configuration
Serdes Configuration

General Configuration

Lane Width: X1 Lane Speed: 3.125 (Gbps)

Buffer Configuration

TX Buffer Depth: 16 RX Buffer Depth: 16

Device ID

Device ID Width: ☒ 8bit ☐ 16bit

Local Device ID: ff (00~ff)

Flow Control

☐ Transmitter Controlled ☒ Receiver Controlled

Arbit Selection

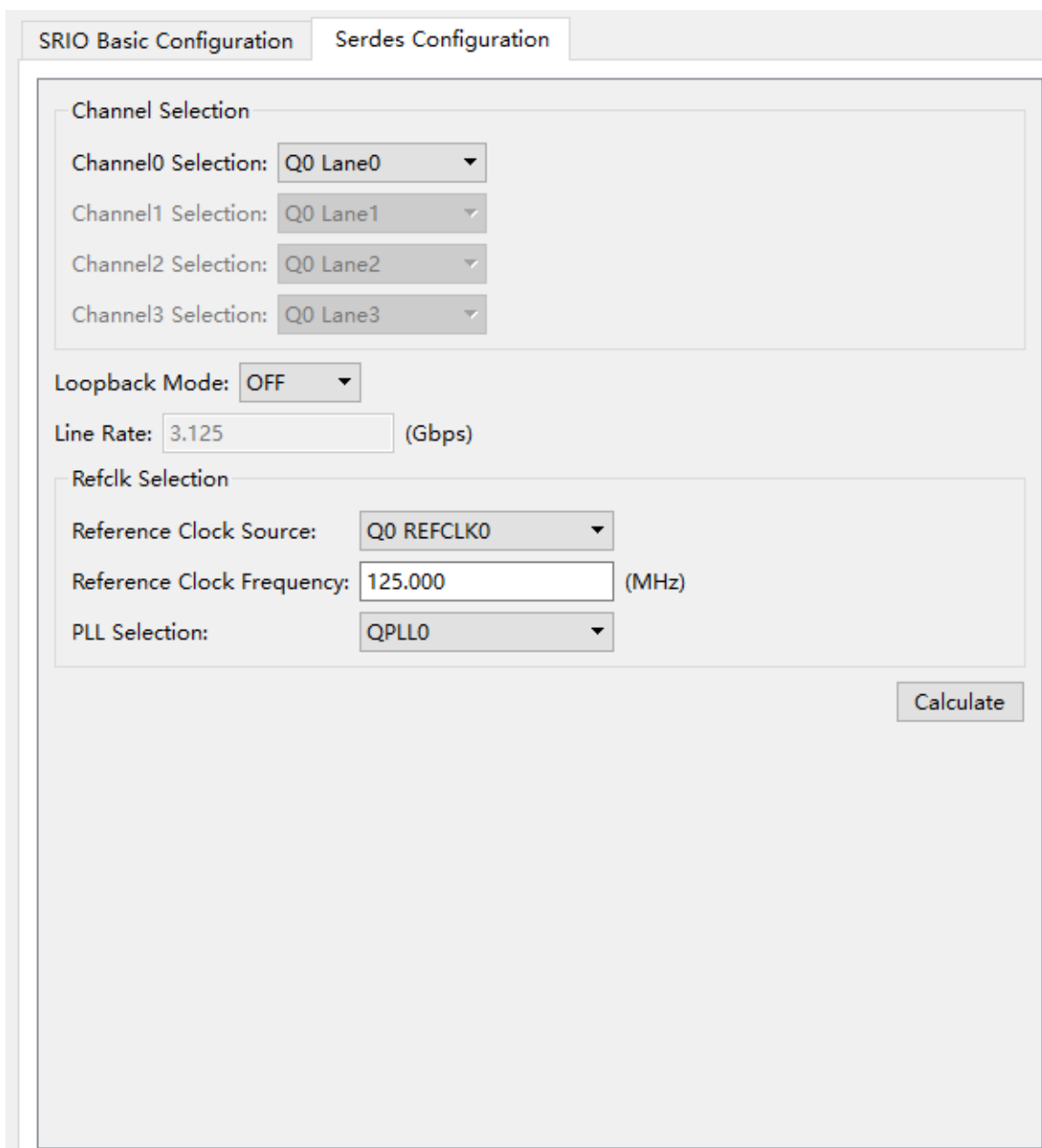
☒ Fixed priority ☐ Round robin

CARs CSRs

Port General Control: ☒ Host ☒ Master Enable
☐ Discovered

Port Link Time-out Control: ffffff (0000~ffffff)

Port Response Time-out Control: ffffff (0000~ffffff)

Figure 4-5 SerDes Configuration Option

The image shows a software configuration window titled "SerDes Configuration Option". It has two tabs: "SRIO Basic Configuration" and "Serdes Configuration", with the latter being the active tab. The configuration is organized into three main sections: "Channel Selection", "Loopback Mode", and "Refclk Selection".

Channel Selection: This section contains four dropdown menus for selecting lanes. All four are currently set to "Q0 Lane0":

- Channel0 Selection: Q0 Lane0
- Channel1 Selection: Q0 Lane1
- Channel2 Selection: Q0 Lane2
- Channel3 Selection: Q0 Lane3

Loopback Mode: A dropdown menu set to "OFF".

Line Rate: A text input field containing "3.125" followed by the unit "(Gbps)".

Refclk Selection: This section contains three configuration options:

- Reference Clock Source: Q0 REFCLK0
- Reference Clock Frequency: 125.000 (MHz)
- PLL Selection: QPLL0

A "Calculate" button is located in the bottom right corner of the configuration area.

Figure 4-6 AFE Configuration Option

The screenshot shows the 'AFE' configuration tab within a larger interface. The 'AFE' tab is highlighted, and the 'Optional Ports Configuration' tab is also visible. The configuration is divided into two main sections: TX and RX.

TX Configuration:

- Differential Swing: 900mV (dropdown)
- FFE Mode:
 - FFE Mode: Auto (dropdown)
 - Cm: 0 (0~19)
 - C0: 40 (21~40)
 - C1: 0 (0~19)

RX Configuration:

- SD Threshold: 100mV (dropdown)
- Equalization:
 - Equalization Mode: Auto (dropdown)
 - ATT: 7 (0~10)
 - BOOST: 9 (0~15)
 - BIAS: 7 (0~15)

Figure 4-7 Optional Ports Configuration Option

The screenshot shows the 'Optional Ports Configuration' tab within the same interface. The 'Optional Ports Configuration' tab is highlighted, and the 'AFE' tab is also visible. The configuration is divided into two main sections: RX Clock Correction and DRP Ports.

RX Clock Correction:

- ☐ RX Clock Correction

DRP Ports:

- ☐ DRP Ports

Table 4-1 Serial RapidIO IP Parameter Configuration

Name	Range	Default	Description
SRIO Basic Configuration			
Lane Width	x1, x2, x4	x1	Select IP lanes
Lane Speed	1.25Gbps, 2.5Gbps, 3.125Gbps, 5Gbps	3.125Gbps	Select lane rate Note! 5Gbps x2/x4 mode is not supported currently; 2.5Gbps/3.125Gbps x4 is not supported currently.
TX Buffer Depth	8, 16, 32	16	Set TX buffer depth
RX Buffer Depth	8, 16, 32	16	Set RX buffer depth
Device ID Width	8 bits, 16 bits	8 bits	Select the width of device ID
Local Device ID	0x00~0xff or 0x0000~0xffff	ff	Set the value of device ID
Flow Control	Transmitter Controlled、Receiver Controlled	Receiver Controlled	Select flow control mode, only Receiver Controlled supported now.
Arbit Selection	Fixed priority、Round robin	Fixed priority	TX arbitration priority selection
Device Identity for Endpoint	0x0000~0xffff	0000	Assigned in accordance with RapidIO, corresponding to register 0x0
Device Vendor Identity	0x0000~0xffff	0000	Assigned in accordance with RapidIO, corresponding to register 0x0
Assembly Identity	0x0000~0xffff	0000	Assigned in accordance with RapidIO, corresponding to register 0x8
Assembly Vendor Identifier	0x0000~0xffff	0000	Assigned in accordance with RapidIO, corresponding to register 0x8
Assembly Revision Level	0x0000~0xffff	0000	Assigned in accordance with RapidIO, corresponding to register 0xC
Processing Element Features	Memory、Bridge、Processor、Memory and Bridge	Memory	Assigned in accordance with RapidIO, corresponding to register 0x10
Host	Check/Uncheck	Check	Assigned in accordance with RapidIO, corresponding to register 0x10
Master Enable	Check/Uncheck	Check	Assigned in accordance with RapidIO, corresponding to register 0x10
Port Link Time-out Control	0x0000~0xffff	ffff	Set port timeout value Assigned in accordance with RapidIO, corresponding to register 0x120
Port Response Time-out Control	0x0000~0xffff	ffff	Set port response timeout value Assigned in accordance with RapidIO, corresponding to register 0x124
PHY Configuration			
Channel0 Selection	Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2, Q1 Lane3,	Q0 Lane0	SerDes lane selection Q0 and Q1 correspond to two Quads of SerDes Lane0, Lane1, Lane2, and Lane3 indicate the 4 Lane numbers for each Quad of SerDes.

Name	Range	Default	Description
			Note! The number of lanes available on the GUI is associated with the option "Lane Width"; Lanes selected for the same IP need to be in the same Quad.
Channel1 Selection	Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2, Q1 Lane3,	Q0 Lane1	SerDes lane selection Q0 and Q1 correspond to two Quads of SerDes Lane0, Lane1, Lane2, and Lane3 indicate the 4 Lane numbers for each Quad of SerDes.
Channel2 Selection	Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2, Q1 Lane3,	Q0 Lane2	SerDes lane selection Q0 and Q1 correspond to two Quads of SerDes Lane0, Lane1, Lane2, and Lane3 indicate the 4 Lane numbers for each Quad of SerDes.
Channel3 Selection	Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2, Q1 Lane3,	Q0 Lane3	SerDes lane selection Q0 and Q1 correspond to two Quads of SerDes Lane0, Lane1, Lane2, and Lane3 indicate the 4 Lane numbers for each Quad of SerDes.
Loopback Mode	OFF, LB_NES, LB_FES, LB_ENC	OFF	SerDes Loopback Selection: ● OFF indicates Normal mode; SerDes data is transmitted and received normally. ● LB_NES, SerDes internal loopback; data is looped back to RX from TX of SerDes. ● LB_ENC, SerDes internal loopback; data is looped back to RX from TX of SerDes. ● LB_FES, SerDes external loopback; data is looped back to TX from RX of SerDes.
Reference Clock Source	● For devices GW5AST-138/GW5AT-138/GW5AT-75 Q0 REFCLK0, Q0 REFCLK1, Q1 REFCLK 0, Q1 REFCLK 1 ● For devices GW5AT-60 Q0 REFCLK0, Q0 REFCLK1, Q0 REFCLK2, Q0 REFCLK3, SERDES Q0CLKIN0, SERDES Q0CLKIN1, SERDES	Q0 REFCLK0	● For devices GW5AST-138/GW5AT-138/GW5AT-75: The reference clock selection for high-speed transceivers is as follows: Q0/Q1 corresponds to the two Quads of SerDes. REFCLK0 and REFCLK1 correspond to the two input reference clocks for each SerDes Quad. Users can select the input reference clock according to their application needs. ● For devices GW5AT-60: The reference clock selection for high-speed transceivers is as follows: Q0REFCLK0, Q0REFCLK1, Q0REFCLK2, and Q0REFCLK3 correspond to the four input reference clocks for Quad0. SERDES Q0CLKIN0, SERDES Q0CLKIN1, SERDES Q0CLKIN2, and SERDES Q0CLKIN3 correspond to the input

Name	Range	Default	Description
	Q0CLKIN2, SERDES Q0CLKIN3		reference clocks for dedicated GPIO pins. The selectable input reference clocks vary depending on the chip package.
Reference Clock Frequency	User input	125M	The input reference clock for high-speed transceivers. After inputting the reference clock, you can click the "Calculate" button to confirm if the frequency is correct.
PLL Selection	QPLL0, QPLL1, CPLL	QPLL0	PLL selection
AFE			
Differential Swing	100mV~900mV	900mV	Configure TX differential signal swing Vdiffpp, Vdiffpp=2xVdiff
FFE Mode	Auto, Manual	Auto	Configure TX FFE mode ● Auto: Auto mode ● Manual: Manual mode
Cm	0~19	0	Transmit FFE pre-cursor
C0	21~40	40	Transmit FFE main-cursor
C1	0~19	0	Transmit FFE post-cursor
SD Threshold	25mV~200mV	100mV	Receive differential signal SD threshold
Equalization Mode	Auto, Manual	Auto	Configure RX equalization mode ● Auto: Auto mode ● Manual: Manual mode
ATT	0~10	7	Adjust RX intermediate-frequency attenuation, with smaller values indicating greater attenuation.
BOOST	0~15	9	Adjust RX high-frequency amplification, with larger values indicating larger gain.
BIAS	0~15	7	Configure SerDes amplification parameters for the RX signal. The higher the configuration, the stronger the amplification of the signal.
Optional Ports Configuration			
RX Clock Correction	Checked/Unchecked	Unchecked	Lookback Port Selection: ● If checked, the IP supports CTC. ● If unchecked, the IP does not support CTC.
DRP Ports	Checked/Unchecked	Unchecked	DRP Port Selection: ● If checked, the IP outputs DRP port. The port supports access to SerDes internal registers. ● If unchecked, the IP does not output this port.

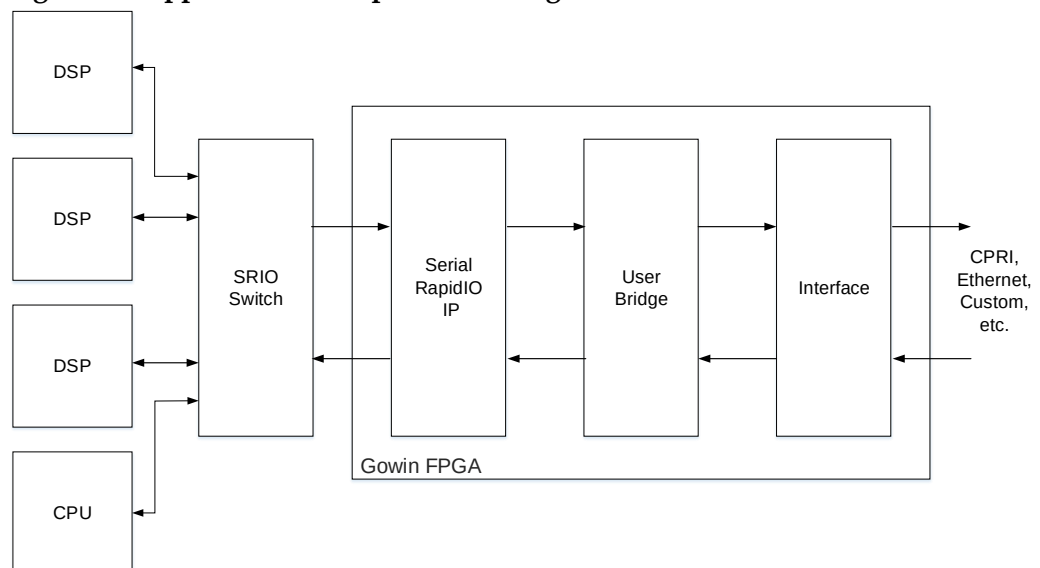
5 Reference Design

For more details, see the [Serial RapidIO reference design](#) at Gowin official website.

5.1 Typical Applications

The RapidIO protocol is a high-performance, low pin-count, packet-switched interconnect architecture. It is an open interconnect technology standard designed to meet the requirements of high-performance embedded systems. An example application is shown in Figure 5-1, where Serial RapidIO IP communicates with other Serial RapidIO Endpoint devices through the switch board.

Figure 5-1 Application Example Block Diagram



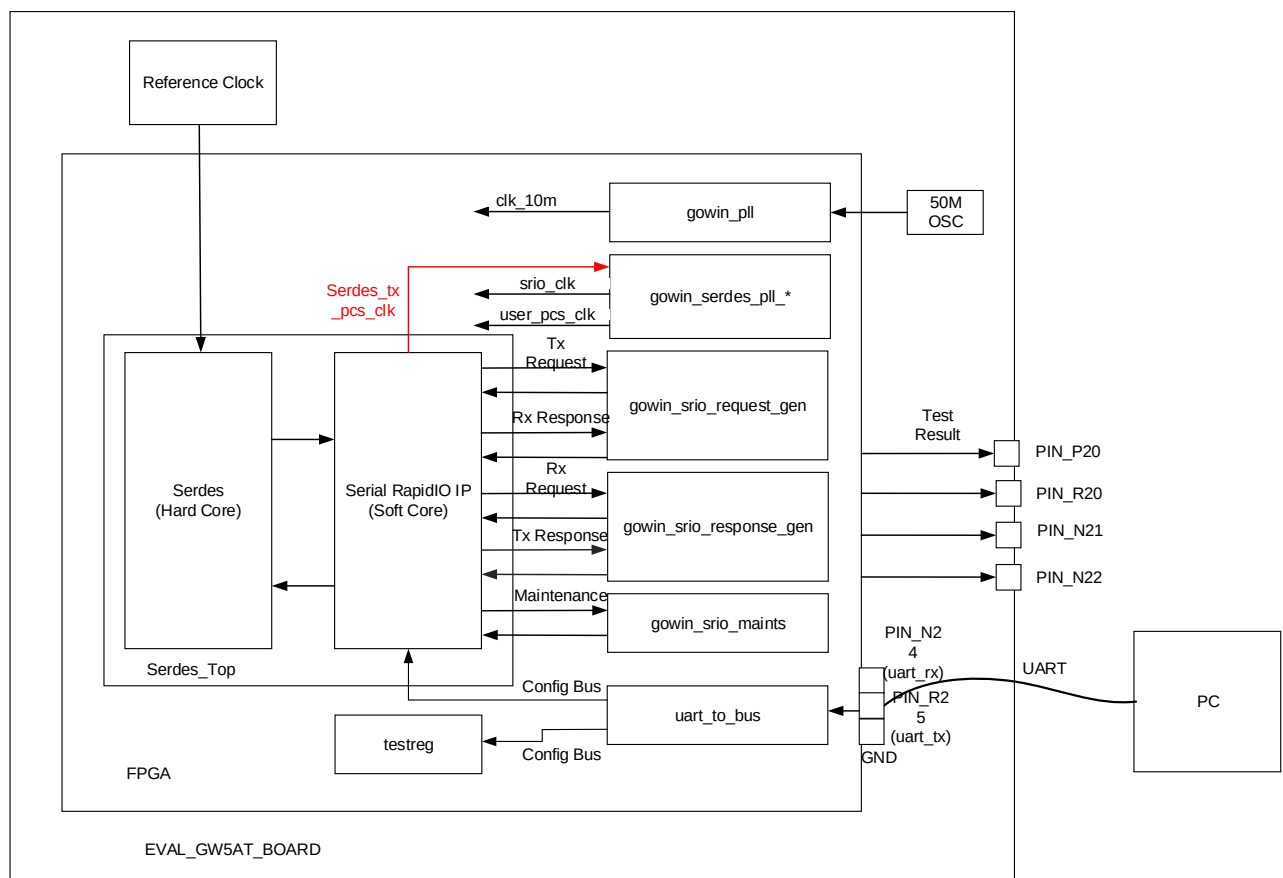
5.2 Serial RapidIO IP Reference Design Project

Gowin Serial RapidIO IP reference design includes SerDes IP module (Serial RapidIO IP soft core included), clock and reset, functional test module and debug module.

- `uart_to_bus`: Converts UART serial port to internal configuration bus interface in FPGA, easy to read/write registers, and easy to debug single board.

- **testreg**: Maintains a set of internal registers, users can access to obtain link status.
- **gowin_pll**: The on-board internal 50MHz crystal oscillator locks out the operating clock for the configuration module.
- **gowin_serdes_pll_1p25g**: Uses the pcs clock output from SerDes to the Fabric as the PLL reference clock to lock out the IP operating clock when the IP Lane Speed is configured as 1.25Gbps. For the line rate and clock frequency correspondence, you can see the description of **srio_clk_i** in Table 3-1.
- **gowin_serdes_pll_2p5g**: Uses the pcs clock output from SerDes to the Fabric as the PLL reference clock to lock out the IP operating clock when the IP Lane Speed is configured as 2.5Gbps. For the line rate and clock frequency correspondence, you can see the description of **srio_clk_i** in Table 3-1.
- **gowin_serdes_pll_3p125g**: Uses the pcs clock output from SerDes to the Fabric as the PLL reference clock to lock out the IP operating clock when the IP Lane Speed is configured as 3.125Gbps. For the line rate and clock frequency correspondence, you can see the description of **srio_clk_i** in Table 3-1.
- **gowin_serdes_pll_5g**: Uses the pcs clock output from SerDes to the Fabric as the PLL reference clock to lock out the IP operating clock when the IP Lane Speed is configured as 5Gbps. For the line rate and clock frequency correspondence, you can see the description of **srio_clk_i** in Table 3-1.
- **gowin_srio_request_gen**: The local device transmits a request transaction to the remote device, and checks the response transaction returned by the remote device, then finally outputs the test completion indication and the receive error indication.
- **gowin_srio_response_gen**: The local device receives the request transaction transmitted by the remote device, and transmits the generated response transaction based on transaction type to the remote device.
- **gowin_srio_maints**: Generates the maintenance transaction, and reads local device registers and remote device registers.
- **Serdes_Top**: Contains SerDes hard core and Serial RapidIO IP soft core; Gowin EDA tool will automatically complete the connection between SerDes hard core and Serial RapidIO IP; user only needs to pay attention to the interface of SerDes top layer after package.

Figure 5-2 Reference Design Instance Basic Structure Diagram



5.3 Reference Design Board Test 1

Gowin currently offers a reference design for SerDes internal loopback testing of single Serial RapidIO IP, allowing users to quickly become familiar with the interface, timing, and function of Gowin Serial RapidIO IP without relying on a daughter card.

The steps for reference project board test are as follows:

- Download the project from the website and compile to generate bit file.
- The build environment is shown in Figure 5-3.
- Download fs to single board
- Press the SW1 (PIN_L25) button to start the test
- To confirm the test results, there are two methods:

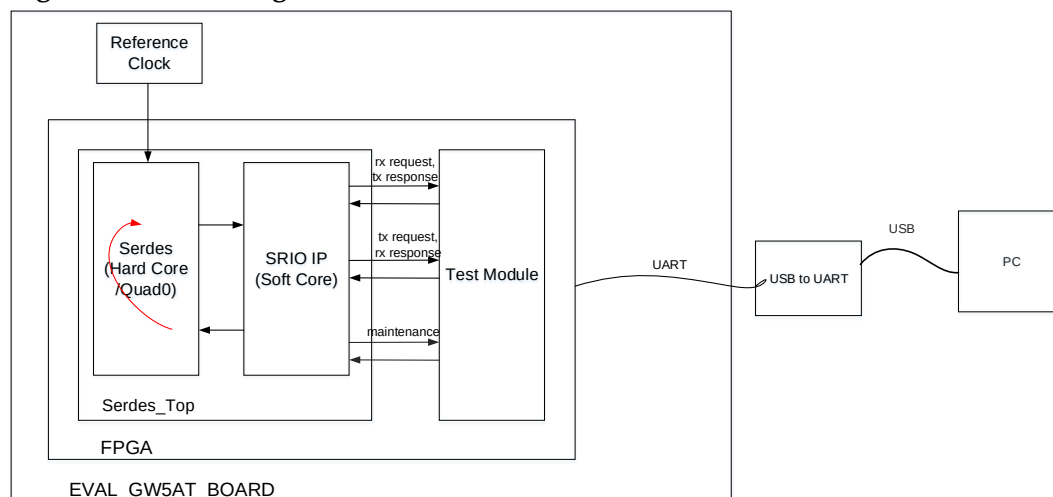
Method 1: Observe the LEDs

- LED0 (PIN_P20): On indicates that the board 50M crystal oscillator is as reference PLL lock, and that Serdes output reference clock is as reference PLL lock
- LED1(PIN_R20): On indicates the completion of port_initialized and link_initialized inside SRIO IP

- LED2 (PIN_N21): On indicates completion of transmitting all request transaction packets.
- LED3 (PIN_N22): On indicates that all received acknowledge transaction packets are correct.

Method 2: Read the register through the serial tool

Figure 5-3 Block Diagram of Test Environment 1



The PC can access the testreg module registers and Serial RapidIO IP registers of the reference design and the registers of the remote device through the serial tool. testreg has an address space of 0x000000~0x3ffffc (byte address); Serial RapidIO IP local device has an address space of 0x400000~0x5ffffc (byte address), and Serial RapidIO IP remote device has an address space of 0x600000~0x7fffffc (byte address).

When the environment is built, input "R 0" in the serial port tool and the register value is displayed as shown in Figure 5-4. If you input "W 0 value", the register value corresponding to value will be written to the register, and if you readback "R 0", the register will become the re-written value.

Note!

The register address operated by the serial port tool is the word address, and the word address multiplied by 4 equals the byte address in the register list. For example, R2, indicating the read address 0x2, corresponds to the address 0x8 bytes in the register list.

Table 5-1 testreg Register Description

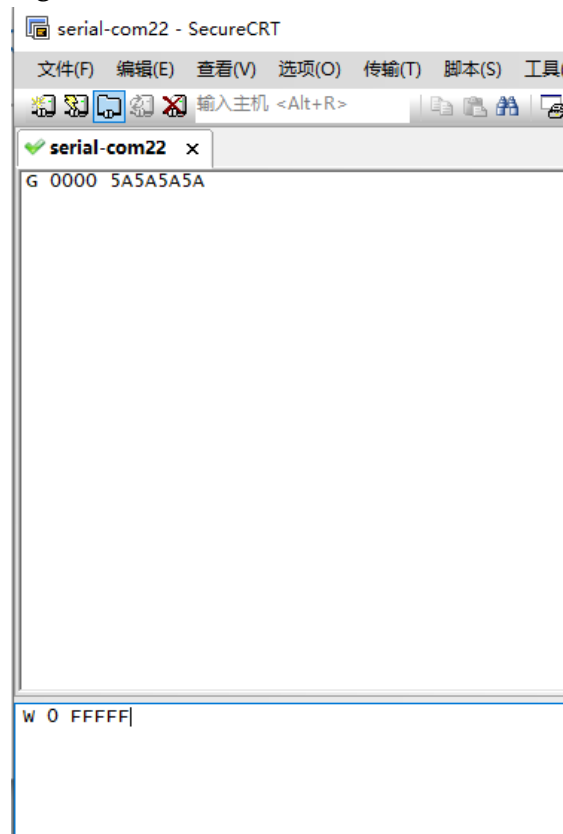
Address (Byte)	Type	Data Width	Signal Name	Description
0x0	RW	[31:0]	test_reg	Test registers that can be written and read back, confirming the register read and write function.
0x4	RO	[31:2]	Rsv.	N/A
	RW	[1:0]	loop_en	rsv
0x8	RO	[31:20]	Rsv.	N/A
	RO	[19:16]	lane_k_lock	Lane K character lock indication
	RO	[15:12]	lane_align_link	Lane alignment indication
	RO	[11:8]	pma_rx_lock	PMA PLL lock indication

Address (Byte)	Type	Data Width	Signal Name	Description
	RO	[7:4]	cmu_ok	SerDes PLL lock indication
	RO	[3:2]	Rsv.	N/A
	RO	[1]	Pll1_lock	Gowin_Serdes_pll* lock indication
	RO	[0]	pll0_lock	Gowin_pll lock indication
0xc	RO	[31:2]	Rsv.	N/A
	RO	[1]	link_initialized	IP link initialization completed indication
	RO	[0]	port_initialized	IP port initialization completed indication
0x10	RO	[31:1]	Rsv.	N/A
	RW	[0]	test_start_o	Start the test with the rising edge active
0x14	RO	[31:3]	Rsv.	N/A
	RW	[2]	ln_pcs_rx_rst_o	Serdes TX PCS reset
	RW	[1]	ln_pcs_tx_rst_o	SerDes RX PCS reset
	RW	[0]	ln_rst_o	Serdes PMA reset
0x18	RO	[31:4]	Rsv.	N/A
	RO	[3:2]	request_check_error	The response transaction check is correct
	RO	[1:0]	request_done	TX request transaction completed indication
0x30	RO	[31:3]	Rsv.	N/A
	RW	[2]	force_reinit_o	Triggers IP re-initialization
	RW	[1]	phy_tx_link_reset_o	Triggers IP to transmit link-reset control character
	RW	[0]	phy_tx_mce_o	Triggers the IP to transmit MCE control character
0x34	RO	[31:16]	Rsv.	N/A
	RO	[15:0]	srio_device_id_2d	The current local device ID value
0x40	RO	[31:2]	Rsv.	N/A
	RO	[1]	test_ok_2d	Test succeed indication, active-high.
	RO	[0]	test_done_2d	Test completed indication, active-high.
0x41	RO	[31:16]	error_cnt_2d	Test error counter
	RO	[15:0]	done_cnt_2d	Test done counter

Note!

Register read/write definition:

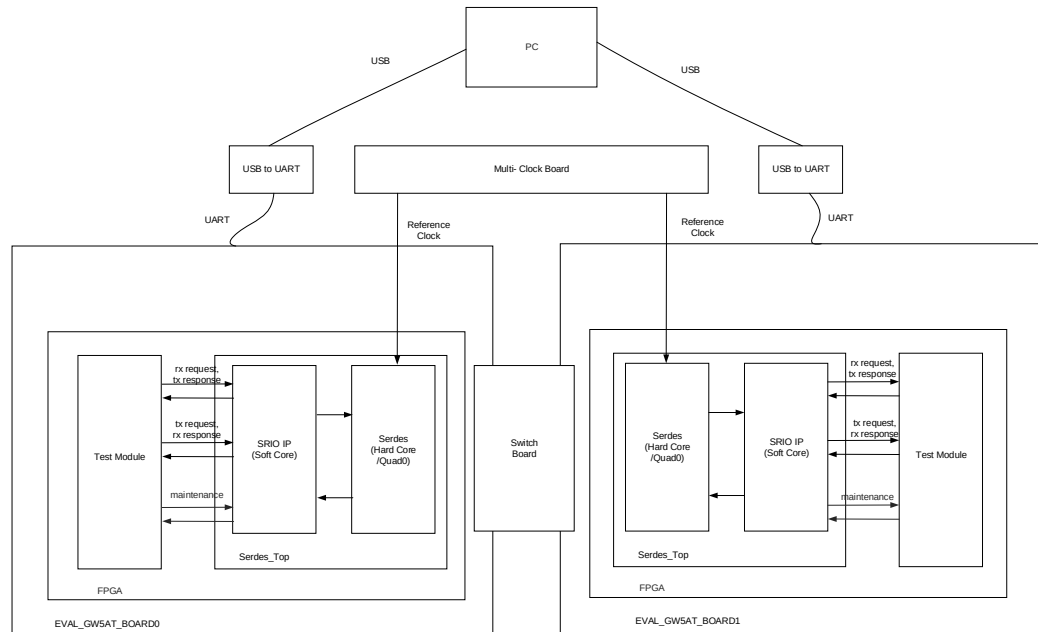
- RO indicates read-only
- RW indicates read-write

Figure 5-4 Serial Port Tool

5.4 Reference Design Board Test 2

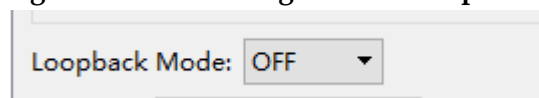
Serial RapidIO IP supports point-to-point connection, and what is described in [5.3 Reference Design Board Test 1](#) is SerDes internal loopback test. Users can also modify the reference project to build the environment for single board-to-board test. The test method is the same as described in [5.3 Reference Design Board Test 1](#), the difference only lies in the environment setup and IP loopback settings. Compared to SerDes internal loopback test, users need to connect the two development boards, and add Gowin multi-clock daughter card and development board connection daughter card.

Figure 5-5 Block Diagram of Test Environment 2



Since the user is testing the connection of two development boards, it is necessary to modify the loopback setting on the GUI of the reference design, and set the option "Loopback Mode" to OFF.

Figure 5-6 GUI Setting for Serial RapidIO IP Board Test 2



6 File Delivery

The delivery file for Gowin Serial RapidIO IP includes documentation, design source code, and reference design.

6.1 Documentation

The folder mainly contains the user guide and release note in PDF version.

Table 6-1 Documents List

Name	Description
IPUG1023, Gowin Serial RapidIO IP User Guide	Gowin Serial RapidIO IP User Guide, namely this one
RN1023, Gowin Serial RapidIO IP Release Note	Gowin IP Release Note

6.2 Design Source Code (Encryption)

The encrypted code file contains the Gowin Serial RapidIO IP RTL encrypted code which is used for GUI in order to cooperate with Gowin Software to generate the IP core required by users.

Table 6-2 Design Source Code List of Gowin Serial RapidIO IP

Name	Description
srio_core_encryption.v	The top-level file of the IP core, which provides users with interface information, encrypted.

6.3 Reference Design

The Ref. Design folder contains the netlist file of Gowin Serial RapidIO IP, user reference design, constraints file, top-level file and the project file, etc.

Table 6-3 File List

Name	Description
srio_board.v	The top module of reference design
srio_ed_prj.cst	Project physical constraints file
srio_ed_prj.sdc	Project timing constraints file

Name	Description
srio_ed_prj.rao	Project capture file
test	Test stimulus folder, including the test stimulus modules gowin_srio_maints.v, gowin_srio_request_gen.v, gowin_srio_response_gen.v and gowin_sdpram.v
SerDes	The SerDes IP folder, including the SerDes-related files generated by EDA tools and srio protocol folder
debug	Debugging-related folders, including the register testing module testreg.v, and the interface configuration arbitration module cfg_2to1.v
uart_to_bus	Generated uart to bus IP file for converting a serial port to an internally configured bus
gowin_pll	PLL module folder includes five IPs: ● gowin_pll: Uses the external input 50MHz clock as a reference clock to lock out the internal configuration clock. ● gowin_serdes_pll_1p25g: Uses the pcs clock output from the SerDes as the reference clock for the PLL to lock out the internal IP operating clock for lane line rates 1.25G. ● gowin_serdes_pll_2p5g: Uses the pcs clock output from the SerDes as the reference clock for the PLL to lock out the internal IP operating clock for lane line rates 2.5G. ● gowin_serdes_pll_3p125g: Uses the pcs clock output from the SerDes as the reference clock for the PLL to lock out the internal IP operating clock for the lane line rate 3.125G. ● gowin_serdes_pll_5g: Uses the pcs clock output from the SerDes as the reference clock for the PLL to lock out the internal IP operating clock for the lane line rate 5G.
fifo_sc_top	The generated FIFO IP file for the test module

