



Gowin JESD204B IP

Release Note

RN1019-1.1E, 06/30/2023

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Revision History

Date	Version	Description
05/25/2023	1.0E	Initial version published.
06/30/2023	1.1E	Up to eight lanes per core supported.

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1 About This Release

This release includes Gowin JESD204B IP user guide and reference design.

Gowin JESD204B IP reference design is available at Gowin Website. The reference design can be used for simulation and overall synthesis, placement & routing after the instantiation with user design.

2 Function and Enhancement Summary

The function and enhancement items are as follows:

Function	Description
Front-end synthesis tool: GowinSynthesis	
Supports JESD204B	● Supports up to eight lanes per core ● Supports initial lane alignment ● Supports scrambling and descrambling ● Supports 1-256 octets per frame ● Supports 1-32 frames per multiframe ● Supports subclass 1 ● The configuration interface supports real-time modification of parameters ● The IP core can be configured to TX, RX, and TX & RX modes
Back-end placement and routing tool: Gowin Software (V1.9.9.Beta-2 and above)	
Enhancements	—

3 Documentation

The released IP manuals are listed in the table below. You can download the PDF manuals at Gowin website or read online.

Documents	Description
IPUG1019, Gowin JESD204B IP User Guide	Online, PDF
RN1019, Gowin JESD204B IP Release Note	Online, PDF

4 IP Support

Since the requirements of user design and the maximum frequency are different, the reference design does not include FPGA specific location (.cst) and timing constraints (.sdc) documents, and you can determine the location and timing constraints on your own.

For the customized IP design and support, please contact Gowin sales and support line.

Official Website: www.gowinsemi.com

Email: support@gowinsemi.com

