



Gowin JESD204B IP

User Guide

IPUG1019-1.2.1E, 10/25/2024

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Revision History

Date	Version	Description
05/25/2023	1.0E	Initial version published.
06/30/2023	1.1E	Up to eight lanes per core supported.
04/19/2024	1.2E	● "Fix Concig Enable" option added in "JESD204B Core Configuration" tab. ● "PCS WIDTH" option added in "PHY Configuration" tab. ● "AFE" tab added. ● "Optional Ports Configuration" tab added.
10/25/2024	1.2.1E	GW5AT-60 devices supported.

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1 About This Guide

1.1 Purpose

The purpose of Gowin JESD204B IP User Guide is to help you learn the features and usage of Gowin JESD204B IP by providing the descriptions of functions, GUI, and reference design, etc. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.9.02 (64-bit). As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find related documents at www.gowinsemi.com.cn/en/

- [SUG100, Gowin Software User Guide](#)
- [IPUG1022, Gowin UART to Bus IP User Guide](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1104, GW5AST series of FPGA Products Data Sheet](#)

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
APB	Advanced Peripheral Bus
CGS	Code Group Sync
DDS	Direct Digital Frequency Synthesizer
DRP	Dynamic Reconfiguration Port
FPGA	Field Programmable Gate Array
ILAS	Initial channel alignment sequence
IP	Intellectual Property
LMFC	Local Multi-Frame Clock

Terminology and Abbreviations	Meaning
SerDes	Serializer/Deserializer

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Function Introduction

2.1 Overview

JESD204B is a high-speed serial interface used to connect Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs) to logic devices. The IP implements the data link layer functions in the JESD204B protocol, including Code Group Sync (CGS), Initial Lane Alignment Sequence (ILAS), user data output, etc. This IP currently only supports subclass 1.

Table 2-1 Gowin JESD204B IP Overview

Gowin JESD204B IP	
Logic Resource	Please refer to Table 2-2
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9.Beta-2 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features

- Supports up to eight lanes per core (No greater than the number of SerDes lanes of the selected device)
- Supports initial lane alignment
- Supports scrambling and descrambling
- Supports 1-256 octets per frame
- Supports 1-32 frames per multiframe
- Supports subclass 1
- The configuration interface supports real-time parameter modification
- The IP core can be configured to TX, RX, and TX & RX modes

2.3 Resource Utilization

JESD204B IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Take GW5AT-138 series and 32-bit PCS as an instance, and the resource utilization is as shown in Table 2-2.

Table 2-2 Resource Utilization of Gowin JESD204B IP

Number of lanes	Type	Resource Utilization				
		Register	LUT	ALU	BSRAM	SSRAM
1	TX & RX	2358	2633	636	1	19
2	TX & RX	4066	4634	1032	2	38
4	TX & RX	7482	8479	1826	4	76
8	TX & RX	12816	13612	3402	8	153
1	TX	822	1141	274	0	19
2	TX	1224	1800	432	0	38
4	TX	2028	3150	750	0	76
8	TX	3915	5769	1374	0	153
1	RX	1537	1506	362	1	0
2	RX	2843	2854	600	2	0
4	RX	5455	5512	1076	4	0
8	RX	8901	7668	2028	8	0

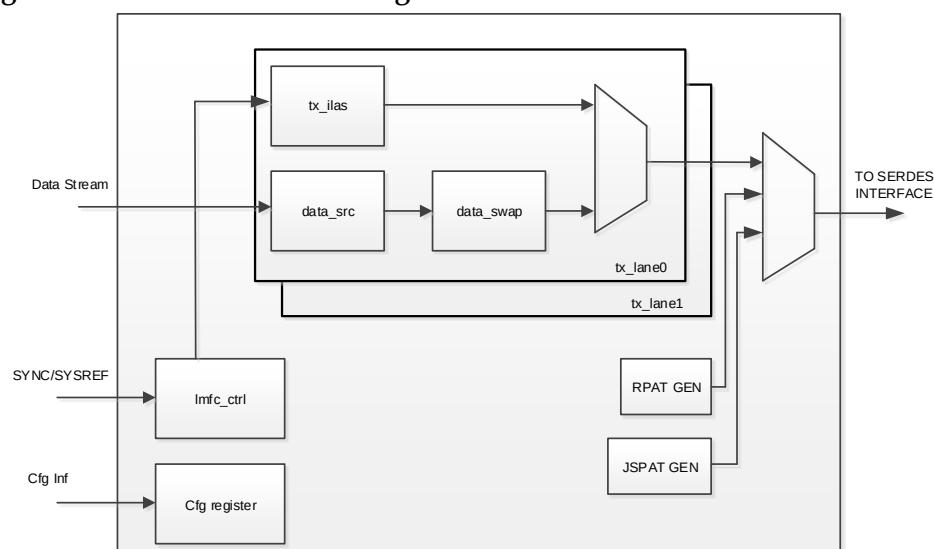
3 Functional Description

3.1 System Block Diagram

3.1.1 Transmitter

The transmitter of JESD204B is as shown in Figure 3-1 .

Figure 3-1 Transmitter Block Diagram



The number of lanes supported by JESD204B TX Core can be configured, and the module tx_lane will be automatically instantiated internally for each additional lane.

The tx_lane module includes:

- tx_ilas module: Used to generate the initial lane alignment sequence
- data_scr module: Used for data scrambling
- data_swap module: Used to replace octets at the end of frame or multiframe according to certain rules

Other modules:

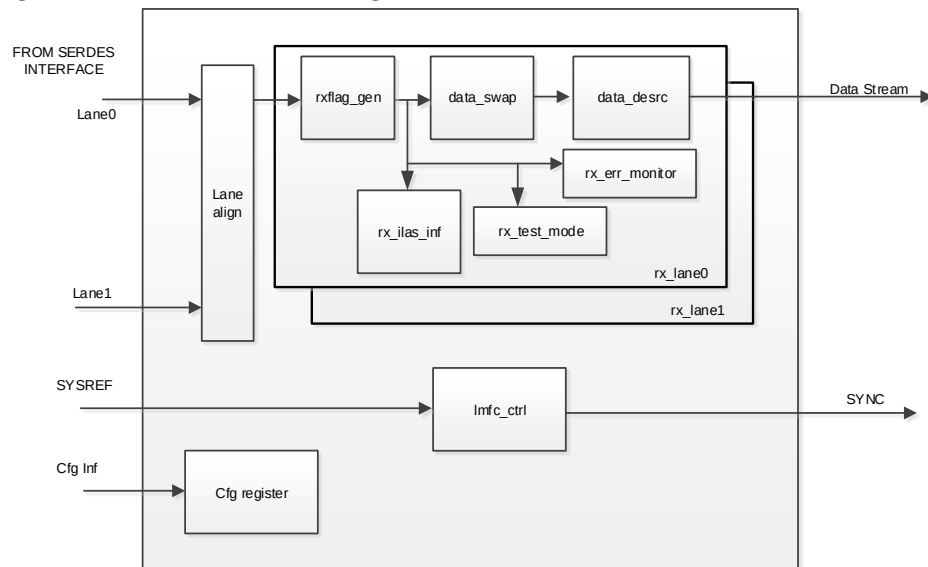
- RPAT module: RPAT generator

- JSPAT Module: JSPAT generator
- tx_lmfc_ctrl module: Used to generate a local multiframe clock for subclass 1
- Cfg_register module: Used to configure and monitor internal registers

3.1.2 Receiver

The receiver of JESD204B is as shown in Figure 3-2 .

Figure 3-2 Receiver Block Diagram



The number of lanes supported by JESD204B RX Core can be configured, and the module rx_lane will be automatically instantiated internally for each additional lane.

The rx_lane module includes:

- rxflag_en module: Used to generate the flags for start of frame, end of frame, end of multiframe, and special characters
- rx_ilas_inf module: Used to capture ILAS
- data_swap module: Used to replace octets at the end of frame or multiframe according to certain rules
- data_desc module: Used for data descrambling
- rx_test_mode module: Error counters for SerDes RX data in test mode
- rx_err_monitor module: Error counters for SerDes data, ILAS, and data fields in normal mode

Other modules:

- Lane_align module: Data buffer for all lanes; when all lanes have received ILAS, the buffer is released at the same time.
- tx_lmfc_ctrl module: Used to generate a local multiframe clock for subclass 1

- Cfg_register module: Used to configure and monitor internal registers

3.2 Port List

Gowin JESD204B IP TX core and RX core interfaces are independent of each other and described separately below.

3.2.1 TX Core Interface

The IO ports of Gowin JESD204B IP TX core are shown in Figure 3-3.

Figure 3-3 Gowin JESD204B IP TX Port Diagram

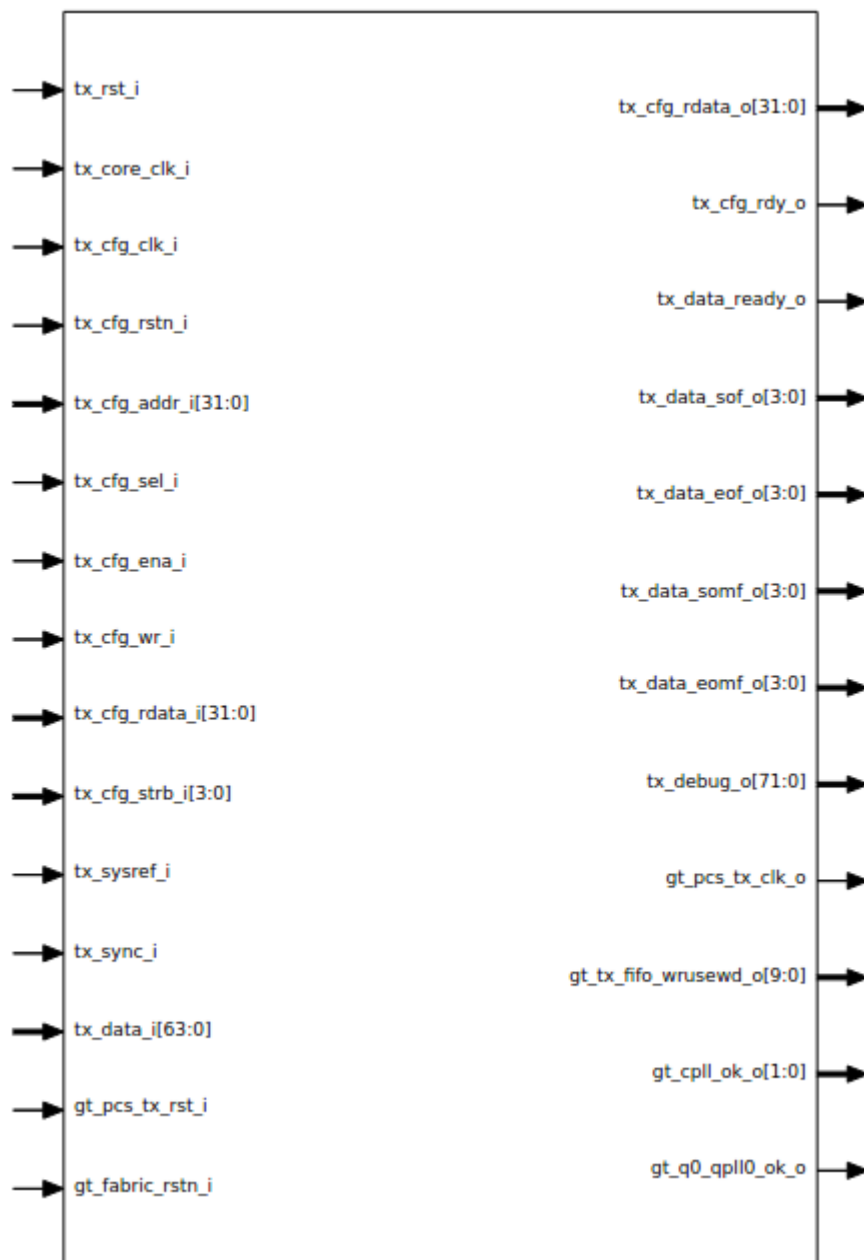


Table 3-1 I/O List of TX Core

Signal Name	I/O	Description
tx_rst_i	IN	TX core reset 1: Reset 0: Operating
tx_core_clk_i	IN	TX core clock, frequency = line rate/ $Y^{[2]}/40$.
tx_cfg_clk_i	IN	Bus configuration clock, free-running clock.
tx_cfg_rstn_i	IN	Bus configuration reset
tx_cfg_addr_i	IN	Bus configuration address
tx_cfg_sel_i	IN	Bus configuration selection
tx_cfg_ena_i	IN	Bus configuration enable
tx_cfg_wr_i	IN	Bus I/O signal 1: Write 0: Read
tx_cfg_rdata_o[31:0]	OUT	Read data
tx_cfg_wdata_i[31:0]	IN	Write data
tx_cfg_rdy_o	OUT	Ready signal
tx_cfg_strb_i[3:0]	IN	Write strobe signal, fixed to 4'hf
tx_sysref_i	IN	SYSREF input, this signal is required when configured as subclass 1.
tx_sync_n_i	IN	JESD204B defines a synchronous signal as a low-level active synchronous request signal, so the signal remains low until the comma alignment is complete and high when ILA and normal data are requested.
tx_data_ready_o	OUT	TX core ready to receive TX data
tx_data_sof_o[4* $Y^{[2]}$ -1:0]	OUT	Start of frame boundary indication; this signal is $4 \times Y^{[2]}$ bits, and is used to indicate the frame first byte position in tx_data in the clock cycle. For example, $Y^{[2]} = 1$ - When tx_data_sof = 0001, the first byte of the frame is located in bits [7:0] of the tx_data word, and the next 3 bytes are located in bits [31:8]. - When tx_data_sof = 0010, the first byte is located in bits [15:8] of the tx_data word and the next 2 bytes are in bits [31:16]; bits [7:0] contain the end of the previous frame. - When tx_data_sof = 0100, the first byte is located in bits [23:16] of the tx_data word and the next byte is in bits [31:24]; bits [15:0] contain the end of the previous frame. - When tx_data_sof = 1000, tx_data contains the last 3 bytes of the previous frame in bits [23:0] and the first byte of the new frame is in bits [31:24].

Signal Name	I/O	Description
		Note! - Multiple bits of tx_data_sof can be asserted in the same cycle, depending on the bytes per frame (e.g., $F = 1$, tx_data_sof = 1111). - The rule is the same when $Y^{[2]} = 2$ as when $Y^{[2]} = 1$.
tx_data_eof_o[4*Y ^[2] -1:0]	OUT	End of frame boundary indication; this signal is 4*Y ^[2] bits, and is used to indicate the frame last byte position in tx_data in the clock cycle.
tx_data_somf_o[4*Y ^[2] -1:0]	OUT	Start of multiframe boundary indication; the position of the first byte of each multiframe is encoded in the same way as tx_data_sof.
tx_data_eomf_o[4*Y ^[2] -1:0]	OUT	End of multiframe boundary indication; the position of the last byte of each multiframe is encoded in the same way as tx_data_eof.
tx_data_i[32*Y ^[2] *N ^[1] -1:0]	IN	TX data; least significant byte is transmitted first. tx_tdata[32*Y ^[2] -1 : 0] data is transmitted through serial lane 0. tx_tdata[64*Y ^[2] -1 : 32*Y ^[2]] data is transmitted through serial lane 1. tx_tdata[((N + 1) * Y ^[2] * 32) - 1 : (N * Y ^[2] * 32)] data is transmitted through serial channel N.
tx_debug_o[36*Y ^[2] *N ^[1] -1:0]	OUT	Debugging Interface
SerDes-related interfaces		
gt_q0_qpll0_ok_o	OUT	Quad0 QPLL0 is locked; there is no this pin if Quad0 QPLL0 is not used.
gt_q0_qpll1_ok_o	OUT	Quad0 QPLL1 is locked; there is no this pin if Quad0 QPLL1 is not used.
gt_q1_qpll0_ok_o	OUT	Quad1 QPLL0 is locked; there is no this pin if Quad1 QPLL0 is not used.
gt_q1_qpll1_ok_o	OUT	Quad1 QPLL1 is locked; there is no this pin if Quad1 QPLL1 is not used.
gt_cppll_ok_o[N-1:0]	OUT	CPLL lock flag per lane
gt_fabric_rstn_i	IN	PMA reset of the lane connected to the core
gt_pcs_tx_clk_o	OUT	Lane PCS TX clock; if it is multilane, the first lane PCS TX clock is output by default.
gt_pcs_tx_rst_i	IN	TX PCS reset of the lane connected to the core
gt_tx_fifo_wrusewd_o[5*N ^[1] -1:0]	OUT	The used write data in lane TX FIFO

Note!

^[1] N in the table means the number of lanes.

^[2] Y in the table means: when PCS is set to 32 bits, Y = 1; when PCS is set to 64 bits, Y = 2.

3.2.2 RX Core Interface

The IO ports of Gowin JESD204B IP RX core are shown in Figure 3-4.

Figure 3-4 Gowin JESD204B IP RX Core Port Diagram

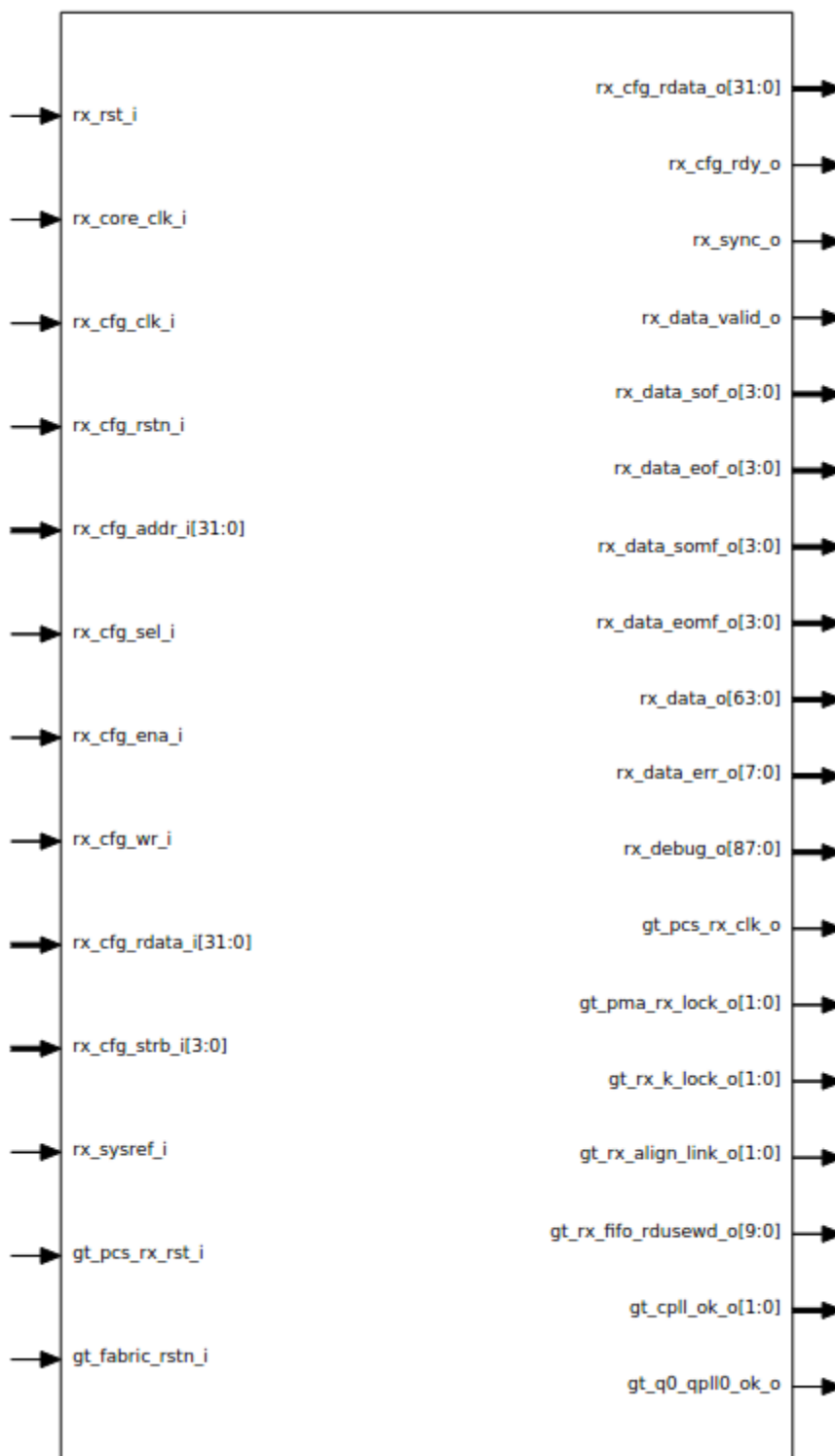


Table 3-2 I/O List of RX Core

Signal Name	I/O	Description
rx_rst_i	IN	RX core reset 1: Reset 0: Operating
rx_core_clk_i	IN	RX core clock, frequency = line rate/ $Y^{[2]}/40$.
rx_cfg_clk_i	IN	Bus configuration clock, free-running clock.
rx_cfg_rstn_i	IN	Bus configuration reset
rx_cfg_addr_i	IN	Bus configuration address
rx_cfg_sel_i	IN	Bus configuration selection
rx_cfg_ena_i	IN	Bus configuration enable
rx_cfg_wr_i	IN	Bus I/O signal 1: Write 0: Read
rx_cfg_rdata_o[31:0]	OUT	Bus read data
rx_cfg_wdata_i[31:0]	IN	Bus write data
rx_cfg_rdy_o	OUT	Bus ready signal
rx_cfg_strb_i[3:0]	IN	Bus strobe signal, fixed to 4'hf.
rx_sysref_i	IN	SYSREF input, this signal is required when configured as subclass 1.
rx_sync_o	OUT	JESD204B defines a synchronous signal as a low-level active synchronous request signal, so the signal remains low until the comma alignment is complete and high when ILA and normal data are requested.
rx_data_valid_o	OUT	RX data ready
rx_data_sof_o [4* $Y^{[2]}$ -1:0]	OUT	Start of frame boundary indication; this signal is 4*$Y^{[2]}$ bits, and is used to indicate the frame first byte position in rx_data in the clock cycle. For example: $Y^{[2]} = 1$ - When rx_data_sof = 0001, the first byte of the frame is located in bits [7:0] of the rx_data word, and the next 3 bytes are located in bits [31:8]. - When rx_data_sof = 0010, the first byte is located in bits [15:8] of the rx_data word and the next 2 bytes are in bits [31:16]; bits [7:0] contain the end of the previous frame. - When rx_data_sof = 0100, the first byte is located in bits [23:16] of the rx_data word and the next byte is in bits [31:24]; bits [15:0] contain the end of the previous

Signal Name	I/O	Description
		frame. - When rx_data_sof = 1000, rx_data contains the last 3 bytes of the previous frame in bits [23:0] and the first byte of the new frame is in bits [31:24]. Note! - Multiple bits of rx_data_sof can be asserted in the same cycle, depending on the bytes per frame (e.g., F = 1, rx_data_sof = 1111). - The rule is the same when $Y^{[2]} = 2$ as when $Y^{[2]} = 1$.
rx_data_eof_o [4* $Y^{[2]}$ -1:0]	OUT	End of frame boundary indication This signal is $4 \times Y^{[2]}$ bits, and is used to indicate the position of last frame byte in rx_data in the clock cycle.
rx_data_somf_o [4* $Y^{[2]}$ -1:0]	OUT	Start of multiframe boundary indication; the position of the first byte of each multiframe is encoded in the same way as rx_data_sof.
rx_data_eomf_o [4* $Y^{[2]}$ -1:0]	OUT	End of multiframe boundary indication; the position of the last byte of each multiframe is encoded in the same way as rx_data_eof.
rx_data_o [$N^{[1]} * Y^{[2]} * 32$ -1:0]	OUT	RX data; least significant byte is received first. The RX data for serial lane 0 is rx_data[32*$Y^{[2]}$-1: 0] The RX data for serial lane 1 is rx_data[64*$Y^{[2]}$-1: 32*$Y^{[2]}$] The RX data for serial lane N is tx_tdata[((N + 1) * $Y^{[2]}$ * 32) - 1:(N * $Y^{[2]}$ * 32))]
rx_data_err_o [$N^{[1]} * Y^{[2]} * 4$ -1:0]	OUT	Byte error; This signal indicates there is a single byte error in the data stream. The bit width corresponds to the bytes in rx_data_o.
rx_debug_o [44* $Y^{[2]} * N^{[1]}$ -1:0]	OUT	Debugging Interface
SerDes-related interfaces		
gt_q0_qpll0_ok_o	OUT	Quad0 QPLL0 is locked; there is no this pin if Quad0 QPLL0 is not used.
gt_q0_qpll1_ok_o	OUT	Quad0 QPLL1 is locked; there is no this pin if Quad0 QPLL1 is not used.
gt_q1_qpll0_ok_o	OUT	Quad1 QPLL0 is locked; there is no this pin if Quad1 QPLL0 is not used.
gt_q1_qpll1_ok_o	OUT	Quad1 QPLL1 is locked; there is no this pin if Quad1 QPLL1 is not used.
gt_cppll_ok_o [$N^{[1]}$ -1:0]	OUT	CPLL lock flag per lane

Signal Name	I/O	Description
gt_fabric_rstn_i	IN	PMA reset of the lane connected to the core
gt_pcs_rx_clk_o	OUT	Lane PCS RX clock; if it is multilane, the first lane PCS RX clock is output by default.
gt_pma_rx_lock_o[N ^[1] -1:0]	OUT	Lane RX PMA layer lock indication, 1: lock.
gt_rx_k_lock_o[N ^[1] -1:0]	OUT	Lane Comma lock indication, 1: lock.
gt_rx_align_link_o[N ^[1] -1:0]	OUT	Lane byte alignment indication, 1: alignment.
gt_pcs_rx_rst_i	IN	RX PCS reset of the lane connected to the core
gt_rx_fifo_rdusewd_o[5*N ^[1] - 1:0]	IN	Number of readable data in the lane RX FIFO

Note!

^[1] N in the table means the number of lanes.

^[2] Y in the table means: when PCS is set to 32 bits, Y = 1; when PCS is set to 64 bits, Y = 2.

3.2.3 DRP (Dynamic Reconfiguration Port) Interface

When "DRP Ports" are enabled, the following ports exist as shown in Figure 3-5.

Figure 3-5 DRP Port Diagram

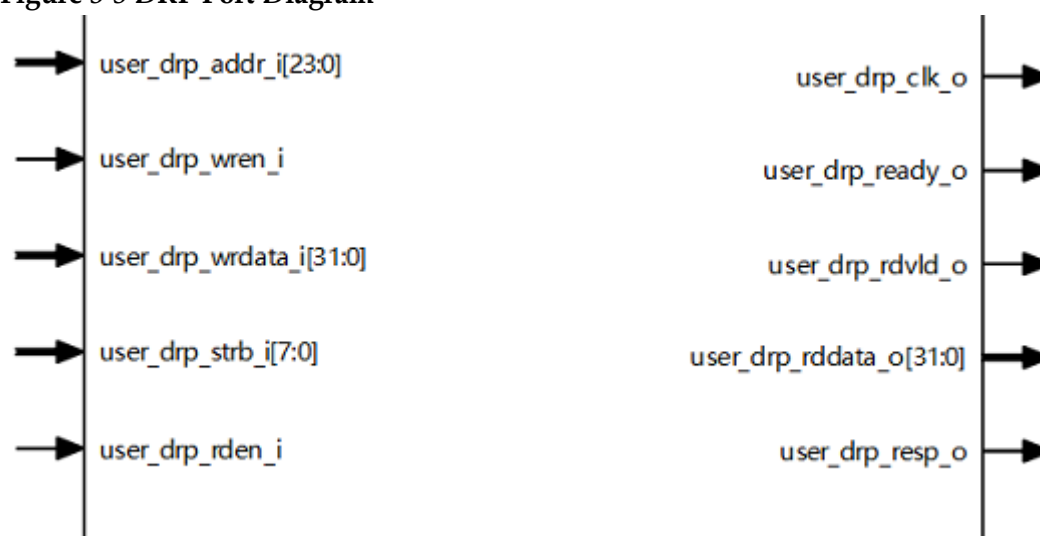


Table 3-3 I/O List of DRP

Signal Name	I/O	Description
user_drp_clk_o	OUT	Synchronization clock signal for DRP interface
user_drp_addr_i[23:0]	IN	Read and write address signals for DRP interface
user_drp_wren_i	IN	Write enable signal for DRP interface
user_drp_wrdata_i[31:0]	IN	Write data signal for DRP interface

Signal Name	I/O	Description
user_drp_strb_i[7:0]	IN	Write mask signal for DRP interface
user_drp_ready_o	OUT	Write handshake signal for DRP interface
user_drp_rden_i	IN	Read enable signal for DRP interface
user_drp_rdvld_o	OUT	Read data valid signal for DRP interface
user_drp_rddata_o[31:0]	OUT	Read data signal for DRP interface
user_drp_resp_o	OUT	read/write operation invalid signal for DRP interface; set to 1 when the read/write address exceeds the accessible space

3.3 Interface Timing

3.3.1 TX Core Interface

Configuration Interface Timing

Internal registers are configured through the bus. Figure 3-5 and Figure 3-6 show the write and read timing of the bus configuration; this interface timing is consistent with the one of APB slave, and can be directly connected to the APB master module.

Figure 3-6 Write Timing Diagram of Configuration Interface

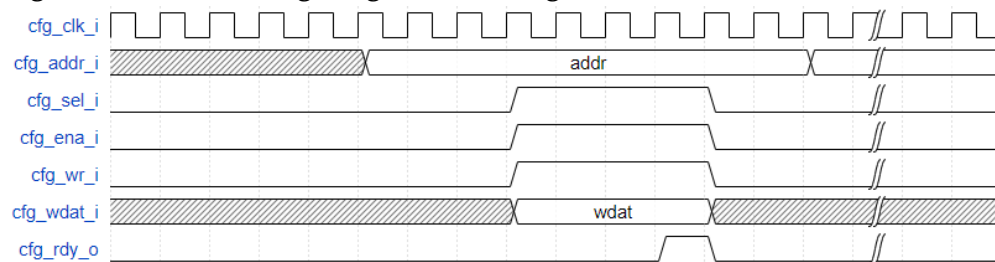
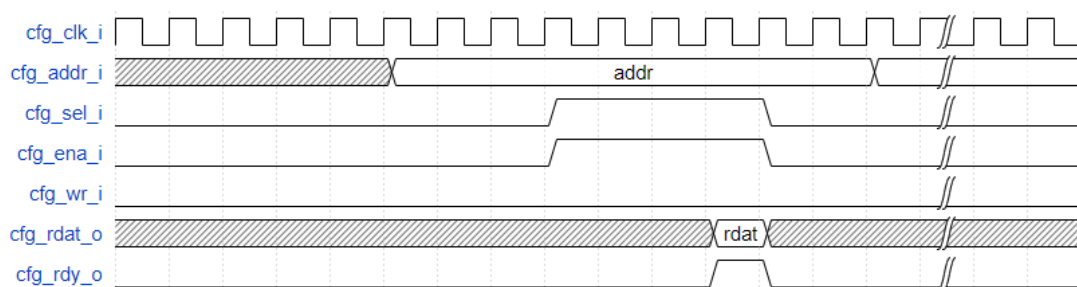
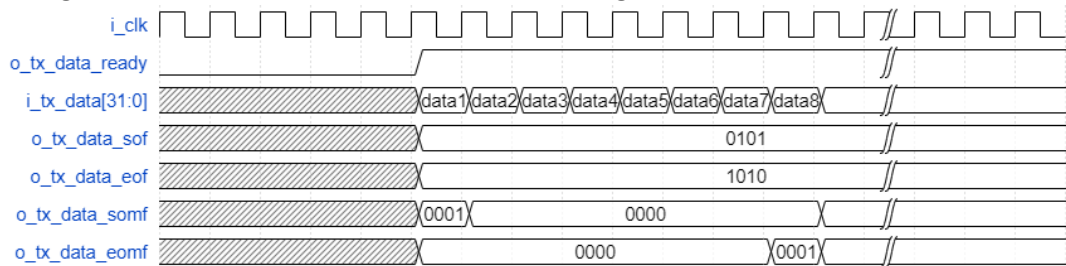


Figure 3-7 Read Timing Diagram of Configuration Interface



Data Interface Timing

Figure 3-8 F=2 K=32, TX Data Interface Timing



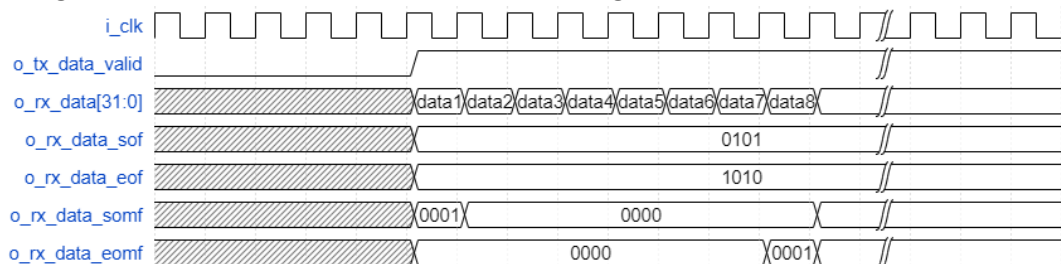
3.3.2 RX Core Interface

Configuration Interfaces

The interface timing of RX core is the same as TX core, and you can see Figure 3-6 and Figure 3-7.

Data Interface Timing

Figure 3-9 F=2 K=32, RX Data Interface Timing

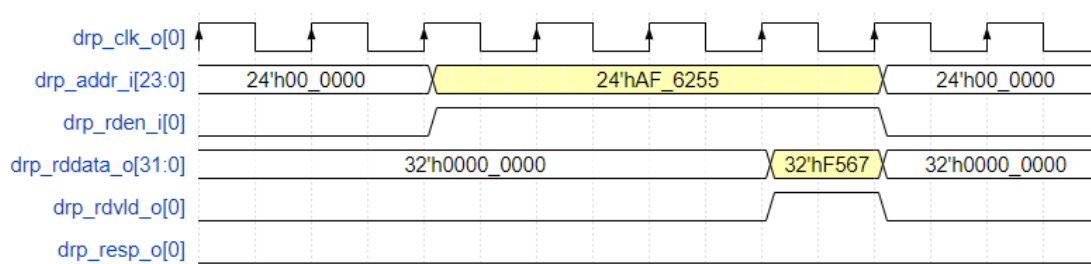
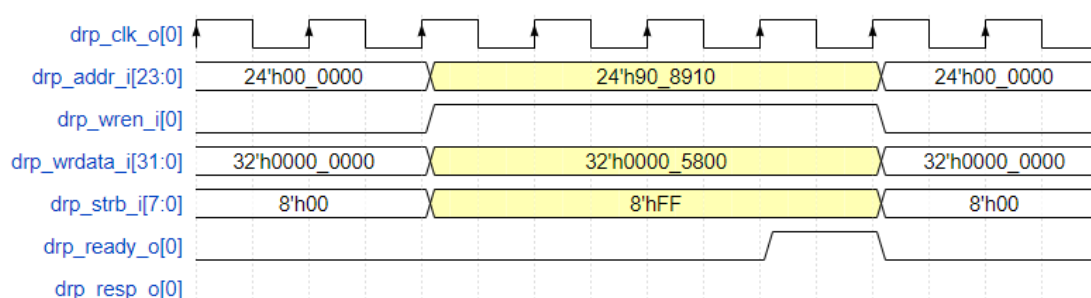


3.3.3 DRP Interface Timing

Gowin JESD204B IP provides DRP interface through which the user can access the SerDes internal registers.

During the read operation, drp_rden_i is set to high, and the read register address is input to drp_addr_i[23:0] in the first clock cycle when drp_rden_i is set to high. drp_rden_i stays high until drp_rdvld_o is set to high; the corresponding drp_rddata_o[31:0] data is the read data returned from the read operation when drp_rdvld_o is high. drp_rden_i should be set to low in the clock cycle immediately following the assertion of drp_rdvld_o to end the current read operation. The DRP interface read timing is shown in Figure 3-10.

During the write operation, drp_wren_i is set to high, and the write register address is input to drp_addr_i[23:0] in the first clock cycle when drp_wren_i is set high, and the write data is input to drp_wrdata_i[31:0] in the same clock cycle; the fixed 8 'hff is input to drp_strb_i[7:0]. drp_wren_i stays high until drp_ready_o is set to high, and drp_ready_o is set high to indicate that this write operation is complete. drp_wren_i should be set to low in the clock cycle immediately following the assertion of drp_ready_o to end the current write operation. The write timing is shown in Figure 3-11.

Figure 3-10 DRP Interface Read Timing Diagram**Figure 3-11 DRP Interface Write Timing Diagram**

3.4 Register Description

Gowin JESD204B IP contains TX and RX cores registers, and is configured through bus interface with addresses in octets.

Table 3-4 Gowin JESD204B IP Registers

RX CORE REGISTER			TX CORE REGISTER	
Address Offset	Description	R/W	Description	R/W
0x000	Reserved	-	Reserved	-
0x004	Version	R	Version	R
0x008	Reset	WR	Reset	WR
0x00C	ILA Support	WR	ILA Support	WR
0x010	Scrambling	WR	Scrambling	WR
0x014	SYSREF Handling	WR	SYSREF Handling	WR
0x018	Test Modes	WR	Test Modes	WR
0x01C	F_and_K.	WR	F_and_K.	WR
0x020	Subclass Mode	WR	Subclass Mode	WR
0x024	Sync Status	R	Sync Status	R
0x028	Link Error Status (Lanes 0 to 7)	R	Reserved	-
0x02C	Alarm Status	R	Alarm Status	R
0x030	RXBUF_DELAY	WR	Reserved	-
0x034	ERR_REPORT	WR	Reserved	-
0x038	LINK_DEBUG	R	Reserved	-
0x040	CLEAR_ERR	WR	Reserved	-

RX CORE REGISTER			TX CORE REGISTER	
0x080	Reserved	-	Lane ID Lane0	WR
0x084	Reserved	-	Lane ID Lane1	WR
0x088	Reserved	-	Lane ID Lane2	WR
0x08C	Reserved	-	Lane ID Lane3	WR
0x090	Reserved	-	Lane ID Lane4	WR
0x094	Reserved	-	Lane ID Lane5	WR
0x098	Reserved	-	Lane ID Lane6	WR
0x09C	Reserved	-	Lane ID Lane7	WR
0x0C0	Lane 0 ILA Config Data 0	R	-	-
0x0C4	Lane 0 ILA Config Data 1	R	-	-
0x0C8	Lane 0 ILA Config Data 2	R	-	-
0x0CC	Lane 0 ILA Config Data 3	R	ILA Config Data 3	WR
0x0D0	Lane 0 ILA Config Data 4	R	ILA Config Data 4	WR
0x0D4	Lane 0 ILA Config Data 5	R	ILA Config Data 5	WR
0x0D8	Lane 0 ILA Config Data 6	R	ILA Config Data 6	WR
0x0DC	Lane 0 ILA Config Data 7	R	ILA Config Data 7	WR
0x0E0	Lane 0 Test Mode Error Count	R	-	-
0x0E4	Lane 0 Link Error Count	R	-	-
0x0E8	Lane 0 Test Mode ILA Count	R	-	-
0x0EC	Lane 0 Test Mode Multiframe Count	R	-	-
0x0F0	Lane 0 Buffer Adjust	R	-	-
0x0F4-0xF4C	Reserved	-	-	-
0x100-0x13C	Same as 0x0c0-0x0fc for lane1	R	-	-
0x140-0x17C	Same as 0x0c0-0x0fc for lane2	R	-	-
0x180-0x1BC	Same as 0x0c0-0x0fc for lane3	R	-	-

Table 3-5 Version [Offset:0x004]

Bit	Default	W/R	Description
31:24	-	-	Reserved
23:16	-	R	Version: Major
15:8	-	R	Version: Minor
7:0	-	R	Version: Revision

Table 3-6 Reset [Offset:0x008]

Bit	Default	W/R	Description
31:1	-	-	Reserved
0	0x0	WR	Reset Write 1 to hold the reset Write 0 to release the reset and the core starts to run.

Table 3-7 ILA Support [Offset:0x00C]

Bit	Default	W/R	Description
31:12	-	-	Reserved
11:4	0x3	WR	The number of multiframe contained in the ILAS Parameter range: 4-256; minus 1 when writing registers. For example, the number of multiframe is 4 by default, and you need to write 3
3:1	-	-	Reserved
0	0x0	WR	1: Enable ILA Support 0: Disable ILA Support

Table 3-8 Scrambling [Offset:0x010]

Bit	Default	W/R	Description
31:1	-	-	Reserved
0	0x0	WR	1: Enable Scrambling 0: Disable Scrambling

Table 3-9 SYSREF Handling [Offset:0x014]

Bit	Default	W/R	Description
31:1	-	-	Reserved
8	-	-	SYSREF Required on Re-Sync - TX core transmits K28.5 until SYSREF re-aligns LMFC. - RX core does not set SYNC until SYSREF re-aligns LMFC. SYSREF is not required on Re-Sync - TX core transmits an ILA sequence in the next LMFC. - RX core sets SYNC in the next LMFC.
7:4	-	WR	SYSREF delay: Add additional delay to SYSREF re-alignment of LMFC counter 1111: 15 core_clk clock cycles delay 0000: 0 core_clk clock cycle delay
3:1	-	-	Reserved
0	0	WR	SYSREF Always 1: Re-aligns LMFC counter on all SYSREFs 0: Only aligns LMFC counter on the first SYSREF

Bit	Default	W/R	Description
			detected following reset, and ignores subsequent SYSREFs.

Table 3-10 Test Modes [Offset:0x018]

Bit	Default	W/R	Description
31:1	-	-	Reserved
2:0	000	WR	Test Mode Selection 000: Normal mode 001: TX/RX K28.5 indefinitely 010: Synchronize as normal then TX/RX repeated ILA sequences 011: TX/RX D21.5 indefinitely 100: TX Modified Random Pattern (RPAT) (TX only) 101: TX Scrambled Jitter Pattern (JSPAT) (TX only)

Table 3-11 F_and_K [Offset:0x01C]

Bit	Default	W/R	Description
31:13	-	-	Reserved
12:8	0x1F	WR	Frames per Multiframe (K) Parameter range 1-32, write register with required value minus 1. For example, F = 32, then 0x1F should be written.
7:0	0x3	WR	Octets per Frame (F) Parameter range 1-256, write register with required value minus 1. For example, F = 4, then 3 should be written.

Table 3-12 Subclass Mode [Offset:0x020]

Bit	Default	W/R	Description
31:2	-	-	Reserved
1:0	0x1	WR	11: Reserved 10: Subclass 2 01: Subclass 1 (currently only subclass 1 is supported) 00: Subclass 0

Table 3-13 Sync Status [Offset:0x024]

Bit	Default	W/R	Description
31:5	-	-	Reserved
4	-	R	SYSREF Captured (Subclass 1 Only) 1: SYSREF captured 0: SYSREF not captured
3:1	-		Reserved

Bit	Default	W/R	Description
0	-	R	SYNC Status 1: Link SYNC completed 1: Link SYNC not completed

Table 3-14 Link Error Status (Lines 0 to 7) [Offset:0x028]

Bit	Default	W/R	Description
31:24	-		Reserved
23:21	-	R	Link Error Status, Lane 7
20:18	-	R	Link Error Status, Lane 6
17:15	-	R	Link Error Status, Lane 5
14:12	-	R	Link Error Status, Lane 4
11:9	-	R	Link Error Status, Lane 3
8:6	-	R	Link Error Status, Lane 2
5:3	-	R	Link Error Status, Lane 1 format is the same as lane 0.
2:0	-	R	Link Error Status, Lane 0 Bit2:1: Unexpected K-character(s) received Bit1:1: 8B10B Disparity Error(s) received Bit0:1: 8B10B Not in Table Error(s) received Each bit indicates that 1 or more errors of that type have been received. Program the 0x40 register to clear the errors

Table 3-15 Alarm Status [Offset:0x02C]

Bit	Default	W/R	Description
31:5	-	-	Reserved
8	-	R	AlignErrDet_alm 1: Multiframe control characters received at illegal locations; an alarm pops up if there are more than 10 character errors or more than 10 character errors of disperr and notintable err.
7	-	-	Reserved
6	-	R	lmfc_cfg_alarm 1: F*K is not an integer multiple of 4
5	-	R	lmfc_size_alarm 1: F*K is not in the [17,1024] range
4	-	R	lmfc_mis_alarm 1: SYSREF misaligned to LMFC
3:1	-	-	Reserved
0	-	R	RxBufOverflow_alm 1: RX lane alignment buffer overflow

Table 3-16 RXBUF_DELAY (RX ONLY) [Offset:0x030]

Bit	Default	W/R	Description
31:10	-	-	Reserved
9:0	0	WR	RX buffer latency can be programmed in conjunction with the RX Buffer Adjust values read from the lanes to minimize overall RX latency.

Table 3-17 ERR_REPORT (RX ONLY) [Offset:0x034]

Bit	Default	W/R	Description
31:5	-	-	Reserved
4	0	WR	Reserved
3:1	-	-	Reserved
0	0	WR	Link Error Counters Enable 1: Enable link error counters (Link errors are counted and reported using Link Error Count registers per lane) 0: Disable link error counters

Table 3-18 LINK_DEBUG (RX ONLY) [Offset: 0x038]

Bit	Default	W/R	Description
31:28	-	R	Link Debug status Lane 7 as per lane 0
27:24	-	R	Link Debug status Lane 6 as per lane 0
23:20	-	R	Link Debug status Lane 5 as per lane 0
19:16	-	R	Link Debug status Lane 4 as per lane 0
15:12	-	R	Link Debug status Lane 3 as per lane 0
11:8	-	R	Link Debug status Lane 2 as per lane 0
7:4	-	R	Link Debug status Lane 1 as per lane 0
3:0	-	R	Link Debug status Lane 0 BIT3:1: Start of data detected BIT2:1: Start of ILA detected BIT1:1: Lane has completed Code Group Sync (CGS) BIT0:1: Lane is receiving K28.5

Table 3-19 ERR_CLEAR [Offset:0x040]

Bit	Default	W/R	Description
31:1	-	-	Reserved
0	0	WR	0: Enable the detection 1: Clears the four errors, such as AlignErrDet, unexpected K-character(s) received, 8B10B disparity errors, 8B10B Not in Table errors, and disable the detection.

Table 3-20 Lane ID [Offset: lane0-0x080, lane1-0x084 lane7-0x09C]

Bit	Default	W/R	Description
31:5	-	-	Reserved
4:0	N	WR	The ID of lane N The value can be any value between 0 and 31. The default value N is set to the lane number.

Note!

This is a register that is included per lane.

Table 3-21 ILA Config Data 0 [Offset: lane0-0x0C0, lane1-0x100 lane7-0x280]

Bit	Default	W/R	Description
31:7	-	-	Reserved
6:4	-	R	JESD204 version 000: JESD204A 001: JESD204B
3	-	-	Reserved
2:0	-	R	Subclass: 000- Subclass 0 001- Subclass 1 010- Subclass 2

Note!

This is a register that is included per lane (RX core only).

Table 3-22 ILA Config Data 1 [Offset: lane0-0x0C4, lane1-0x104 lane7-0x284]

Bit	Default	W/R	Description
31:8	-	-	Reserved
7:0	-	R	F (Octets per Frame), binary value minus 1.

Note!

This is a register that is included per lane (RX core only).

Table 3-23 ILA Config Data 2 [Offset: lane0-0x0C8, lane1-0x108 lane7-0x288]

Bit	Default	W/R	Description
31:5	-	-	Reserved
4:0	-	R	K (Frames per Multiframe), binary value minus 1.

Note!

This is a register that is included per lane (RX core only).

Table 3-24 ILA Config Data 3 [Offset: lane0-0x0CC, lane1-0x10C lane7-0x28C]

Bit	Default	W/R	Description
31:22	-	-	Reserved
21:17	-	R(RX)	L (Lanes per Link), binary value.
16:12	-	R(RX)	LID (Lane ID), binary value
11:8	0x0	R(RX) WR(TX)	BID (bank ID), binary value. For TX core, set the field to be transmitted in the ILA sequence for all lanes. For RX core, capture the field from the ILA sequence per lane.
7:0	0x00	R(RX) WR(TX)	DID (Device ID). Binary value For TX core, set the field to be transmitted in

Bit	Default	W/R	Description
			the ILA sequence for all lanes. For RX core, capture the field from the ILA sequence per lane.

Note!

This is a register that is included per lane.

Table 3-25 ILA Config Data 4 [Offset: lane0-0x0D0, lane1-0x110 lane7-0x290]

Bit	Default	W/R	Description
31:21	-	-	Reserved
20:16	-	R(RX) WR(TX)	N' (Totals bits per Sample), binary value minus 1
15:13	-	-	Reserved
12:8	0x0	R(RX) WR(TX)	N (Converter Resolution), binary value minus 1 For TX core, set the field to be transmitted in the ILA sequence for all lanes. For RX core, capture the field from the ILA sequence per lane.
7:0	0x00	R(RX) WR(TX)	M (Convertors per Device), binary value minus 1 For TX core, set the field to be transmitted in the ILA sequence for all lanes. For RX core, capture the field from the ILA sequence per lane.

Note!

This is a register that is included per lane.

Table 3-26 ILA Config Data 5 [Offset: lane0-0x0D4, lane1-0x114 lane7-0x294]

Bit	Default	W/R	Description
31:21	-	-	Reserved
20:16	-	R(RX) WR(TX)	CF (Control Words per Frame). Binary value For TX core, set the field to be transmitted in the ILA sequence for all lanes. For RX core, capture the field from the ILA sequence per lane.
15:13	-	-	Reserved
12	-	R(RX) WR(TX)	HD (High Density format) For TX core, set the field to be transmitted in the ILA sequence for all lanes. For RX core, capture the field from the ILA sequence per lane.
11:9	-	-	Reserved
8:4	0x0	R(RX) WR(TX)	S (Samples per Converter per Frame). Binary value minus 1 For TX core, set the field to be transmitted in the ILA sequence for all lanes. For RX core, capture the field from the ILA sequence per lane.
3:1	-	-	Reserved
0	0x00	R(RX)	SCR (Scrambling Enable)

Bit	Default	W/R	Description
			1: Enable

Note!

This is a register that is included per lane.

Table 3-27 ILA Config Data 6 [Offset: lane0-0x0D8, lane1-0x118 lane7-0x298]

Bit	Default	W/R	Description
31:28	-	-	Reserved
27:20	0x0	R(RX)	FCHK (Checksum), binary value
19:12	0x0	R(RX) WR(TX)	RES2 (Reserved Field 2) For TX core, set the field to be transmitted in the ILA sequence for all lanes. For RX core, capture the field from the ILA sequence per lane.
11:4	0x0	R(RX) WR(TX)	RES1 (Reserved Field 1) For TX core, set the field to be transmitted in the ILA sequence for all lanes. For RX core, capture the field from the ILA sequence per lane.
3:2	-	-	Reserved
1:0	0x0	R(RX) WR(TX)	CS (Control bits per Sample). Binary value For TX core, set the field to be transmitted in the ILA sequence for all lanes. For RX core, capture the field from the ILA sequence per lane.

Note!

This is a register that is included per lane.

Table 3-28 ILA Config Data 7 [Offset: lane0-0x0DC, lane1-0x11C lane7-0x29C]

Bit	Default	W/R	Description
31:9	-	-	Reserved
8	0x0	R(RX) WR(TX)	ADJDIR (Adjust Direction) [Subclass 2 Only]. Binary value For TX core, set the field to be transmitted in the ILA sequence for all lanes. For RX core, capture the field from the ILA sequence per lane.
7:5	-	-	Reserved
4	0x0	R(RX) WR(TX)	PHADJ (Phase Adjust Request) [Subclass 2 Only]. Binary value For TX core, set the field to be transmitted in the ILA sequence for all lanes. For RX core, capture the field from the ILA sequence per lane.
3:0	0x0	R(RX) WR(TX)	ADJCNT (Number of Adjustment Resolution Steps) [Subclass 2 Only]. Binary value For TX core, set the field to be transmitted in the ILA sequence for all lanes. For RX core, capture the field from the ILA

Bit	Default	W/R	Description
			sequence per lane.

Note!

This is a register that is included per lane.

Table 3-29 Test Mode Error Count [Offset: lane0-0x0E0, lane1-0x120 lane7-0x2A0]

Bit	Default	W/R	Description
31:0	-	R	Test Mode Error Count Test Mode: 001 (Continuous K28.5): Count any non K28.5 characters received Test Mode: 010 (Continuous ILA): Count any unexpected characters received This count resets to zero when test mode changes.

Note!

This is a register that is included per lane.

Table 3-30 Link Error Count [Offset: lane0-0x0E4, lane1-0x124 lane7-0x2A4]

Bit	Default	W/R	Description
31:0	-	R	Link Error Count Count the total received link errors (per lane) when Link Error Counters is Enabled. Errors counted are Disparity Errors or Not In Table errors indicated by the lane. The error counter can be reset by disabling and re-enabling using the control bit in the Error Reporting register.

Note!

This is a register that is included per lane.

Table 3-31 Test Mode ILA Count [Offset: lane0-0x0E8, lane1-0x128 lane7-0x2A8]

Bit	Default	W/R	Description
31:0	-	R	Test Mode ILA Count Count the total ILA Sequences received when Test Mode = 010 (Continuous ILA).

Note!

This is a register that is included per lane.

Table 3-32 Test Mode Multiframe Count [Offset: lane0-0x0EC, lane1-0x12C . lane7-0x2AC]

Bit	Default	W/R	Description
31:0	-	R	Test Mode Multiframe Count Count the total ILA multiframe received when Test Mode = 010 (Continuous ILA).

Note!

This is a register that is included per lane.

Table 3-33 Buffer Adjust [Offset: lane0-0x0F0, lane1-0x130 lane7-0x2B0]

Bit	Default	W/R	Description
31:10			Reserved
9:0	-	R	RX Buffer Adjust Indicate the RX Buffer fill level (per lane)

Note!

This is a register that is included per lane.

4 Design Considerations

4.1 Line Rate

The JESD204B specification does not define a specific serial line rate for any JESD204B link. The JESD204B core supports line rates depending on the selection of the device and speed grade.

In most cases, the serial line rate selection depends on the specifications of the ADC/DAC device(s) to which the core is connected. The required operating serial line rate is directly related to the clock rate for the core logic operation (core clock); the serial line rate also determines the choice of the reference clock required by the transceiver.

4.2 Clock

4.2.1 Core Clock (core clk)

The JESD204B core clock is determined based on the PCS bit width. When 32 bits is selected for the PCS bit width, the JESD204B core operates using a 32-bit (4-byte) data path. The core clock frequency is the line rate divided by 40. For example, for a serial line rate of 4.9152 Gbs, the core clock frequency is 122.88 MHz. The RX and TX data interfaces operates at this core clock frequency.

When 64 bits is selected for the PCS bit width, the JESD204B core operates using a 64-bit (8-byte) data path. The core clock frequency is the line rate divided by 80. For example, for a serial line rate of 9.8304 Gbs, the core clock frequency is 122.88 MHz. The data stream RX and TX data interfaces operates at this core clock frequency.

This clock will be connected not only to the JESD204B core, but also to the internal SerDes PCS clock interface.

4.2.2 Reference Clock

The serial transceivers require a stable, low-jitter reference clock which has a device and speed grade dependent range. The selection of the reference clock requires confirmation that the required line rate is supported.

4.2.3 Configuration Clock (cfg clk)

The core reads and writes registers through the configuration interface. The clock for this interface is independent of the core clock or the reference clock. There are no dependencies between this clock and the core clock or the reference clock.

4.2.4 SerDes PCS Clock

The JESD204B core outputs the SerDes lane PCS RX clock; if it is multilane, the first lane PCS RX clock is output by default. This clock frequency is the same as the core clock. It is also possible to connect the `gt_pcs_tx_clk_o` or `gt_pcs_rx_clk_o` pin to the `core_clock` port to use as the core clock.

4.2.5 Generic Clock Scheme

Figure 4-1 Generic Clock Scheme

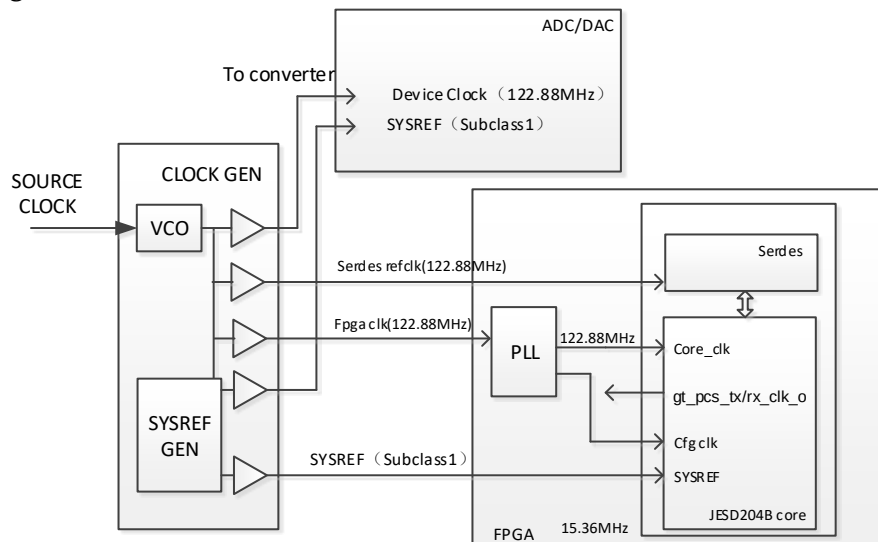


Figure 4-1 shows the most generic and flexible clock scheme, where the external clock generation unit provides SerDes reference clock and FPGA fabric clk, respectively. With this configuration, the reference clock and core clock are physically separate clocks and can operate at independent frequencies without additional constraints. The reference clock can operate at any frequency within the limitations of the transceiver for the selected line rate. The fabric clock (or the clock with PLL) always runs at the desired rate.

The configuration clock `cfg_clk` is independent of both the core clock and the reference clock in terms of source and frequency.

The frequency values such as 122.88MHz shown in the above figure are an example; in the actual use, it can be any other frequency.

4.3 Reset

4.3.1 Bus Reset Port

The bus configuration interface provides a separate reset signal (tx/rx_cfg_rstn_i), the register reset is the default.

4.3.2 Reset Core Logic via Pins

It provides an asynchronous reset to reset the overall core logic. On the TX core, this signal is tx_rst_i and on the receiver, this signal is rx_rst_i. The bus configuration and the registers are unaffected by these reset signals.

4.3.3 Reset Core Logic via Registers

A register 0x8 is provided through the bus configuration interface, which triggers a reset operation of the TX or RX logic data path via software. The registers are not affected by this operation. Its function is the same as the reset via pin.

4.3.4 SerDes Related Reset

The JESD204B core connecting to SerDes provides an interface for PMA and PCS resets, and the gt_fabric_rstn_i pin is active for both transceiver PMA.

4.3.5 Reset Flow

Users can reset via pins. After loading FPGA, both SerDes and core are in reset state, release SerDes and core reset in turn, then the overall logic starts to operate.

The recommended flow is as follows:

TX Core

1. Pull up tx_rst_i or set register 0x8 to 1 after power up.
2. If the QPLL or CPLL LOCK signal is locked, it means the reference clock is ready.
3. Use the gt_fabric_rstn_i pin to reset SerDes PMA.
4. If it is a TX core, reset tx_rst_i, and the TX core logic starts to operate.

RX Core

1. Pull up rx_rst_i or set register 0x8 to 1 after power up.
2. If the QPLL or CPLL LOCK signal is locked, it means the reference clock is ready.
3. Use the gt_fabric_rstn_i pin to reset SerDes PMA.
4. When TX ready, check the status of gt_pma_rx_lock_o, gt_rx_k_lock_o, gt_rx_align_link_o; if all of them are high, reset rx_rst_i and the RX core logic starts to operate.

4.4 Subclass

The JESD204B specification includes three subclasses: Subclass0, Subclass1, and Subclass2. The JESD204B core supports only subclass 1 for now.

4.5 SYSREF

4.5.1 SYSREF Timing

When JESD204B is used in Subclass 1, the SYSREF signal is the master timing reference for the system. To achieve accurate deterministic latency, the SYSREF signal and the core clock must be captured synchronously. When 32 bits is selected for the PCS bit width, the SYSREF period must be a multiple of 4-byte clock cycle because the core uses a 4-byte internal data path. When 64 bits is selected for the PCS bit width, the SYSREF cycle must be a multiple of the 8-byte clock cycle because the core uses an 8-byte internal data path.

Proper SYSREF handling is critical in Subclass 1 operations. The JESD204B specification allows SYSREF to be generated in any of the following ways:

- Periodic
- One-Shot
- Gapped Periodic

The JESD204B core provides several options for how subclass 1 operations handle SYSREF to support maximum flexibility.

The SYSREF cycle must be an integer multiple of the multiframe cycle and also satisfy the relationship of being an integer multiple of 4 bytes (PCS = 32 bits) or 8 bytes (PCS = 64 bits).

4.5.2 SYSREF Always

The core provides a programmable option that allows selection of how periodic SYSREF is used internally. This is selected using the SYSREF Always control bit in the SYSREF handling register, as shown in Table 3-9.

When SYSREF Always is set to 0, only the initial SYSREF event seen after a reset (or when the link is resynchronized) is used to align the internal LMFC counter.

When SYSREF Always is set to 1, all SYSREF events are used to (re)align the LMFC counters. This setting requires that the SYSREF period be the correct multiple of the multiframe period.

4.5.3 SYSREF on Initial Link Established

After reset, the JESD204B core requires at least one SYSREF event to align the internal LMFC counters and to initiate the link:

- The RX core requires an initial SYSREF event to align the LMFC, and then pulls up SYNC at the next LMFC boundary when code-group synchronization has been implemented. The SYNC is not pulled up in

the core until the initial SYSREF event is detected.

- The TX core requires a SYSREF event to align the LMFC. After SYNC is invalidated, the kernel starts transmitting ILAs on the LMFC boundary. The core does not begin ILA transfers until the initial SYSREF event is detected.

The system must ensure that the SYSREF for the JESD204B core is generated after the core completes its reset. This is especially important if the system is running One-shot SYSREF.

4.5.4 SYSREF on Link Resynchronization

When a link resynchronization is requested after the initial link is brought up (deasserting SYNC by receiving device), the SYSREF-related behavior can be controlled using the SYSREF required on re-sync control bits in the SYSREF handling register.

When SYSREF Required on Re-Sync is set to 0, a SYSREF event is not required for link resynchronization (assuming the LMFC counter continues to run freely and remains valid).

- For RX core, SYNC is pulled up at the next LMFC boundary after the code group is synchronized.
- The TX core sends an ILA sequence at the next LMFC boundary after SYNC is invalid.

When SYSREF Required on Re-Sync is set to 1, the link requires a SYSREF event to re-establish SYNC after a re-sync request.

- The RX core waits for a SYSREF event to realign the LMFC counters, and pulls up SYNC only at the next LMFC boundary.
- The TX core waits for a SYSREF event to realign the LMFC counters, and then start an ILA transfer at the LMFC boundary after a SYNC is pulled up.

4.5.5 SYSREF Delay

The deterministic latency mechanism defined in the JESD204B standard requires a multiframe size larger than the maximum possible delay on the link. In practice, this is difficult to achieve, especially for small frame sizes. However, deterministic delay can be achieved as long as the multiframe size is larger than the maximum change in delay on the link.

A potential problem arises when the maximum delay variation causes the latency delay to cross the boundary between two adjacent LMFC periods. In this case, a latency change of exactly one LMFC period can be observed between system restarts.

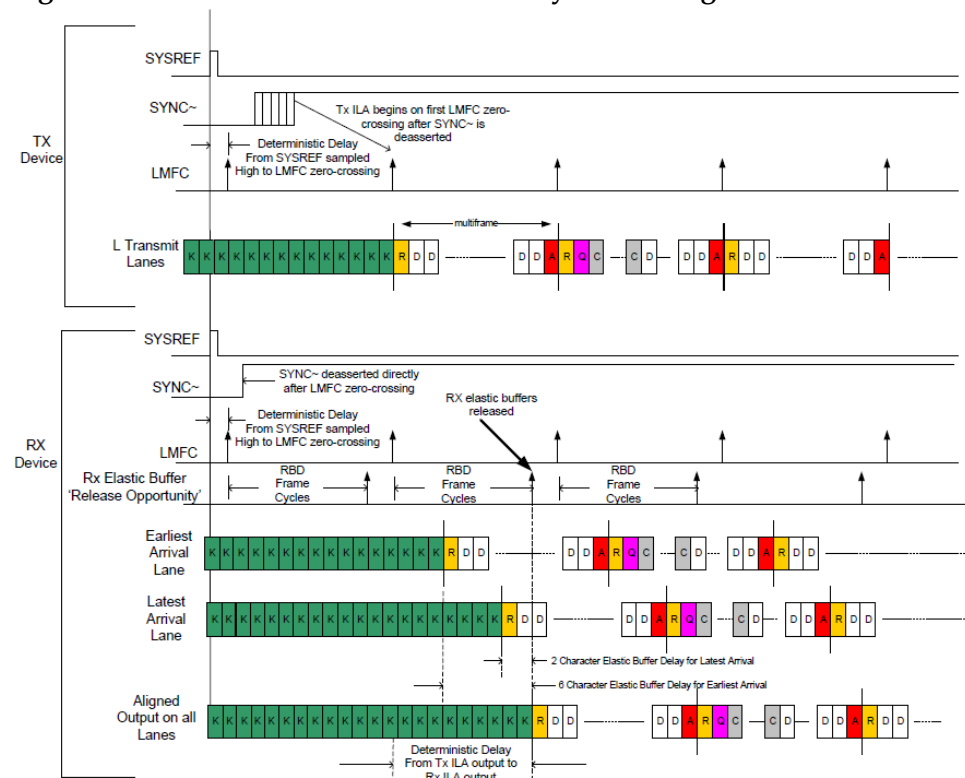
In this case, the LMFC boundary in the TX or RX device can be moved relative to each other by adding additional delay to SYSREF in one of the devices. The JESD204B core supports this shift of the internal LMFC by allowing additional delays in the internal SYSREF handling logic. This is programmed using the SYSREF delay field in the SYSREF register, which allows a delay of 0 to 15 core clock cycles to be inserted

between SYSREF event detection and LMFC counter reset. Changes in the SYSREF delay value require a core reset to force the link to realign.

4.6 Minimum Deterministic Latency Support

The receiver outputs data when the JESD204B link is first established in a subclass 1 device. After valid data is detected in all lanes, data is output at the LMFC crossing. The minimum delay can be supported by adjusting the number of octets entered on the buffer_delay register. An indication of the maximum allowable delay reduction is output on the buffer_adjust register. This provides an indication of the difference between the write and read pointers of the receiver elastic buffer in each lane. The number of octets output in each 10-bit value indicates the buffer fill level in each lane. The given minimum number can be used to calculate a value that can be programmed into the buffer_delay register to reduce the overall latency by that number of octets. The maximum value programmed into the buffer delay register must take into account the octets margin described in implementing repeatable latency, and therefore should not be greater than the lowest buffer_adjust value minus 8. The reset of the JESD204B RX core and the full link resynchronization cycle must occur before the modified latency setting takes effect. The following figure shows an example of the minimum latency.

Figure 4-2 Minimum Deterministic Latency Block Diagram



4.7 Link Test Mode

4.7.1 Continuous K28.5 Characters

This mode transmits K28.5 characters continuously; you need to set TX core register 0x18 to 0x1 to enable this mode.

The receiver will receive K28.5 continuously, and the Test Mode Error Count register of each lane will record the number of all non-K28.5 characters; and you need to set RX core register 0x18 to 0x1 to enable this mode.

4.7.2 Continuous ILA Sequence

In this mode, the transmitter will keep transmitting ILA sequences after receiving SYNC assertion, and you need to set TX core register 0x18 to 0x2 to enable this mode.

The receiver will keep counting the number of ILAs after the ILA sequence received; the Test Mode Error Count register of each lane will record the number of ILA sequences received; and you need to set RX core register 0x18 to 0x2 to enable this mode.

At the same time, the Test Mode ILA Count register of each lane will record the number of ILA sequences, and the Test Mode Multiframe Count of each lane will record the number of multiple frames.

4.7.3 Continuous D21.5 Characters

This mode transmits D21.5 characters continuously; you need to set TX core register 0x18 to 0x3 to enable this mode.

4.7.4 RPAT

This mode transmits a continuous random sequence. This mode is generated by the RPAT module and must be selected in Gowin IDE and will take up additional resources. You need to set TX core register 0x18 to 0x4 to enable this mode.

4.7.5 JSPAT

This mode transmits a continuous random sequence. This mode is generated by the RPAT module and must be selected in Gowin IDE and will take up additional resources. You need to set TX core register 0x18 to 0x5 to enable this mode.

4.8 Real-time Configuration

The runtime operations of the JESD204B core is configured through the APB register interface. For more information on register mapping, see [3.4 Register Description](#).

In order to properly operate and initialize JESD204B link, the main framing and link operation parameters must match on both ends of the link:

- Number of octets per frame

- Number of frames per multiframe
- Scrambling on/off
- Subclass mode
- SYSREF handling (for subclass 1 mode)

These parameters are determined by the configuration available in the ADC/DAC converter to which the core is connected.

For the TX core, in addition to these parameters, some additional elements of the configuration data transmitted in the ILA sequence at link initialization are programmed through the register interface. The data values transmitted in the ILA configuration data are usually not important for the link operation, but this depends on the behavior of the receiver.

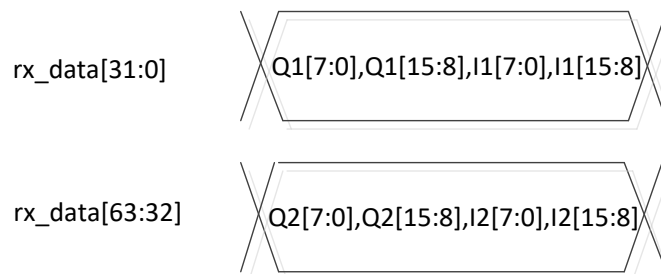
For the RX core, the configuration data received in the ILA sequence is captured; for each lane, you can be check using the register interface.

After the configuration registers are completed, a core reset operation is required in order to allow the core to operate properly.

4.9 Data Interface

The DATA Stream TX and RX interfaces are used to pass JESD204B formatted data to and from the core. The data input and output by the core contains 4-byte per clock cycle per lane with the least significant byte position in each 32-bit block holding the first byte received from the ADC or transmitted to the DAC. Figure 4-3 shows an example of how the JESD204B data is mapped to the DATA Stream interface.

Figure 4-3 Data Stream Interface Data Format



For example, ADI AD9371 ADC 4 converters, 2-lane mode.

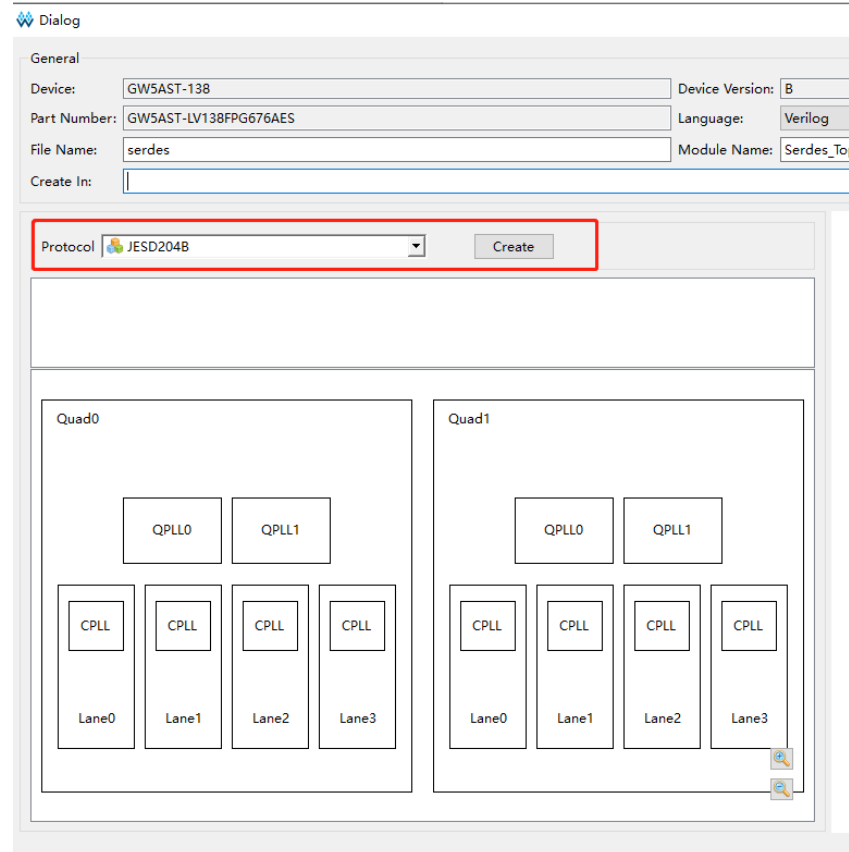
122.88 MHz sampling rate, 4.9152 Ghz lane rate; for the converter with 16-bit width, the core clock is 122.88 MHz.

- `Adc0_sample = {rx_data[07:00],rx_data[15:08]};`
- `Adc1_sample = {rx_data[23:16],rx_data[31:24]};`
- `Adc2_sample = {rx_data[39:32],rx_data[47:40]};`
- `Adc3_sample = {rx_data[55:48],rx_data[63:56]};`

5 Interface Configuration

Find SerDes IP in the IP library, click SerDes IP and Figure 5-1 pops up. Select "JESD204B" in the protocol box, then click "Create" button, and the interface configuration of JESD204B IP pops up.

Figure 5-1 Open SerDes IP



Gowin JESD204B IP configuration interface is shown in Figure 5-2.

Figure 5-2 JESD204B Core Configuration Tab

The screenshot shows the 'JESD204B Core Configuration' tab with the following settings:

- Core Mode:** Radio buttons for 'Receive', 'Transmit', and 'Both Receive and Transmit' (selected).
- Number of Lanes:** A dropdown menu set to '2'.
- LMFC Buffer (Receiver parameter):** A dropdown menu set to '1024'.
- Pattern Generator (Transmitter parameter):** Two checkboxes, 'Include RPAT Generator' and 'Include JSPAT Generator', both are unchecked.
- Link Parameters:**
 - Default SYSREF Always: 'Always Off' (dropdown)
 - Default Scrambling ON/OFF: 'Scrambling OFF' (dropdown)
 - Default F(Octets per Frame): '4' (text input, range 1~256)
 - Default K(Octets per MultiFrame): '32' (text input, range 1~32)
 - Default SYSREF Required on Re-Sync: 'Not Required' (dropdown)
 - Fixed Config Enable: unchecked checkbox
- Clock Options:**
 - Config Clock Frequency(MHz): '10.0' (text input, range 1~100)

- Core Mode: You can select "Receive", "Transmit", and "Both Receive And Transmit".
- Number of Lanes: Indicates the number of lanes in the core with value of 1-8.
- LMFC Buffer: A buffer (Octet) supported by lane alignment and deterministic latency. The LMFC Buffer Size option allows the use of minimal resources where appropriate. LMFC Buffer size should be larger than the maximum multiframe size used in the implemented design (multiframe size is $F \times K$, where F = number of octets per frame; K = number of frames per multiframe)
- Pattern Generator: If necessary, select "Include RPAT Generator" or "Include JSPAT Generator" to generate the logic needed for these test patterns, which will require additional resources.

- **Default Link Parameters:** All parameters are used to set the default values of the registers, refer to the definition of the registers. If the relevant registers are written using the configuration bus during runtime, the default values will be overwritten.
- **Default SYSREF Always:** Sets the initial value of the SYSREF Always field in register 0x14.
- **Default Scrambling ON/OFF:** Sets the initial value of Scrambling field in register 0x10.
- **Default F:** Sets the initial value of F field in register 0x1C.
- **Default K:** Sets the initial value of K field in register 0x1C.
- **Default SYSREF Required on Re-Sync:** Sets the initial value of SYSREF Required on Re-Sync field in register 0x14.
- **Fixed Config Enable:** When enabled, the IP core will not be able to dynamically modify the F and Scrambling parameters, but will be able to reduce logic resources, while timing performance can be improved.
- **Config Clock Frequency:** Sets the clock frequency of the configuration bus, and the frequency range can be from 1MHz to 100MHz.

Figure 5-3 PHY Configuration Tab

The screenshot displays the 'PHY Configuration' tab within the 'JESD204B Core Configuration' window. The interface is divided into two main sections: 'Base Parameters' and 'Lane Connect'.

Base Parameters:

- PCS WIDTH:** Two radio buttons are present: '32bit' (selected) and '64bit'.
- Line Rate(Gbps):** A text input field containing the value '4.9152'.
- Reference Clock Source:** A dropdown menu showing 'Q1 REFCLK0'.
- Reference Clock Frequency(MHz):** A text input field containing the value '122.88'.
- PLL Selection:** A dropdown menu showing 'QPLL1'.
- Loopback Mode:** A dropdown menu showing 'LB_NES'.
- Calculate:** A button located to the right of the PLL Selection dropdown.

Lane Connect:

This section lists eight JESD204B lanes and their connection targets:

- JESD204B Lane0 connect with: Q1 Lane0
- JESD204B Lane1 connect with: Q1 Lane1
- JESD204B Lane2 connect with: Q0 Lane2
- JESD204B Lane3 connect with: Q0 Lane3
- JESD204B Lane4 connect with: Q1 Lane0
- JESD204B Lane5 connect with: Q1 Lane1
- JESD204B Lane6 connect with: Q1 Lane2
- JESD204B Lane7 connect with: Q1 Lane3

- PCS WIDTH: Sets PCS bit width; it affects the core clock frequency and data input/output bit width. When it is difficult to meet timing requirements with a 32-bit width in certain scenarios, a 64-bit width is needed.
- Line Rate: Lane line rate.
- Reference_Clock_Source: Reference clock source; you can select clock source 0 and 1, which is related to the pin connection.
- Reference_Clock_Frequency: Reference clock.

Note!

There is a limitation between the line rate and the reference clock; make sure that the reference clock can generate the above line rate.

- PLL Selection: PLL source; you can select QPLL0, QPLL1, CPLL, etc.
- Loopback_Mode: Loopback mode; you can select OFF, LB_NES, LB_FES, LB_ENC, etc.
- Calculate: This option is used to check whether the correspondence between line rate and reference clock is reasonable.
- JESD204B LaneX connect with: This option is used to set the lane correspondence between JESD204B and SerDes. After the parameters are configured, click "OK"; SerDes interface shows the configured protocols and lane locations, as well as the use of PLL.

Figure 5-4 AFE Tab

The screenshot shows the 'AFE' configuration tab with the following settings:

Section	Parameter	Value	Range
TX	Differential Swing	900mV	
	FFE Mode	Auto	
	Cm	0	(0~19)
	C0	40	(21~40)
RX	SD Threshold	100mV	
	Equalization Mode	Auto	
	ATT	7	(0~10)
	BOOST	9	(0~15)
	BIAS	7	(0~15)

- Differential Swing: TX differential swing, and the range is 180mV~900mV.
- FFE mode: FFE operating mode; when Auto is selected, SerDes automatically adjusts FFE coefficients according to the hardware environment, at this time, Cm, C0 and C1 configurations are invalid. When Manual is selected, user can adjust Cm and C1 coefficients manually; C0 is calculated automatically according to Cm and C1 coefficients, and there is no need to set.

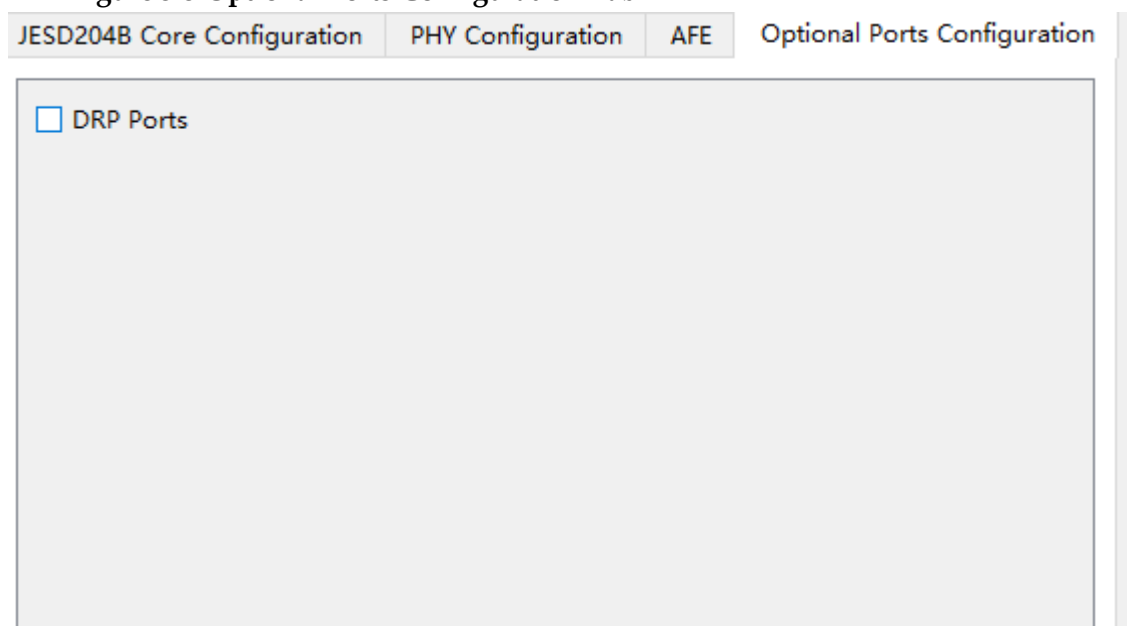
- **SD Threshold:** Valid voltage threshold for RX signals; when receive differential signal is greater than threshold, Serdes judges that valid data is received; when receive differential signal is less than threshold, Serdes judges that valid data is not received and enters into Electrical Idle state.
- **Equaliaztion Mode:** RX Equalization Mode; when Auto is selected, the equalizer is in automatic mode. The equalizer will automatically adjust the equalizer to the best state according to the current quality of the received data when SerDes RX link-up is established; and the ATT and BOOST options are not configurable at this time. When Manual is selected, the equalizer is in manual mode. The user needs to manually configure the ATT and BOOST options to optimize the equalizer.
- **ATT:** Attenuator, used to adjust the receive Intermediate frequency attenuation. Smaller value means higher attenuation with the range 0~10.
- **BOOST:** Analog boost, used to adjust the receive high frequency amplification. Larger value means higher gain with the range 0~15.

Note!

If users configure the equalizer as Manual, they need to keep trying the combination of ATT and BOOST options to make the SerDes reach the optimal state. Therefore, it is recommended that users prioritize Auto mode. If Auto mode is not able to adapt to the optimal state, you can try Manual mode.

- **BIAS:** Used to configure the amplification parameters of SerDes for the RX signals. When the RX signal rate is high and the attenuation is high, the user can change the configuration of this option. The higher the configuration of this option, the stronger the amplification of the signal. This option is based on the QUAD configuration. When changing the configuration of one lane, it will change the configuration of all the lanes in the Quad where the current lane is located.

Figure 5-5 Optional Ports Configuration Tab

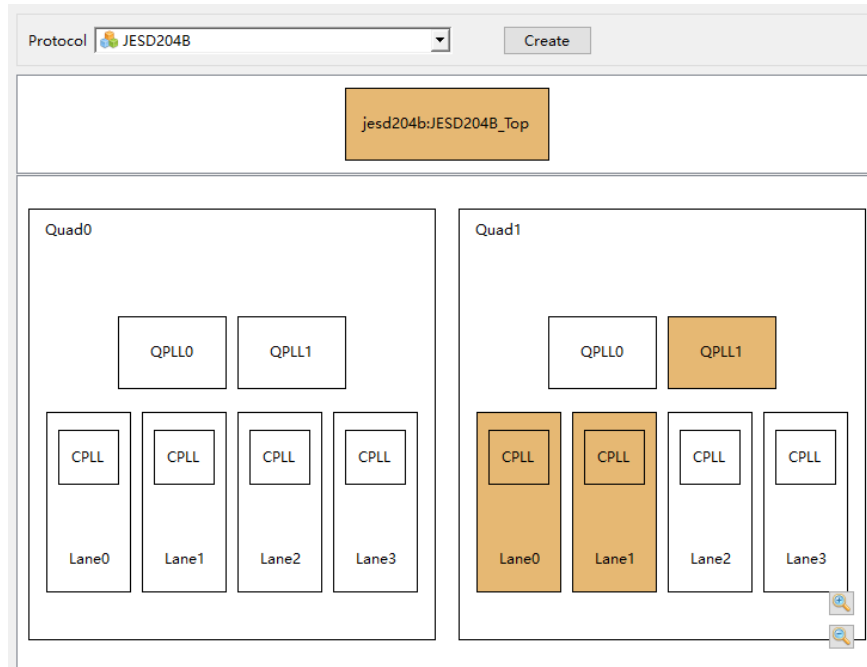


DRP Ports: Used to dynamically configure SerDes through the DRP

interface, such as dynamically configuring loopback and other functions.

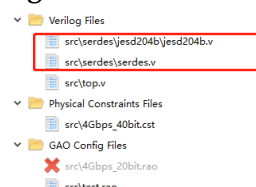
After the parameters are configured, click "OK", and the SerDes interface shows the configured protocols and lane locations, as well as the PLL usage.

Figure 5-6 jesd204b: JESD204B_Top



Then click "OK" again, the jesd204b IP file and a text file containing the primitives of SerDes such as serdes.v will be generated and will be added to the project automatically; users just need to invoke it.

Figure 5-7 Generated Files



```

6 //Device: GW5AST-138B
7 //Device Version: 8
8 //Created Time: Tue May 16 10:28:47 2023
9
10 //Change the instance name and port connections to the signal names
11 //-----Copy here to design-----
12
13 Serdes_Top your_instance_name(
14     .JESD204B_Top_tx_cfg_rdata_o(JESD204B_Top_tx_cfg_rdata_o_o), //output
15     .JESD204B_Top_tx_cfg_rdy_o(JESD204B_Top_tx_cfg_rdy_o_o), //output JESD
16     .JESD204B_Top_tx_data_ready_o(JESD204B_Top_tx_data_ready_o_o), //outp
17     .JESD204B_Top_tx_data_sof_o(JESD204B_Top_tx_data_sof_o_o), //output [
18     .JESD204B_Top_tx_data_eof_o(JESD204B_Top_tx_data_eof_o_o), //output [
19     .JESD204B_Top_tx_data_somf_o(JESD204B_Top_tx_data_somf_o_o), //output

```

6 Reference Design

See JESD204B IP [reference design](#) for details at Gowinsemi website.

6.1 Applications

The JESD204B is mainly used to connect logic devices to ADCs or DACs. The following diagram describes how the FPGA connects to ADCs or DACs through four lanes using JESD204B interface.

Figure 6-1 Connection Diagram of FPGA and ADC

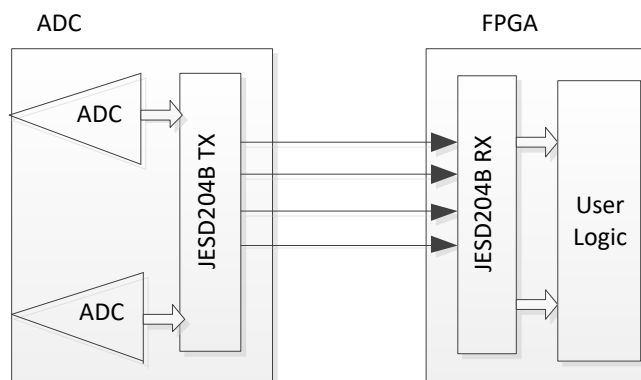
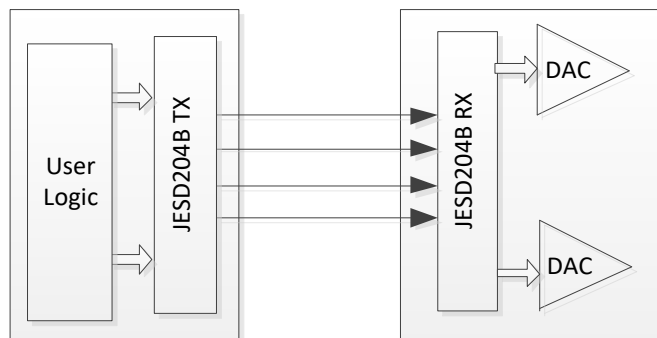


Figure 6-2 Connection Diagram of FPGA and ADC

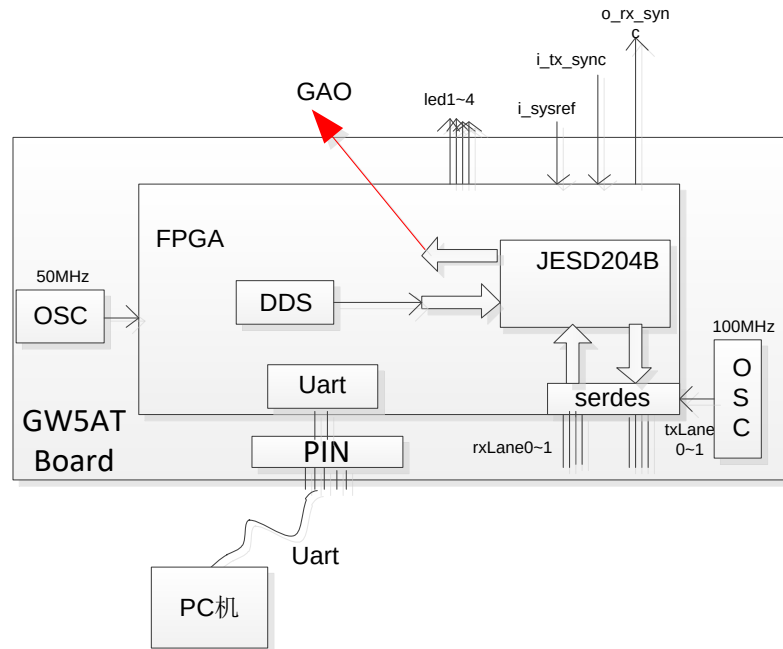


6.2 Reference Design

This chapter is intended to introduce the example and using of Gowin JESD204B IP reference design.

6.2.1 Hardware Platforms

Figure 6-3 Platforms Diagram

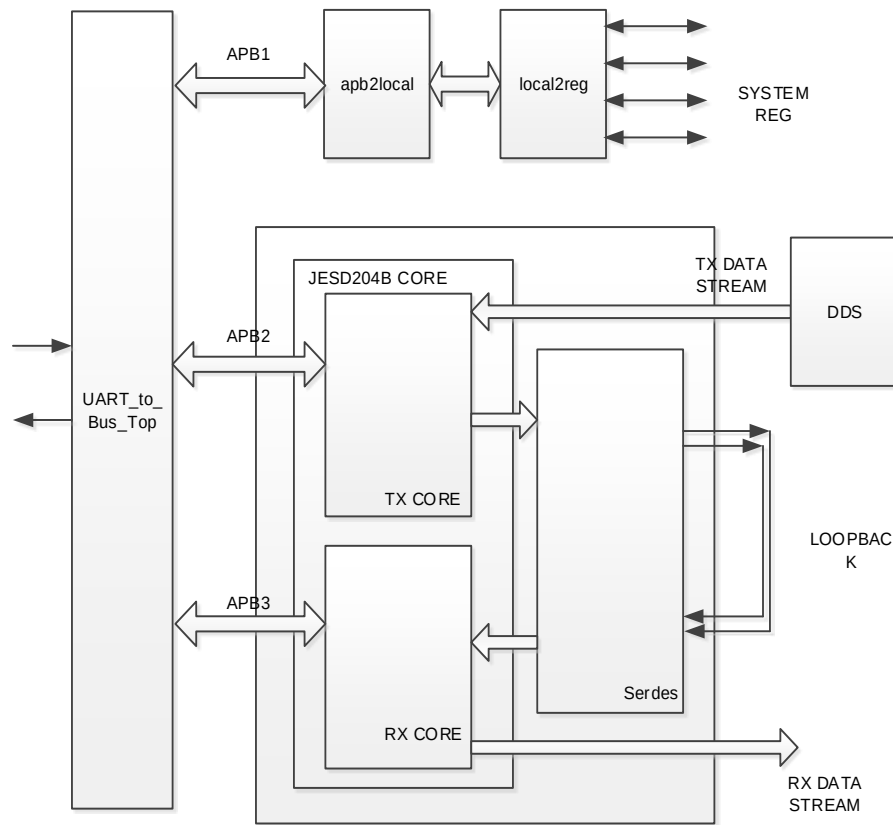


One such reference example is implemented on a GW5AT board with the following hardware conditions.

1. There is an on-board 50MHz crystal to generate the freerun clock, the bus configuration clock, SerDes AHB clock, and JESD204B core configuration clock. There is an on-board 50MHz crystal that outputs 10MHz after PLL IP for generating configuration clocks for bus configuration, SerDes AHB, and JESD204B core configuration.
2. SerDes reference clock is generated through on-board crystal with the frequency of 100MHz.
3. Connect to the serial port of the PC through a row of pins; control the internal registers in the FPGA through the serial assistant or the master.
4. Four LEDs are used to indicate the link bring-up status.
 - LED D1 - SYNC indicator received by TX core
 - LED D2 – Transmit ready indicator for TX core
 - LED D3 - SYNC indicator sent by RX core
 - LED D4 - Reception valid indicator for TX core
5. External input sysref, tx_sync and output rx_sync are supported. It is also possible to configure the internal loopback test using registers without the above 3 ports.

6.2.2 Implementation Diagram

Figure 6-4 Block Diagram of Reference Design



The **UART_to_Bus** IP module does the necessary parsing of the custom bus protocol into the APB interface, and mounts **APB1** to manage the global parameters, **APB2** to manage the **JESD204B TX CORE**, and **APB3** to manage the **JESD204B RX CORE** respectively.

The two lanes of **SerDes** are set to loopback; **TX CORE** receives the tone signal from **DDS**, loops back to **RX SerDes** interface through **TX SerDes** interface, and finally **RX CORE** receives the tone signal from **DDS**.

The main modules are as follows:

- **UART_to_Bus** IP module: Serial to bus module, converting serial commands sent by serial assistant or master into bus control timing.
- **DDS** module: Used to generate tone signal
- **Apb2local** module and **local2reg** module: Used to generate local system configuration registers.
- **JESD204B** module: The configuration of this module is shown in Figure 5-2 and Figure 5-3.

6.2.3 Bus Protocol and Address

The core of Gowin UART to Bus IP is a simple command parser that can be used to access the internal bus through the UART interface, and the custom serial bus protocol conventions are as follows:

Write bus "W AAAA BBBBBBBBB"

Read bus "R AAAA"

The read bus will return the following command "G AAAA BBBBBBBBB"

W means write, R means read, and G means read result return. They are separated by spaces, and you need to enter a carriage return at the end. AAAA means address, 16 bits; BBBBBBBBBB means data, 32 bits. For the details, see [IPUG1022, Gowin Uart to Bus IP User Guide](#)

In this reference design, UART to Bus IP parameters are set as follows:

Figure 6-5 UART to Bus IP Parameter Setting 1

Basic Slave Address

Bus Config

Bus Mode: ☒ APB ☐ Local

Address Width: 16 bits

Data Width: 32 bits

Timeout Value: 16 clocks

Uart Config

Clock Frequency: 10.000 (1.000~200.000)MHz

Baudrate Value: 115200

Generation Config

☒ Disable I/O Insertion

Figure 6-6 UART to Bus IP Parameter Setting 2

Slave Config

Slave	Base Address	High Address
☒ slave0	0x0000	0x00FF
☒ slave1	0x0100	0x01FF
☒ slave2	0x0200	0x02FF

Slave0: The address range of APB1 is 0x0000~0x00FF.

Slave1: The address range of APB2 is 0x0100~0x01FF.

Slave2: The address range of APB3 is 0x0200~0x02FF.

The detailed register address definitions in the reference project are as follows:

Table 6-1 Register Definition

Offset address	Default	W/R	Description
APB1			
0x00	0	WR	Used to verify that the serial to bus module works properly. If X is input to this register, the 0x80 register will return X+1.
0x10	0	Used to verify that the serial to bus module works properly.	SerDes PMA reset 0: Reset 1: Operating
0x11	0	Used to verify that the serial to bus module works properly.	SerDes TX PCS reset 0: Operating 1: Reset
0x12	0	Used to verify that the serial to bus module works properly.	SerDes RX PCS reset 0: Operating 1: Reset
0x13	0	Used to verify that the serial to bus module works properly.	JESD204B TX core reset 0: Reset 1: Operating
0x14	0	Used to verify that the serial to bus module works properly.	JESD204B RX core reset 0: Reset 1: Operating
0x15	0	Used to verify that the serial to bus module works properly.	Test Mode 0: Communicates with external devices 1: For loopback testing, internal sysref is used and rx_sync is connected to tx_sync.
0x16	0	Used to verify that the serial to bus module works properly.	Test Data 0: Transmits 0 1: Transmits DDS
0x8A	32'h20230406	R	Development Date
0x8B	-	R	Development Version
0x90	—	R	[0]: TX CORE sync indicator [1]: TX CORE data_ready indicator
0x91	—	R	[0]: RX CORE sync indicator [1]: RX CORE data_valid indicator
0x92	—	R	[0]: Quad0 qpll0 lock indicator [1]: Quad0 qpll1 lock indicator [2]: Quad1 qpll0 lock indicator [3]: Quad1 qpll1 lock indicator [5:4]: cpll lock indicator for each lane

Offset address	Default	W/R	Description
0x93	—	R	[1:0]: Byte alignment indicator for each RX lane [9:8]: K-code lock indicator for each TX lane
0x94	—	R	[1:0]: PMA CDR lock indicator for each RX lane
APB2 ---- is connected to the TX core bus configuration interface Note! The custom serial protocol is 4 bytes per address, while the IP core bus is 1 byte per address; pay attention to the correspondence.			
APB3 ---- is connected to the RX core bus configuration interface Note! The custom serial protocol is 4 bytes per address, while the IP core bus is 1 byte per address; pay attention to the correspondence.			

6.3 On-Board Testing

6.3.1 Operation Description

The sample project is tested on the DK_START_GW5AT-LV138FPG676A_V2.0 development board. If you don't have this board, but you want to run the reference project, you just need to modify the serial port pins and clock input pins according to the actual situation of your board for testing.

After the modification, the bit file is generated and download it to the FPGA to start testing.

6.3.2 Operation Steps

There are two ways for testing the reference design.

Using Serial Port Command

The serial port command is not only for reset control, but also for setting and monitoring the internal registers of the IP core, and the baud rate of the serial port is set to 115200.

1. After the bit file is downloaded to the FPGA, you first need to check if the serial instruction works.

Enter R 008A

Return G 008A 20230406

Then the communication between PC and FPGA is OK, otherwise, you have to check the reason why they can't communicate first before proceeding to the next step.

2. Set the parameters of TX core and RX core

Normally the main parameters can be set in the GUI, but they also can be set by entering instruction if needed; and you do not need to set in this sample project.

For example, the default F and K parameters are F=4, K=32, and you need to set F=2, K=16.

F and K parameters corresponding to the register area is 0x01C

(F_ and _K). for the corresponding serial protocol address, TX core is 0x0107, and RX core is 0x207. You can first check these two registers.

R 0107

R 0207

F and K parameters are default, and send instructions

W 0107 00000F01

W 0207 00000F01

Read back these two registers again to see if they are set correctly.

3. Check if QPLL is locked.

Enter R 0092

Return G 0092 00000008

Show that Quad1 QPLL1 is locked.

4. Set loopback mode

Send the instruction W 0015 00000001

5. SerDes PMA reset

Send the instruction W 0010 00000001

6. TX core reset

Send the instruction W 0013 00000001

7. RX core reset

Send the instruction W 0014 00000001

8. Send DDS

Send the instruction W 0016 00000001

9. Check link bring-up status

Send the instruction R 0090, R 0091

Send instructions R 0090, R 0091

If the feedback instructions

G 0090 00000003

G 0091 00000003

The return values are 3, which means that both TX and RX have been successfully linked. The command input is shown in the following figure.

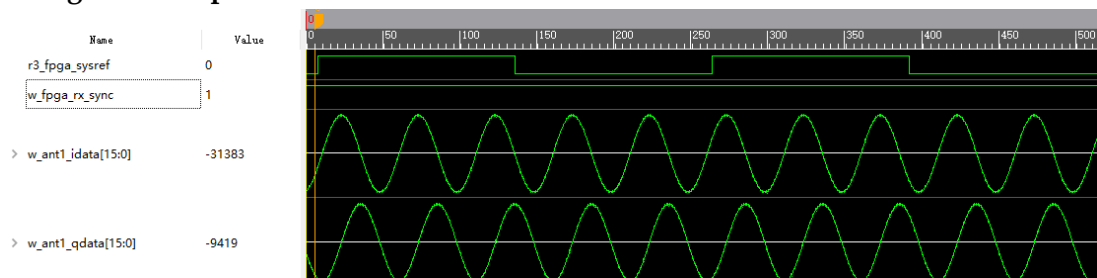
Figure 6-7 Command Input

```

COM24 - Tera Term VT
File Edit Setup Control Window Help
R 8A
G 008A 20230406
R 92
G 0092 00000008
W 0015 00000001
W 0010 00000001
W 0013 00000001
W 0014 00000001
W 0016 00000001
R 0090
G 0090 00000003
R 0091
G 0091 00000003

```

At this time, if all four indicators are on, it also means that both TX and RX have been successfully linked. The received DDS data can be captured by GAO.

Figure 6-8 Capture DDS Data

Switch Operation

If the serial port operations are not available, you can also perform a switch operation. Switch SW1 (L25) on DK_START_GW5AT-LV138FPG676A_V2.0 development board, then the internal code will automatically enter loopback mode; release SerDes PMA reset; release TX core reset; release RX core reset, and send DDS. After the switch operation, if all four indicators are on, it means that both TX and RX have brought up the link successfully, and the received DDS data can be captured through GAO.

7 File Delivery

The delivery file for Gowin JESD204B IP includes documentation, design source code, and reference design.

7.1 Documentation

The documents are listed in the below table.

Table 7-1 Documents List

Name	Description
IPUG1019, Gowin JESD204B IP User Guide	Gowin JESD204B IP User Guide, namely this one.

7.2 Design Source Code (Encryption)

The encrypted code file contains Gowin JESD204B IP RTL encrypted code which is used for GUI in order to cooperate with Gowin Software to generate the IP core required by users.

Table 7-2 Design Source Code List of Gowin JESD204B IP

Name	Description
jesd204b_core.v	The top-level file of the IP core, which provides users with interface information, encrypted.

7.3 Reference Design

The Ref. Design folder contains the netlist file, user reference design, constraints file, top-level file and the project file, etc.

Table 7-3 Gowin JESD204B IP RefDesign Folder List

Name	Description
top.v	The top module of reference design
top.cst	Project physical constraints file
top.sdc	Project timing constraints file
jesd204b.v	Generate JESD204B IP top-level file, encrypted
Serdes.v	SerDes primitives and jesd204b instantiation
Uart_to_Bus_Top.v	Serial to bus IP
Cos_sin_table.v	Sine and cosine table generation module

Name	Description
sysreg.v	SysReg generation module
Gowin_pll.v	PLL IP file

