



Gowin CPRI IP User Guide

IPUG1017-1.4E, 10/25/2024

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Revision History

Date	Version	Description
05/25/2023	1.0E	Initial version published.
07/06/2023	1.0.1E	The port name in "Table 3-1 Gowin CPRI IP Port List" of chapter 3.4 "Port List" updated.
08/18/2023	1.1E	● Resource utilization updated. ● Port list updated. ● Reference design updated.
09/08/2023	1.2E	8.11008Gbps and 10.1376Gbps added.
03/29/2024	1.3E	● 12.16512Gbps added. ● "AFE Configuration" option added. ● "Optional Ports Configuration" option added.
10/25/2024	1.4E	Descriptions of "Reference Clock Source" configuration option updated.

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1 About This Guide

1.1 Purpose

Gowin Common Public Radio Interface (CRPI) IP User Guide includes function introductions, function descriptions, interface configurations and reference designs, aiming to help you learn the features and usage of Gowin CRPI IP. The software screenshots in this manual are based on V1.9.10.03. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com.

- [SUG100, Gowin Software User Guide](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1104, GW5AST series of FPGA Products Data Sheet](#)

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
CPRI	Common Public Radio Interface
DRP	Dynamic Reconfiguration Port
FPGA	Field Programmable Gate Array
GMII	Gigabit Media Independent Interface
HDLC	High level Data Link Control
IP	Intellectual Property
IQ	In-Phase and Quadrature
MII	Medium Independent Interface
PRBS	Pseudo-Random Binary Sequence

Terminology and Abbreviations	Meaning
RE	Remote Radio Equipment
REC	Radio Equipment Control

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Function

2.1 Overview

Gowin CPRI IP implements the CPRI Specification V7.0 and high-speed serial signal transmission between Radio Equipment Control (REC) and Remote Radio Equipment (RE). The IP includes the grouping/parsing frames design and SerDes RTL design in CPRI IP specification, providing independent IQ interfaces, Ethernet interfaces, HDLC interfaces, Vendor interface and the internal frame counting interface for users.

Table 2-1 Gowin CPRI IP Overview

Gowin CPRI IP	
Logic Resource	See Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9 Beta-1 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features

The main features of the Gowin CPRI IP are as follows:

- Compliant with the CPRI Specification V7.0
- Support line bit rates: 1.2288Gbps, 2.4576Gbps, 3.072Gbps, 4.9152Gbps, 6.144Gbps, and 9.8304Gbps, 8.11008Gbps, 10.1376Gbps, 12.16512Gbps

Note!

Fixed line bit rates is supported while online negotiation to switch between multiple rates is not supported.

- Support configuration as an REC or an RE

- Support HDLC transparent transmission
- Support Ethernet transmission through GMII interface or MII interface
- Support managing configuration interfaces
- Support vendor-specific control word transmission
- Provide interfaces for reporting delay value and status

Note!

Do not support specification version negotiation, HDLC rate negotiation, Ethernet rate negotiation. You can implement these functions through managing configuration interfaces to operate registers.

2.3 Resource Utilization

Gowin CPRI IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different density, speed, or grade. Taking Gowin GW5AT series of FPGA as an instance, the resource utilization of Gowin CPRI IP is as shown in Table 2-2.

Table 2-2 Gowin CPRI IP Resource Utilization

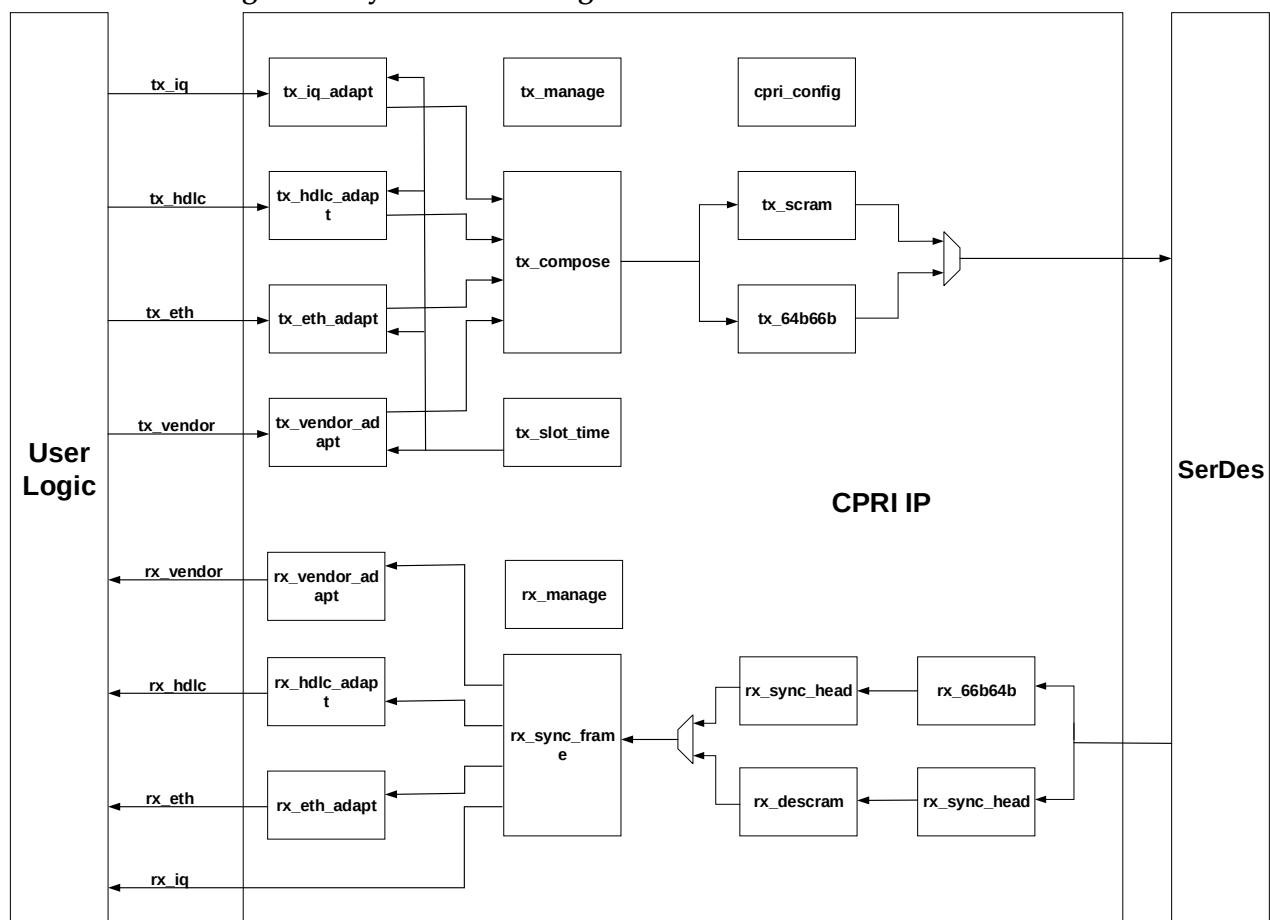
Rate (Gbps)	Fixed Config	Resource Utilization				
		Register	LUT	ALU	BSRAM	SSRAM
1.2288	Enable	1759	873	281	11	0
	Disable	1954	1042	301	11	0
2.4576	Enable	1825	882	281	11	0
	Disable	2018	1044	301	11	0
3.072	Enable	1865	905	281	11	0
	Disable	2056	1049	301	11	0
4.9152	Enable	2991	1519	288	11	0
	Disable	3341	1849	308	11	0
6.144	Enable	3063	1525	295	11	0
	Disable	3411	1858	308	11	0
9.8304	Enable	4354	2319	295	11	0
	Disable	4852	2870	308	11	0
8.11008	Enable	7077	3466	441	15	0
	Disable	7573	4050	454	15	0
10.1376	Enable	7077	3475	441	15	0
	Disable	7573	4037	454	15	0
12.16512	Enable	7154	4353	467	15	0
	Disable	7650	4889	480	15	0

3 Functional Description

3.1 System Block Diagram

Gowin CPRI IP includes a transmit direction and a receive direction. In the transmit direction, IQ, HDLC, Vendor, and Ethernet data from user input are framed, and then transmitted through SerDes; In the receive direction, the CPRI IP receives data from SerDes and parse IQ, HDLC, Vendor, and Ethernet data according to CPRI specification. The system block diagram is as shown in Figure 3-1.

Figure 3-1 System Block Diagram



3.2 Module Functions

The descriptions of Gowin CPRI IP submodules are as follows:

- tx_iq_adapt module: Used to fill CPRI frames with IQ data according to the corresponding time slots
- tx_hdlc_adapt module: Used to fill CPRI frames with HDLC data according to the corresponding time slots
- tx_eth_adapt module: Used to transmit Ethernet packets to the corresponding time slots of CPRI frame
- tx_vendor_adapt module: Used to fill CPRI frames with vendor data according to the corresponding time slots
- tx_compose module: Used to compose IQ data, HDLC data, Ethernet data, and vendor data into a CPRI frame.
- tx_manage module: Used to complete the reset and parameter configuration of other modules, such as line bit rate and HDLC rate, etc.
- tx_slot_time module: A counter used to generate time slot count, chip count, hyperframe count, 10ms-frame count, etc.
- cpri_config module: Used to maintain the register list within the CPRI IP
- tx_scram module: The scrambling module used during 8B/10B encoding. It scrambles data based on the configured scrambling seed; choose scrambling or not according to the specification version only at 4.9152G, 6.144G, and 9.8304G rates.
- tx_64b66b module: This module handles clock domain crossing, 64B/66B encoding, scrambling, and Gearbox processing during 64B/66B encoding. It is reserved for rates such as 8.11008G and 10.1376G, and is bypassed during 8B/10B encoding and decoding.
- rx_66b64b module: This module handles Gearbox processing, receive bitslip synchronization, descrambling, 66B/64B decoding, and clock domain crossing during 66B/64B decoding. It is reserved for rates such as 8.11008G and 10.1376G, and is bypassed during 8B/10B encoding and decoding.
- rx_descram module: The descrambling module used during 8B/10B decoding. It descrambles data according to the parsed seed on the receiving side; choose descrambling or not according to the specification version only at 4.9152G, 6.144G, and 9.8304G.
- rx_sync_head module: The counter used to determine if link is linked, recalibrate internal time slot/chip/hyperframe.
- rx_sync_frame module: Used to extract IQ data
- rx_manage module: Used to receive management module to complete the reset and parameter configuration of other modules, such as line bit rate and HDLC rate, etc.

- rx_hdlc_adapt module: Used to extract HDLC data from the received CPRI frame
- rx_eth_adapt module: Used to extract Ethernet packets from the received CPRI frame
- rx_vendor_adapt module: Used to extract vendor data from the received CPRI frame

3.3 User Interface

The descriptions of user-side interfaces provided by CPRI are as follows:

- I/Q Interface: I/Q data real-time transmission interface
- Frame Counting Interface: The interface that outputs the frame counts transmitted and received within CPRI
- Synchronization Interface: Supports resynchronize from the transmit side to the input 10ms frame header; supports input 10ms frame header and frame ID on the transmit side; and supports output 10ms frame header and frame ID on the receive side.
- HDLC Interface: Supports transparent transmission for HDLC transmitting and receiving
- Ethernet Interface: Supports Ethernet message transmission on MII or GMII interfaces, with internal Ethernet buffering in the CPRI IP.
- Vendor-specific Interface: Supports transmit and receive vendor-specific control words
- Real-time vendor-specific interface: When the rate is greater than or equal to 10.1376Gbps, the specification provides additional bandwidth for data transmission in addition to vendor-specific control words, IQ data, and protocol control words, etc. You can choose to transmit IQ data or custom data with additional bandwidth.
- Management Interface: Provides configuration interfaces to access the register list within the CPRI IP
- Z130_0 Protocol Control Word Interface: Supports transparent transmission for transmitting and receiving Z130.0 protocol control words
- Status Interface: Reports delay values, synchronization status, etc.
- SerDes Interfaces: Includes clock, reset, etc.

3.4 Port List

The ports of Gowin CPRI IP are shown in Figure 3-2.

Figure 3-2 Gowin CPRI IP Port Diagram

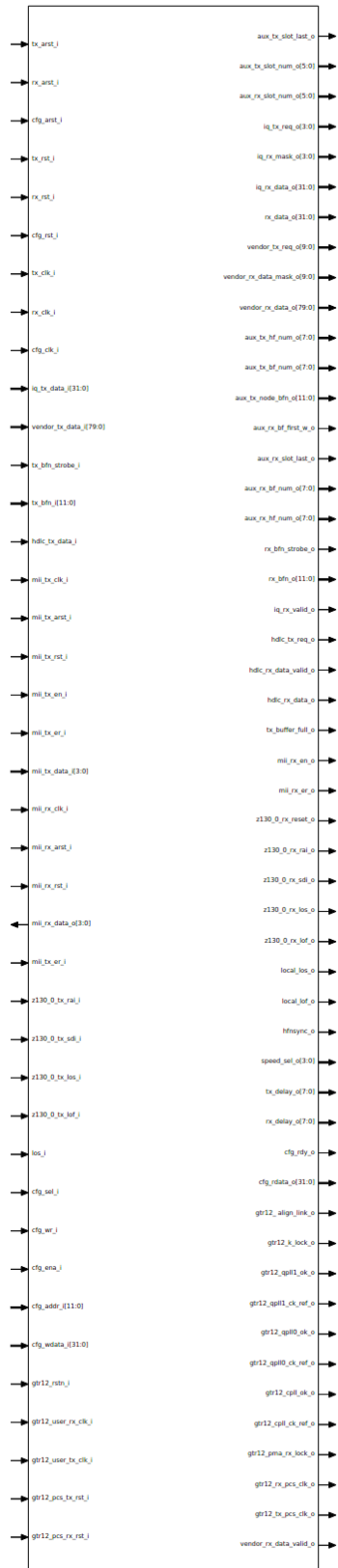


Table 3-1 Gowin CPRI IP Port List

Port Name	I/O	Data Width	Description
Clock and Reset			
tx_arst_i	input	1	Asynchronous reset signal in transmit direction, active-high
rx_arst_i	input	1	Asynchronous reset signal in receive direction, active-high
cfg_arst_i	input	1	Asynchronous reset signal of configuration module, active-high
tx_rst_i	input	1	Synchronous reset signal in transmit direction, active-high
rx_rst_i	input	1	Synchronous reset signal in receive direction, active-high
cfg_rst_i	input	1	Synchronous reset signal of configuration module, active-high
tx_clk_i	input	1	The frequency of CPRI IP clock in transmit direction varies with the rate. ● 1.2288G, 61.44M ● 2.4576G, 122.88M ● 3.072G, 153.6M ● 4.9152G, 122.88M ● 6.144G, 153.6M ● 9.8304G, 122.88M ● 8.11008G, 122.88M ● 10.1376G, 153.6M ● 12.16512G, 184.32M
rx_clk_i	input	1	The frequency of CPRI IP clock in receive direction is the same as the frequency of tx_clk_i.
cfg_clk_i	input	1	You can enter the frequency of configuration clock via "Config clk Period" option.
Frame Counting Interface			
aux_tx_slot_last_o	output	1	Transmitting frame count, active-high, indicates the last time slot of each chip.
aux_tx_slot_num_o	output	[N-1:0]	Transmitting frame count, time slot counter: ● 1.2288G, 0~15 cycle counting ● 2.4576G, 0~31 cycle counting ● 3.072G, 0~39 cycle counting ● 4.9152G, 0~31 cycle counting ● 6.144G, 0~39 cycle counting ● 9.8304G, 0~31 cycle counting ● 8.11008G, 0~31 cycle counting ● 10.1376G, 0~39 cycle counting ● 12.16512G, 0~47 cycle counting
aux_tx_bf_num_o	output	[7:0]	Transmitting frame count, chip counter 0~255

Port Name	I/O	Data Width	Description
aux_tx_hf_num_o	output	[7:0]	Transmitting frame count, hyperframe counter 0~149
aux_tx_node_bfn_o	output	[11:0]	Transmitting frame count, 10ms frame No.
aux_rx_bf_first_w_o	output	1	Receiving frame count, active-high, indicates the first time slot of each chip.
aux_rx_slot_last_o	output	1	Receiving frame count, active-high, indicates the last time slot of each chip.
aux_rx_slot_num_o	output	[N-1:0]	Receiving frame count, time slot counter: ● 1.2288G, 0~15 cycle counting ● 2.4576G, 0~31 cycle counting ● 3.072G, 0~39 cycle counting ● 4.9152G, 0~31 cycle counting ● 6.144G, 0~39 cycle counting ● 9.8304G, 0~31 cycle counting ● 8.11008G, 0~31 cycle counting ● 10.1376G, 0~39 cycle counting ● 12.16512G, 0~47 cycle counting
aux_rx_bf_num_o	output	[7:0]	Receiving frame count, chip counter 0~255
aux_rx_hf_num_o	output	[7:0]	Receiving frame count, hyperframe counter 0~149
Frame Synchronization Signal			
tx_bfn_strobe_i	input	1	Transmitting frame start signal, active-high, to calibrate the time slot on the transmit side
tx_bfn_i	input	[11:0]	Transmitting 10ms frame No.
rx_bfn_strobe_o	output	1	Receiving frame start signal, active-high, indicates the starting point of 10ms frames.
rx_bfn_o	output	[11:0]	Receiving 10ms frame No.
IQ Interface			
iq_tx_req_o	output	[N-1:0]	Transmitting IQ data request signal, active-high ● 1.2288G, [1:0] valid ● 2.4576G, [1:0] valid ● 3.072G, [1:0] valid ● 4.9152G, [3:0] valid ● 6.144G, [3:0] valid ● 9.8304G, [7:0] valid ● 8.11008G, [7:0] valid ● 10.1376G, [7:0] valid ● 12.16512G, [7:0] valid
iq_tx_data_i	input	[N-1:0]	Transmit IQ data When iq_tx_req_o is valid, the data

Port Name	I/O	Data Width	Description
			iq_tx_data_i is input to this interface one clock cycle delayed than iq_tx_req_o. ● 1.2288G, [15:0] valid ● 2.4576G, [15:0] valid ● 3.072G, [15:0] valid ● 4.9152G, [31:0] valid ● 6.144G, [31:0] valid ● 9.8304G, [63:0] valid ● 8.11008G, [63:0] valid ● 10.1376G, [63:0] valid ● 12.16512G, [63:0] valid
iq_rx_valid_o	output	1	Receive IQ data valid signal, active-high
iq_rx_mask_o	output	[N-1:0]	Receive byte indicator Note! Meaningful only when iq_rx_valid_o is valid. The bit width is the same as iq_tx_req_o.
iq_rx_data_o	output	[N-1:0]	IQ data received The bit width is the same as iq_tx_data_i.
rx_data_o	output	[N-1:0]	CPRI data received The bit width is the same as iq_tx_data_i.
HDLC Interface			
hdlc_tx_req_o	output	1	Transmitting HDLC request signal, active-high
hdlc_tx_data_i	input	1	When hdlc_tx_req_o is valid, HDLC data hdlc_tx_data_i is input to this interface one clock cycle delayed than hdlc_tx_req_o.
hdlc_rx_data_valid_o	output	1	High: Indicates HDLC data is high
hdlc_rx_data_o	output	1	HDLC data received
Ethernet MII Interface (Either MII Interface or GMII Interface)			
mii_tx_clk_i	input	1	Transmit direction, Ethernet interface clock, 25MHz
mii_tx_arst_i	input	1	Transmit direction, Ethernet interface asynchronous reset
mii_tx_rst_i	input	1	Transmit direction, Ethernet interface synchronous reset
mii_tx_en_i	input	1	Transmit direction, Ethernet interface enable, active-high
mii_tx_er_i	input	1	Transmit direction, Ethernet interface error indication, active-high When mii_tx_en_i is valid, mii_tx_er_i should be determined.

Port Name	I/O	Data Width	Description
mii_tx_data_i	input	[3:0]	Transmit direction, Ethernet data
tx_buffer_full_o	output	1	Transmit direction, indicate that the transmit buffer is full therefore cannot buffer new packets, active-high
mii_rx_clk_i	input	1	Receive direction, Ethernet interface clock, 25MHz
mii_rx_arst_i	input	1	Receive direction, Ethernet interface asynchronous reset
mii_rx_rst_i	input	1	Receive direction, Ethernet interface synchronous reset
mii_rx_en_o	output	1	Receive direction, Ethernet interface enable, active-high
mii_rx_data_o	output	[3:0]	Receive direction, Ethernet data
mii_rx_er_o	output	1	Receive direction, Ethernet interface error indication, active-high When mii_rx_en_o is valid, mii_rx_er_o should be determined.
Ethernet GMII interface (Either MII Interface or GMII Interface)			
gmii_tx_clk_i	input	1	Transmit direction, Ethernet interface clock, 125MHz
gmii_tx_arst_i	input	1	Transmit direction, Ethernet interface asynchronous reset
gmii_tx_rst_i	input	1	Transmit direction, Ethernet interface synchronous reset
gmii_tx_en_i	input	1	Transmit direction, Ethernet interface enable, active-high
gmii_tx_er_i	input	1	Transmit direction, Ethernet interface error indication, active-high When gmii_tx_en_i is valid, gmii_tx_er_i should be determined.
gmii_tx_data_i	input	[7:0]	Transmit direction, Ethernet data
gmii_tx_buffer_full_o	output	1	Transmit direction, indicating that the transmit buffer is full therefore cannot buffer new packets, active-high
gmii_rx_clk_i	input	1	Receive direction, Ethernet interface clock, 125MHz
gmii_rx_arst_i	input	1	Receive direction, Ethernet interface asynchronous reset
gmii_rx_rst_i	input	1	Receive direction, Ethernet interface synchronous reset
gmii_rx_en_o	output	1	Receive direction, Ethernet interface enable, active-high
gmii_rx_data_o	output	[7:0]	Receive direction, Ethernet data
gmii_rx_er_o	output	1	Receive direction, Ethernet interface error indication, active-high When gmii_rx_en_o is valid, gmii_rx_er_o should be determined.
Vendor-specific Control Word Interface			

Port Name	I/O	Data Width	Description
vendor_tx_req_o	output	[N-1:0]	Transmit direction, vendor-specific data request, active-high ● 1.2288G, [1:0] valid ● 2.4576G, [3:0] valid ● 3.072G, [4:0] valid ● 4.9152G, [7:0] valid ● 6.144G, [9:0] valid ● 9.8304G, [15:0] valid ● 8.11008G, [15:0] valid ● 10.1376G, [15:0] valid ● 12.16512G, [15:0] valid
vendor_tx_data_i	input	[N-1:0]	Transmit direction, vendor-specific control word When vendor_tx_req_o is valid, vendor-specific control word data vendor_tx_data_i is input to this interface one clock cycle delayed than vendor_tx_req_o. ● 1.2288G, [15:0] valid ● 2.4576G, [31:0] valid ● 3.072G, [39:0] valid ● 4.9152G, [63:0] valid ● 6.144G, [79:0] valid ● 9.8304G, [127:0] valid ● 8.11008G, [127:0] valid ● 10.1376G, [127:0] valid ● 12.16512G, [127:0] valid
vendor_rx_data_valid_o	output	1	Receive direction, active-high, indicating that vendor data is valid
vendor_rx_data_mask_o	output	[N-1:0]	Receive direction, vendor-specific control word byte pointer The bit width is the same as vendor_tx_req_o.
vendor_rx_data_o	output	[N-1:0]	Receive direction, vendor data received The bit width is the same as vendor_tx_data_i.
Real-time Vendor-specific Control Word Interface			
up10g_rt_tx_req_o	output	[7:0]	Transmit direction, real-time vendor-specific control data request, active-high
up10g_rt_tx_data_i	input	[63:0]	Transmit direction, real-time vendor-specific control data
up10g_rt_rx_data_o	output	[63:0]	Receive direction, real-time vendor-specific control data
up10g_rt_rx_mask_o	output	[7:0]	Receive direction, real-time vendor-specific control word byte pointer
up10g_rt_rx_valid_o	output	1	Receive direction, active-high,

Port Name	I/O	Data Width	Description
			indicating that the data is valid.
Protocol Control Word Interface			
z130_0_tx_reset_i	input	1	Transmit Direction, Z.130.0 protocol control word Reset 0: No reset 1: Reset DL: Reset request UL: Reset acknowledge
z130_0_tx_rai_i	input	1	Transmit direction, Z.130.0 protocol control word RAI
z130_0_tx_sdi_i	input	1	Transmit direction, Z.130.0 protocol control word SDI
z130_0_tx_los_i	input	1	Transmit direction, Z.130.0 protocol control word LOS
z130_0_tx_lof_i	input	1	Transmit direction, Z.130.0 protocol control word LOF
z130_0_rx_reset_o	output	1	Receive direction, Z.130.0 protocol control word Reset 0: No reset 1: Reset DL: Reset request UL: Reset acknowledge
z130_0_rx_rai_o	output	1	Receive direction, Z.130.0 protocol control word RAI
z130_0_rx_sdi_o	output	1	Receive direction, Z.130.0 protocol control word SDI
z130_0_rx_los_o	output	1	Receive direction, Z.130.0 protocol control word LOS
z130_0_rx_lof_o	output	1	Receive direction, Z.130.0 protocol control word LOF
Status Port			
local_los_o	output	1	Local LOS state
local_lof_o	output	1	Local LOF state
hfnsync_o	output	1	Local hyperframe number synchronization status
speed_sel_o	output	[3:0]	Current line bit rate within IP Fixed line bit rates is supported while online negotiation to switch between multiple rates is not supported. ● 1.2288G, 4'd1 ● 2.4576G, 4'd2 ● 3.072G, 4'd3 ● 4.9152G, 4'd4 ● 6.144G, 4'd5 ● 9.8304G, 4'd6 ● 8.11008G, 4'd8 ● 10.1376G, 4'd9

Port Name	I/O	Data Width	Description
			12.16512G, 4'd10
tx_delay_o	output	[7:0]	Processing delay in IP transmit direction, excluding SerDes
rx_delay_o	output	[7:0]	Processing delay in IP receive direction, excluding SerDes
los_i	input	1	Active-high, indicating that optical signal is lost
Configuration Interface			
cfg_sel_i	input	1	Chip select enable signal
cfg_wr_i	input	1	Write control signal High: Indicates that current operation is a write operation
cfg_ena_i	input	1	Transmission enable signal High: Indicates that current transmission is valid
cfg_addr_i	input	[11:0]	Address line, byte address
cfg_wdata_i	input	[31:0]	Write data bus
cfg_rdy_o	output	1	Ready signal
cfg_rdata_o	output	[31:0]	Read data bus
User-side SerDes-control Interface			
gtr12_rstn_i	input	1	SerDes lane reset signal, active-low Only reset the single lane corresponding to the protocol.
gtr12_pcs_tx_rst_i	input	1	SerDes PCS layer transmit direction reset, active-high
gtr12_pcs_rx_rst_i	input	1	SerDes PCS layer receive direction reset, active-high
gtr12_user_rx_clk_i	input	1	SerDes user-side receiving clock, and the clock frequency is related to the rate 1.2288G, 61.44M 2.4576G, 122.88M 3.072G, 153.6M 4.9152G, 122.88M 6.144G, 153.6M 9.8304G, 122.88M 8.11008G, 126.72M 10.1376G, 158.4M 12.16512G, 190.08M
gtr12_user_tx_clk_i	input	1	SerDes user-side transmitting clock, and the clock frequency is related to the rate 1.2288G, 61.44M 2.4576G, 122.88M 3.072G, 153.6M 4.9152G, 122.88M 6.144G, 153.6M

Port Name	I/O	Data Width	Description
			● 9.8304G, 122.88M ● 8.11008G, 126.72M ● 10.1376G, 158.4M ● 12.16512G, 190.08M
gtr12_align_link_o	output	1	SerDes lane alignment status High: Indicates link is in normal operation
gtr12_k_lock_o	output	1	SerDes lane Comma Character lock status High: Indicates link is in normal operation
gtr12_pll_ok_o	output	1	SerDes PLL lock status; High, indicates clock lock; This corresponds to the PLL lock status selected in the configuration interface using the PLL_Selection option (QPLL0, QPLL1, or CPLL).
gtr12_pll_ck_ref_o	output	1	SerDes PLL reference clock
gtr12_pma_rx_lock_o	output	1	SerDes lane receive PMA layer lock status High: Indicates link is in normal operation
gtr12_rx_pcs_clk_o	output	1	SerDes lane PCS receiving clock, which can be output to external Phase-locked Loop as a reference clock on the slave side ● 1.2288G, 61.44M ● 2.4576G, 122.88M ● 3.072G, 153.6M ● 4.9152G, 122.88M ● 6.144G, 153.6M ● 9.8304G, 122.88M ● 8.11008G, 126.72M ● 10.1376G, 158.4M ● 12.16512G, 190.08M
gtr12_tx_pcs_clk_o	output	1	SerDes lane PCS transmitting clock ● 1.2288G, 61.44M ● 2.4576G, 122.88M ● 3.072G, 153.6M ● 4.9152G, 122.88M ● 6.144G, 153.6M ● 9.8304G, 122.88M ● 8.11008G, 126.72M ● 10.1376G, 158.4M ● 12.16512G, 190.08M
gtr12_rx_fifo_rdusewd_o	output	[4:0]	The distance between the read and write pointers of the GearFIFO in the SerDes RX direction, used for delay value calculation.

Port Name	I/O	Data Width	Description
gtr12_tx_fifo_wrusewd_o	output	[4:0]	The distance between the read and write pointers of the GearFIFO in the SerDes TX direction, used for delay value calculation.
SerDes Hard Core Interface			
SerDes_*	–	–	The signals starting with "SerDes_" are CPRI IP and SerDes hard connection signals. EDA tools automatically complete the wiring, so you can leave them alone.
SerDes Configuration Interface			
loopback_en_i	input	1	SerDes loopback enable; when set to high, the loopback_mode_i data is valid. The corresponding clock domain is user_drp_clk_o.
loopback_mode_i	input	[1:0]	SerDes loopback mode selection, with the corresponding clock domain as user_drp_clk_o: ● 2'b00, Normal mode ● 2'b01, SerDes PMA layer internal loopback ● 2'b10, SerDes PMA layer external loopback
user_drp_clk_o	output	1	DRP (Dynamic Reconfiguration Port) bus, used for configuring SerDes internal registers; DRP interface clock signal.
user_drp_ready_o	output	1	DRP bus, used for configuring SerDes internal registers; write handshake signal for DRP interface, active-high.
user_drp_rdvld_o	output	1	DRP bus, used for configuring SerDes internal registers; read data valid signal for DRP interface, active-high.
user_drp_rddata_o	output	[31:0]	DRP bus, used for configuring SerDes internal registers; read data signal for DRP interface.
user_drp_resp_o	output	1	DRP bus, used for configuring SerDes internal registers; current read/write operation invalid signal for DRP interface, reserved.
user_drp_addr_i	input	[23:0]	DRP bus, used for configuring SerDes internal registers; read/write address signal for DRP interface.
user_drp_wren_i	input	1	DRP bus, used for configuring SerDes internal registers; write request signal for DRP interface, active-high.
user_drp_wrdata_i	input	[31:0]	DRP bus, used for configuring

Port Name	I/O	Data Width	Description
			SerDes internal registers; write data signal for DRP interface.
user_drp_strb_i	input	[7:0]	DRP bus, used for configuring SerDes internal registers; write mask signal for DRP interface, with all to high level.
user_drp_rden_i	input	1	DRP bus, used for configuring SerDes internal registers; read request signal for DRP interface, active-high.

3.5 User Interface Timing

3.5.1 Frame Counting Interface Timing Diagram

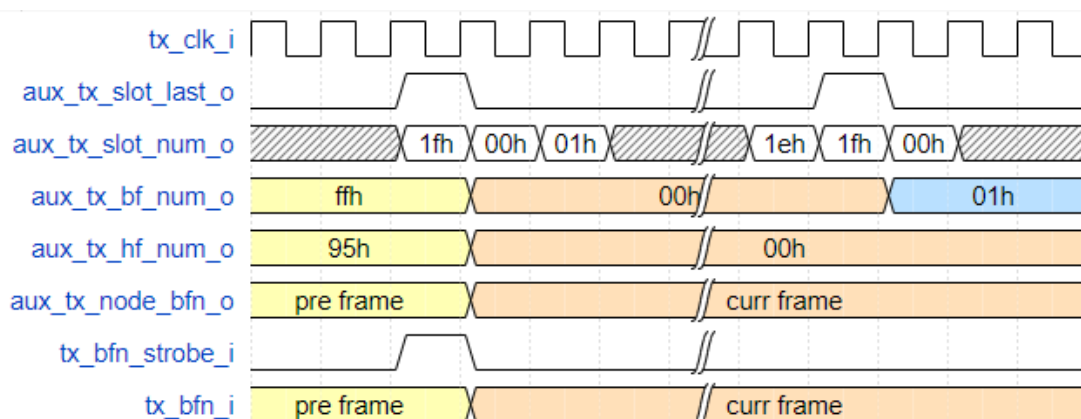
Gowin CPRI IP internally maintains a set of transmitting and receiving frame counts. You can obtain the transmitting and receiving statistics within the IP via the frame counting interface.

The frame counting timing in the transmit direction is shown in Figure 3-3. Aux_tx_slot_last_o is the end of each basic frame.

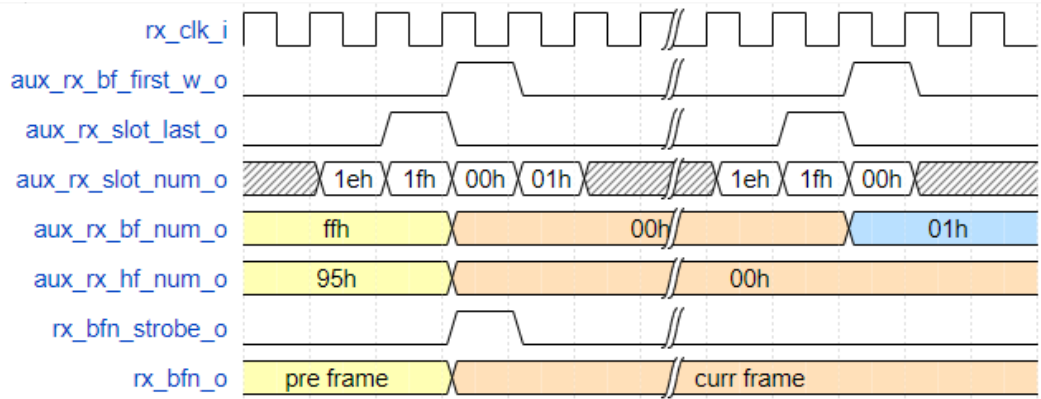
Aux_tx_slot_num_o, aux_tx_bf_num_o, and aux_tx_hf_num_o count in cycles according to the frame format specified by the CPRI specification. Every 10ms is a radio frame. Add 1 to aux_tx_node_bfn_o at the end of each radio frame.

The transmit direction supports calibration of internal frame counting statistics according to the frame ID (tx_bfn_i) and frame start (tx_bfn_strobe_i) input from the user side. If you have need for this function, you can set the frame start to 0, and the IP works according to the internal timing counter.

Figure 3-3 Timing Diagram of Frame Counting Interface in Transmit Direction



The frame counting timing in receive direction is shown in Figure 3-3. Aux_rx_bf_first_w_o is the start of each basic frame. Aux_rx_slot_last_o is the end of each basic frame. Aux_rx_slot_num_o, aux_rx_bf_num_o, and aux_rx_hf_num_o counts in cycles according to the frame format specified by the CPRI specification. Every 10ms is a radio frame. Rx_bfn_strobe_o indicates frame start. Add 1 to rx_bfn_o at the end of each radio frame.

Figure 3-4 Timing Diagram of Frame Counting Interface in Receive Direction

CPRI IP counts in cycles according to the frame format. The counting range of slot_num is linked to the rate, as listed below. The counting range of bf_num is 0~255, the counting range of hf_num is 0~149, and the counting range of bfn radio frame number is 0~1023.

- 1.2288G, slot_num 0~15 cycle counting
- 2.4576G, slot_num 0~31 cycle counting
- 3.072G, slot_num 0~39 cycle counting
- 4.9152G, slot_num 0~31 cycle counting
- 6.144G, slot_num 0~39 cycle counting
- 9.8304G, slot_num 0~31 cycle counting
- 8.11008G, slot_num 0~31 cycle counting
- 10.1376G, slot_num 0~39 cycle counting
- 12.16512G, slot_num 0~47 cycle counting

3.5.2 IQ Interface Timing Diagram

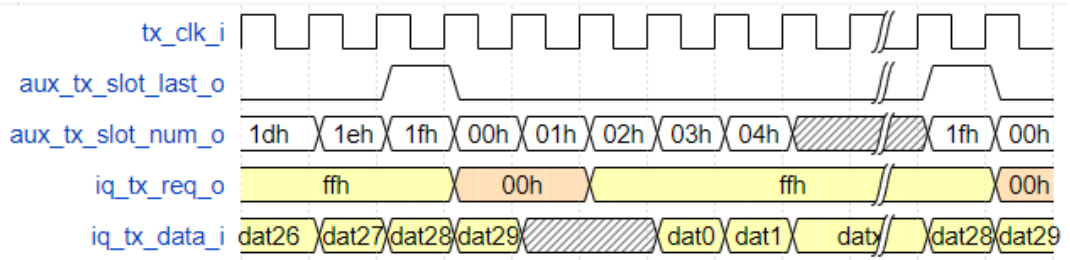
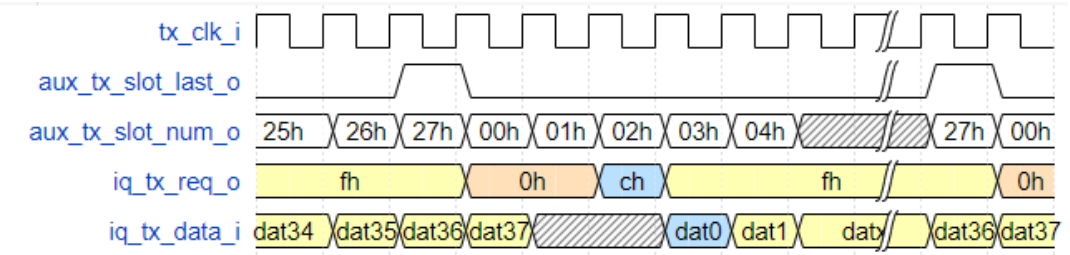
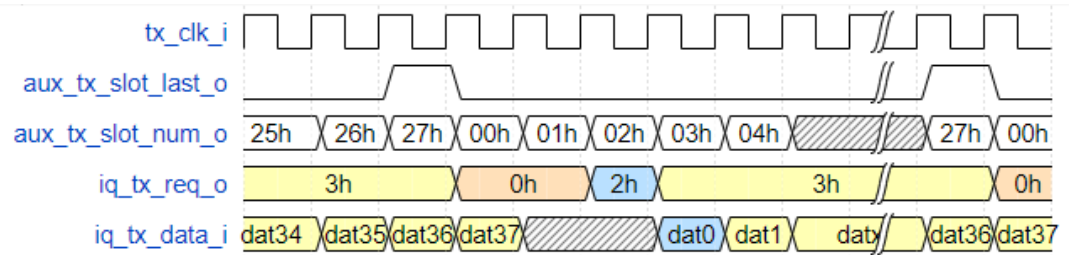
The IQ interface is used to transmit I/Q data in real time.

The I/Q interface in transmit direction at 9.8304Gbps line bit rate is shown in Figure 3-5. Iq_tx_data_i is used to transmit IQ data. The bit width is 64 bits. Iq_tx_req_o is transmitting IQ request signal and is transmitted one clock cycle in advance than iq_tx_data_i. The bit width of Iq_tx_req_o is 8 bits. Each bit of iq_tx_req_o corresponds to a byte of iq_tx_data_i. For example, bit0 of iq_tx_req_o is high for request data [7:0], bit1 of iq_tx_req_o is high for request data [15:8], and so on. Each bit of iq_tx_req_o is active-high.

Except for 9.8304G, the timing of other rates is similar to that of 9.8304G, and the difference only lies in the different frame structure, as listed below.

- 1.2288G, the bit width of iq_tx_data_i is 16 bits, and the bit width of iq_tx_req_o is 2 bits. iq_tx_req_o is 2'b00 when slot_num is 0 (request data [15:0] is invalid); iq_tx_req_o is 2'b11 when slot_num is 1~15 (request data [15:0] is valid).

- 2.4576G, the bit width of iq_tx_data_i is 16 bits, and the bit width of iq_tx_req_o is 2 bits. iq_tx_req_o is 2'b00 when slot_num is 0~1 (request data [15:0] is invalid), iq_tx_req_o is 2'b11 when slot_num is 2~31 (request data [15:0] is valid).
- 3.072G, the bit width of iq_tx_data_i is 16 bits, and the bit width of iq_tx_req_o is 2 bits. iq_tx_req_o is 2'b00 when slot_num is 0~1 (request data [15:0] is invalid), iq_tx_req_o is 2'b10 when slot_num is 2 (request data [15:8] is valid, request data [7:0] is invalid), iq_tx_req_o is 2'b11 when slot_num is 3~39 (request data [15:0] is valid).
- 4.9152G, the bit width of iq_tx_data_i is 32bit, and the bit width of iq_tx_req_o is 4bit. iq_tx_req_o is 4'b0000 when slot_num is 0~1 (request data [31:0] is invalid), iq_tx_req_o is 4'b1111 when slot_num is 2~31 (request data [31:0] is valid).
- 6.144G, the bit width of iq_tx_data_i is 32bit, and the bit width of iq_tx_req_o is 4bit. iq_tx_req_o is 4'b0000 when slot_num is 0~1 (request data [31:0] is invalid), iq_tx_req_o is 4'b1100 when slot_num is 2 (request data [31:16] is valid, request data [15:0] is invalid), iq_tx_req_o is 4'b1111 when slot_num is 3~39 (request data [31:0] is valid).
- 9.8304G, the bit width of iq_tx_data_i is 64bit, and the bit width of iq_tx_req_o is 8bit. iq_tx_req_o is 8'b00000000 when slot_num is 0~1 (request data [63:0] is invalid), iq_tx_req_o is 8'b11111111 when slot_num is 2~31 (request data [63:0] is valid).
- 8.11008G, the bit width of iq_tx_data_i is 64bit, and the bit width of iq_tx_req_o is 8bit. iq_tx_req_o is 8'b00000000 (request data [63:0] is invalid) when slot_num is 0~1, and iq_tx_req_o is 8'b11111111 (request data [63:0] is valid) when slot_num is 2~31. req_o is 8'b11111111 (request data [63:0] is valid).
- 10.1376G, the bit width of iq_tx_data_i is 64bit, and the bit width of iq_tx_req_o is 8bit. If "Real Time Vendor" is checked on the GUI, iq_tx_req_o is 8'b00000000 (request data [63:0] is invalid) when slot_num is 0~1; iq_tx_req_o is 8'b11110000 (request data [63:32] is valid) when slot_num is 2; iq_tx_req_o is 8'b11111111 (request data [63:0] is valid) when slot_num is 3~39. If "Real Time Vendor" is unchecked on the GUI, iq_tx_req_o is 8'b00000000 (request data [63:0] is invalid) when slot_num is 0~1; iq_tx_req_o is 8'b11111111 (request data [63:0] is valid) when slot_num 2~39.
- 12.16512G, the bit width of iq_tx_data_i is 64bit, and the bit width of iq_tx_req_o is 8bit. If "Real Time Vendor" is checked on the GUI, iq_tx_req_o is 8'b00000000 (request data [63:0] is invalid) when slot_num 0~2, and iq_tx_req_o is 8'b11111111 (request data [63:0] is valid) when slot_num 3~47. If "Real Time Vendor" is unchecked on the GUI, iq_tx_req_o is 8'b00000000 (request data [63:0] is invalid) when slot_num is 0~1, and iq_tx_req_o is 8'b11111111 (request data [63:0] is valid) when slot_num is 2~47.

Figure 3-5 9.8304Gbps I/Q Interface in Transmit Direction**Figure 3-6 6.144Gbps I/Q Interface in Transmit Direction****Figure 3-7 3.072Gbps I/Q Interface in Transmit Direction**

The I/Q interface in receive direction at 9.8304Gbps line bit rate is shown in Figure 3-8. Iq_rx_valid_o indicates data is valid, active-high. Iq_rx_mask_o indicates receive data byte is valid, active-high. Iq_rx_data_o indicates the IQ data received. Rx_data_o indicates the CPRI data received, including control words in addition to IQ data. You can enable or disable as required.

Except for 9.8304G, the receiving timing of other rates is similar to that of 9.8304G, and the difference only lies in the different frame structure. The frame structure can be described with reference to the transmit timing.

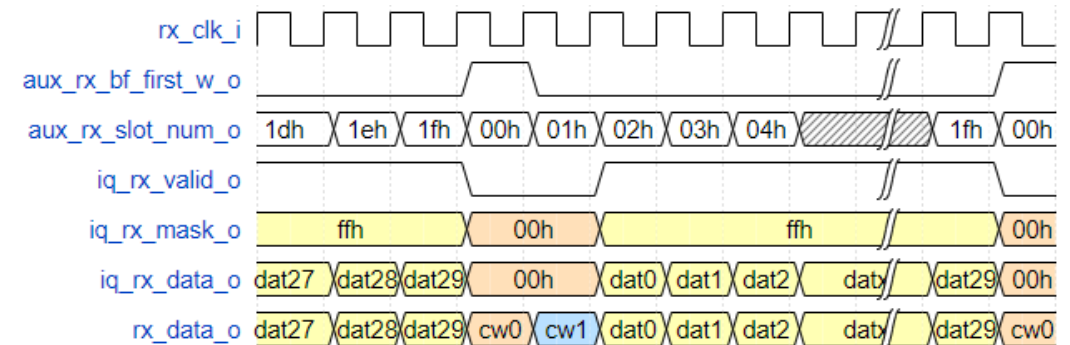
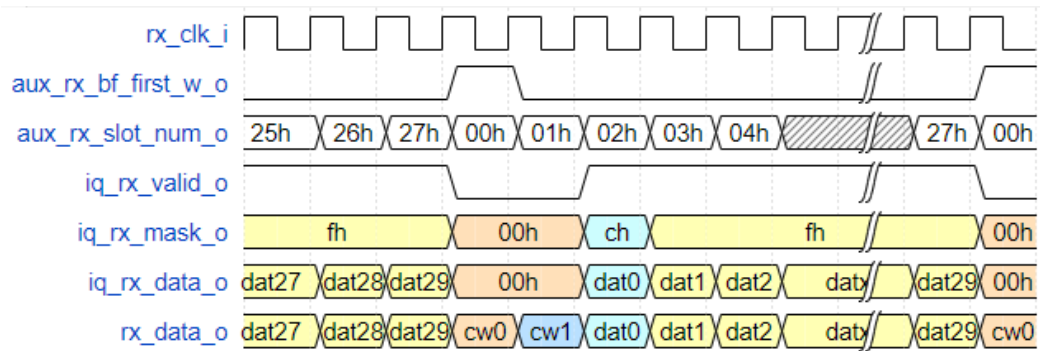
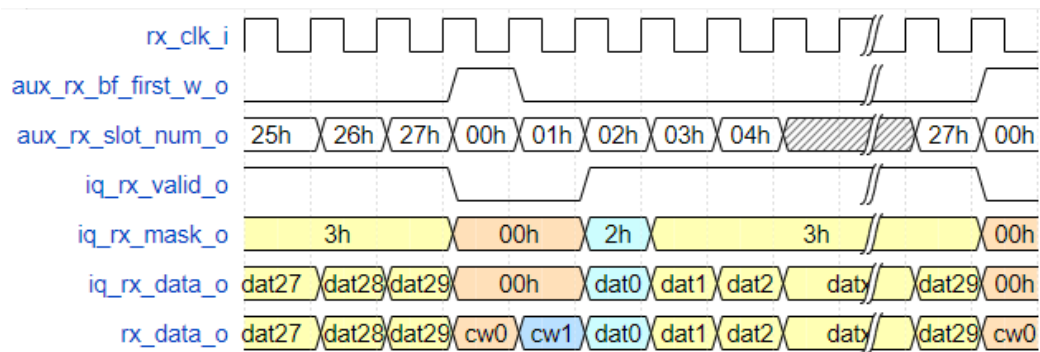
Figure 3-8 9.8304Gbps I/Q Interface in Receive Direction

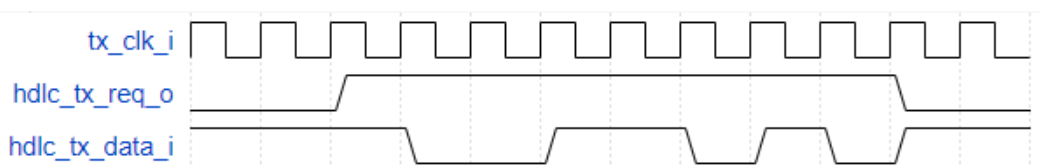
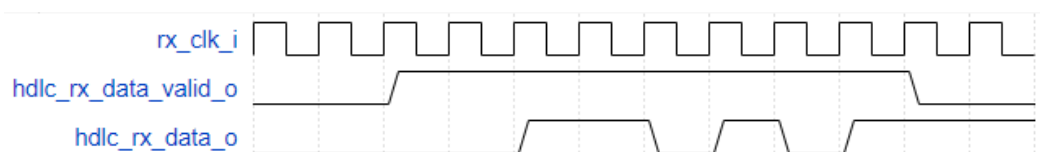
Figure 3-9 6.144Gbps I/Q Interface in Receive Direction**Figure 3-10 3.072Gbps I/Q Interface in Receive Direction**

3.5.3 HDLC Interface Timing Diagram

HDLC supports transparent transmission in transmit and receive directions of single-bit HDLC data.

The timing of interface in transmit direction is shown in Figure 3-11. hdlc_tx_req_o is transmitted one clock cycle in advance than hdlc_tx_data_i.

The timing of interface in receive direction is shown in Figure 3-12. hdlc_rx_data_valid_o is active-high when hdlc_rx_data_o is valid.

Figure 3-11 HDLC Transmitting Interface Timing Diagram**Figure 3-12 HDLC Receiving Interface Timing Diagram**

3.5.4 Ethernet Interface Timing Diagram

CPRI IP supports the transmitting and receiving of Ethernet messages. You can transmit Ethernet messages using MII interface or GMII interface. CPRI IP includes Ethernet buffer, and 4 Ethernet messages are buffered by default. You can select MII interface or GMII interface in the GUI, either one or the other.

The timing of interface in transmit direction is as shown in Figure 3-13. After `mii_tx_en_i` is pulled high, input a packet of full Ethernet packet data. And `tx_buffer_full_o` indicates the full status of current buffer during the IDLE time between the end of each packet transmission and the start of next packet transmission. Before you are ready to start transmitting the next packet, you need to determine the status of `tx_buffer_full_o`. If it is low, you can transmit a full Ethernet message; if it is high, you need to wait for `tx_buffer_full_o` to be low before transmitting a full Ethernet message.

The timing of interface in receive direction is shown in Figure 3-14. `mii_rx_en_i` indicates receiving frame is valid, `mii_rx_data_o` is receiving data.

Figure 3-13 Ethernet Transmitting Interface Timing Diagram

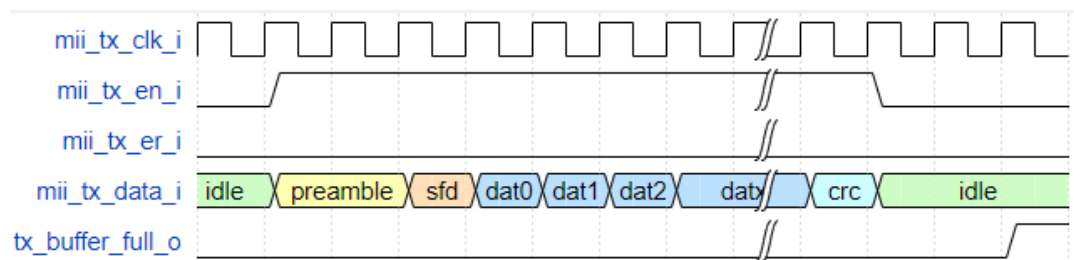
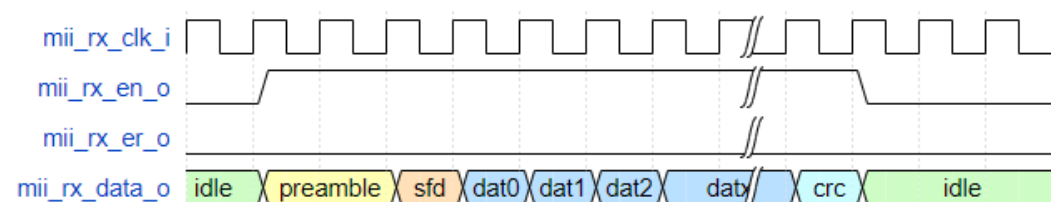


Figure 3-14 Ethernet Receiving Interface Timing Diagram



3.5.5 Vendor Interface Timing Diagram

The Vendor interface supports transmitting and receiving vendor-specific control words.

The transmitting interfaces are shown in Figure 3-15. When `aux_tx_bf_num_o[4:0]` is 5'h10, 5'h11, 5'h12, 5'h13, the control word is vendor-specific control word. `Vendor_tx_req_o` indicates transmitting vendor-specific control word request signal. If each bit is high, it indicates that a vendor-specific control word corresponding to the byte is requested. `Vendor_tx_data_i` indicates inputting vendor-specific control word data by users. `Vendor_tx_req_o` is valid one clock cycle in advance than `vendor_tx_data_i`. Vendor-specific bit widths vary at different speeds:

- 1.2288G, `vendor_tx_data_i[15:0]` is valid, and `vendor_tx_req_o[1:0]` is

valid.

- 2.4576G, vendor_tx_data_i [31:0] is valid, and vendor_tx_req_o[3:0] is valid.
- 3.072G, vendor_tx_data_i [39:0] is valid, and vendor_tx_req_o[4:0] is valid;
- 4.9152G, vendor_tx_data_i [63:0] is valid, and vendor_tx_req_o[7:0] is valid.
- 6.144G, vendor_tx_data_i [79:0] is valid, and vendor_tx_req_o[9:0] is valid.
- 9.8304G, vendor_tx_data_i [127:0] is valid, and vendor_tx_req_o[15:0] is valid.
- 8.11008G, vendor_tx_data_i [127:0] is valid, and vendor_tx_req_o [15:0] is valid.
- 10.1376G, vendor_tx_data_i [127:0] is valid, and vendor_tx_req_o [15:0] is valid.
- 12.16512G, vendor_tx_data_i [127:0] is valid, and vendor_tx_req_o[15:0] is valid.

The receiving interfaces are shown in Figure 3-16. When aux_rx_bf_num_o[4:0] is 5'h10, 5'h11, 5'h12, and 5'h13, the control word is vendor-specific control word. Vendor_rx_data_valid_o indicates that receiving vendor-specific control word is valid. Vendor_rx_data_mask_o indicates receiving vendor-specific control word bytes valid signal. If each bit is high, it indicates that the request of vendor-specific control word corresponding to the byte is valid. Vendor_rx_data_o indicates vendor-specific control word data received. The bit widths of vendor_rx_data_mask_o and vendor_rx_data_o are the same as the ones in transmit direction.

Figure 3-15 Vendor Transmitting Interface Timing Diagram

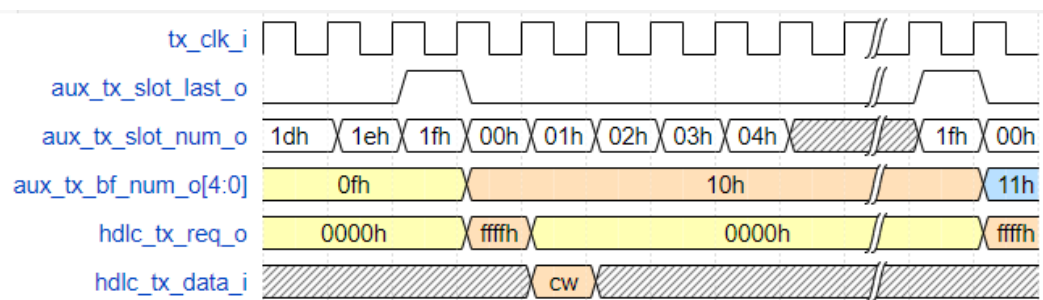
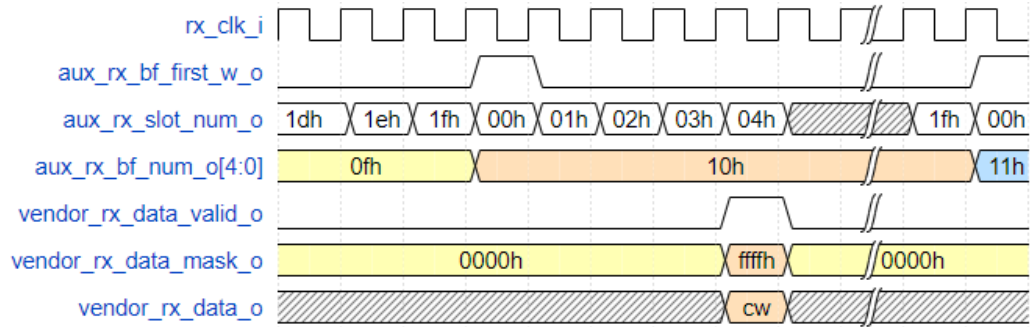


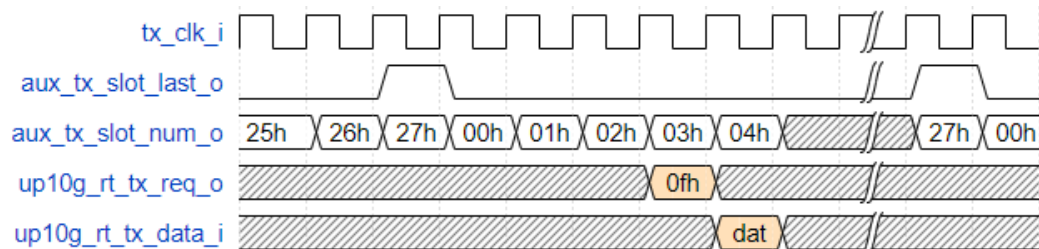
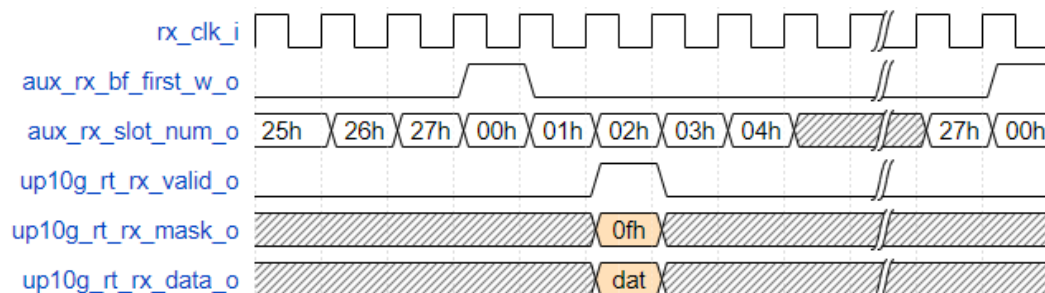
Figure 3-16 Vendor Receiving Interface Timing Diagram

3.5.6 Real-time Vendor-specific Interface Timing Diagram

When the line bit rate of CPRI IP is 10.1376Gbps or 12.16512Gbps, each basic frame has additional bandwidth for data transmission in addition to the 128-bit protocol control word. You can open the real-time vendor-specific interface through the "Real Time Vendor" in the GUI of CPRI IP. And the additional bandwidth is used to transmit user-defined data.

Real-time vendor-specific transmitting interface timing diagram is shown in Figure 3-17. Up10g_rt_tx_req_o is a real-time vendor-specific control word request signal, one clock cycle in advance than up10g_rt_tx_data_i.

The real-time vendor-specific receiving interface timing diagram is shown in Figure 3-18. Up10g_rt_rx_valid_o is a real-time vendor-specific control word valid signal. Up10g_rt_rx_mask_o is a real-time vendor-specific control word byte valid signal. Up10g_rt_rx_data_o is a real-time vendor-specific control word data received.

Figure 3-17 Real-time Vendor-specific Transmitting Interface Timing Diagram**Figure 3-18 Real-time Vendor-specific Receiving Interface Timing Diagram**

3.5.7 Configuration Interface Timing Diagram

The CPRI IP provides configuration interfaces. You can access the internal registers through the configuration interface. The read timing of the configuration interface is shown in Figure 3-19 and the write timing is shown in Figure 3-20.

Figure 3-19 Read Timing Diagram of cfg Interface

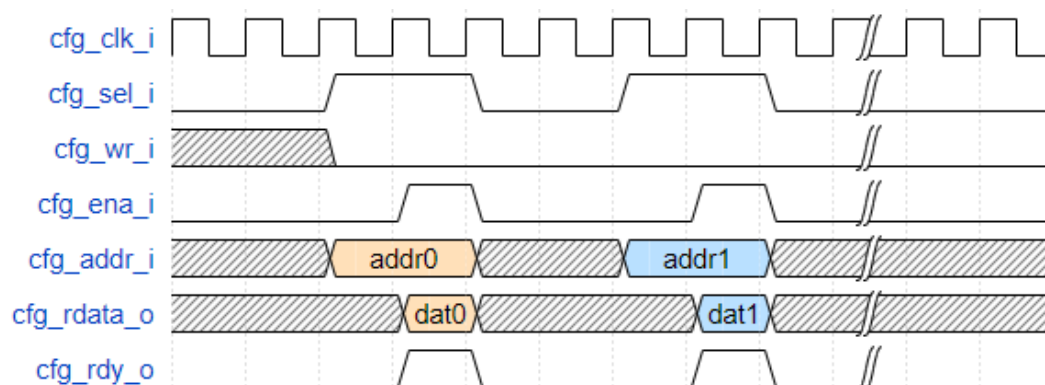
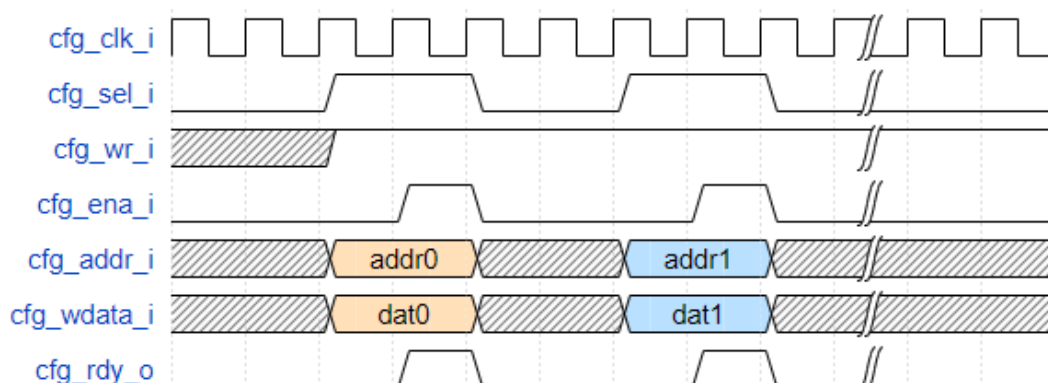


Figure 3-20 Write Timing Diagram of cfg Interface



3.5.8 DRP Interface Timing Diagram

Gowin CPRI IP provides DRP interface through which the user can access the SerDes internal registers.

During the read operation, drp_rden_i is set to high, and the read register address is input to drp_addr_i[23:0] in the first clock cycle when drp_rden_i is set to high. drp_rden_i stays high until drp_rdvld_o is set to high; the corresponding drp_rddata_o[31:0] data is the read data returned from the read operation when drp_rdvld_o is high. drp_rden_i should be set to low in the clock cycle immediately following the assertion of drp_rdvld_o to end the current read operation. The DRP interface read timing is shown in Figure 3-21.

During the write operation, drp_wren_i is set to high, and the write register address is input to drp_addr_i[23:0] in the first clock cycle when drp_wren_i is set high, and the write data is input to drp_wrdata_i[31:0] in the same clock cycle; the fixed 8 'hff is input to drp_strb_i[7:0]. drp_wren_i stays high until drp_ready_o is set to high, and drp_ready_o is set high to

indicate that this write operation is complete. drp_wren_i should be set to low in the clock cycle immediately following the assertion of drp_ready_o to end the current write operation. The write timing is shown in Figure 3-22.

Figure 3-21 DRP Interface Read Timing Diagram

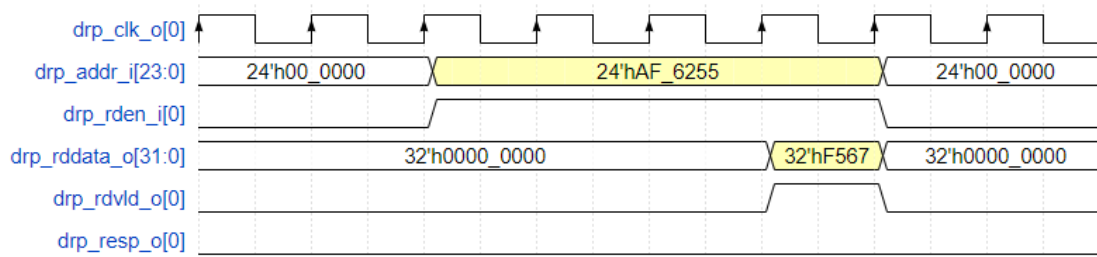
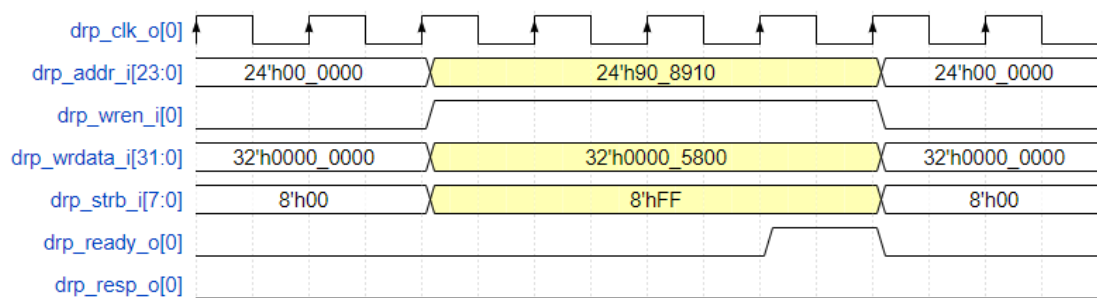


Figure 3-22 DRP Interface Write Timing Diagram



3.6 Register Interface

Table 3-2 Register Description

Address (Byte)	Name	Type	Description
0x0	Link status	RC	Get status and event info. of LOF/LOS/ERR link
0x4	State machine status	RO	Get the status of the internal state machine L1
0x8	Current rate	RO	Select the rate at which IP works.
0xc	Protocol version status	RW or RO	The status of the protocol version on the transmit and receive sides
0x10	Scrambling seed on transmit side	RW or RO	The register to configure the scrambling seed on the transmit side
0x14	Descrambling seed on receive side	RO	The register to fetch the descrambling seed on the receive side
0x18	HDLC rate	RW or RO	HDLC current rate
0x1c	Ethernet rate	RW or RO	Ethernet rate selection, indicated by the P pointer
0x20	HDLC user-defined	RW or RO	User-defined HDLC transmission rate configuration
0x24	Statistics of errors that	RC	The statistical information used to count the errors that occurred

Address (Byte)	Name	Type	Description
	occurred during reception		during reception.
0x28	Loopback configuration	RW	Loopback Register
0x2c	Delay register	RO	The number of delay CLK required for transmitting and receiving within the IP (in clock frequency region)
0x30	Synchronous state on SerDes receive side	RO	The status that indicates whether the synchronization on SerDes receive side is normal or not.

Note!

Register read/write definition:

- RC indicates read-clear
- RO indicates read-only
- RW indicates read-write
- RW or RO; you can choose RW or RO through "Fixed Config Enable" option in the configuration interface. If "Fixed Config Enable" is checked, it indicates that a fixed configuration is used, then this part of register is RO (Read Only). If "Fixed Config Enable" is not checked, it indicates that a nonfixed configuration is used, then this part of register is RW (Read Write).

3.6.1 Link Status (0x0)

Table 3-3 Link Status Register

Name	Bit(s)	Type	Description	Default
rsv	31:28	RO	N/A	0x0
LINE_RATE_MASK	27:16	RO	Bit enable rate, active-high: ● bit16 rsv ● bit17 enables 1.2288Gbps ● bit18 enables 2.4576Gbps ● bit19 enables 3.072Gbps ● bit20 enables 4.9152Gbps ● bit21 enables 6.144Gbps ● bit22 enables 9.8304Gbps ● bit23 rsv ● bit24 enables 8.11008Gbps ● bit25 enables 10.1376Gbps ● bit26 enables 12.16512Gbps ● bit27 rsv	0x0

Name	Bit(s)	Type	Description	Default
ETH_GMII_ENABLE	15	RO	Ethernet selects GMII or MII in the user interface, 0 for MII and 1 for GMII	0x0
local_rx_alarm_event	14	RC	Local LOS or LOF event info.	0x0
local_rx_lof_event	13	RC	Local LOF event info.	0x0
local_rx_los_event	12	RC	Local LOS event info.	0x0
rsv	11:10	RO	N/A	0x0
rx_err_event	9	RC	SerDes receives error event info.	0x0
z130_0_rx_reset_event	8	RC	Receive remote Z.130.0 Reset event info.	0x0
z130_0_rx_rai_event	7	RC	Receive remote Z.130.0 RAI event info.	0x0
z130_0_rx_sdi_event	6	RC	Receive remote Z.130.0 SDI event info.	0x0
z130_0_rx_los_event	5	RC	Receive remote Z.130.0 LOS event info.	0x0
z130_0_rx_lof_event	4	RC	Receive remote Z.130.0 LOF event info.	0x0
rx_err	3	RO	SerDes receiving error status indication High, indicates errors exist.	0x0
rsv	2	RO	N/A	0x0
lof	1	RO	L1 loss of frame indication Low, indicates no LOF and frame synchronization is normal.	0x0
los	0	RO	Loss of light signal indication of the optical module Low, indicates no LOS and optical module receiving light signal is normal.	0x0

3.6.2 State Machine Status (0x4)

Table 3-4 L1 State Machine Status Register

Name	Bit(s)	Type	Description	Default
rsv	31:13	RO	N/A	0x0
state_l1_sync	12:8	RO	L1 Synchronous state machine status: ● 5'b00001: C_XACQ1 ● 5'b00010: C_XACQ2 ● 5'b00100: C_XSYNC1 ● 5'b01000: C_XSYNC2 ● 5'b10000: C_HFNSYNC	0x0
rsv	7:4	RO	N/A	0x0
rsv	3:0	RO	N/A	0x0

3.6.3 Current Rate (0x8)

Table 3-5 Current Rate Register

Name	Bit(s)	Type	Description	Default
rsv	31:4	RO	N/A	0x0
speed_sel	3:0	RO	Current line bit rate within IP Fixed line bit rates is supported while online negotiation to switch between multiple rates is not supported ● 4'd0, rsv ● 4'd1, 1.2288Gbps ● 4'd2, 2.4576Gbps ● 4'd3, 3.072Gbps ● 4'd4, 4.9152Gbps ● 4'd5, 6.144Gbps ● 4'd6, 9.8304Gbps ● 4'd8, 8.11008Gbps ● 4'd9, 10.1376Gbps ● 4'd10, 12.16512Gbps	0x0

3.6.4 Protocol Version Status (0xc)

Table 3-6 Protocol Version Status Register

Name	Bit(s)	Type	Description	Default
rsv	31:12	RO	N/A	0x0
rx_protocol_ver	11:8	RO	Version info. received, 4'h1 or 4'h2	0x0
rsv	7:4	RO	N/A	0x0
tx_protocol_ver	3:0	RW or RO	Protocol version info. transmitted, 4'h1 or 4'h2 You can preset the initial value through "Preset Configuration".	0x0

3.6.5 Scrambling Seed on Transmit Side (0x10)

Table 3-7 Transmitting Scrambling Seed Registers

Name	Bit(s)	Type	Description	Default
rsv	31	RO	N/A	0x0
scrambler_seed	30:0	RW or RO	Scrambling seed on transmit side You can preset the initial value through "Preset Configuration".	0x0

3.6.6 Descrambling Seed on Receive Side (0x14)

Table 3-8 Receiving Descrambling Seed Register

Name	Bit(s)	Type	Description	Default
rsv	31	RO	N/A	0x0
descrambler_seed	30:0	RO	Descrambling Seed on Receive Side, scrambling seed	0x0

Name	Bit(s)	Type	Description	Default
			recovered from received data.	

3.6.7 HDLC Rate (0x18)

Table 3-9 HDLC Rate Register

Name	Bit(s)	Type	Description	Default
rsv	31:11	RO	N/A	0x0
hdlc_rx_rate	10:8	RO	The HDLC rate received, the rate parsed from the receiving data control word.	0x0
rsv	7:3	RO	N/A	0x0
hdlc_tx_rate	2:0	RW or RO	The HDLC transmitted You can preset the initial value through "Preset Configuration". ● 0: no hdlc ● 1: 240kbps ● 2: 480kbps ● 3: 960kbps ● 4: 1920kbps ● 5: 2400kbps ● 6: Highest possible HDLC bit rate for line bit rates above 3072.0Mbit/s ● 7: HDLC bit rate negotiated on higher layer (User defined HDLC rate)	0x2

3.6.8 Ethernet Rate (0x1c)

Table 3-10 Ethernet Rate Register

Name	Bit(s)	Type	Description	Default
rsv	31:14	RO	N/A	0x0
rx_eth_pointer	13:8	RO	Ethernet P Pointer received, P Pointer parsed from the receiving data control word.	0x0
rsv	7:6	RO	N/A	0x0
tx_eth_pointer	5:0	RW or RO	Ethernet P Pointer transmitted You can preset the initial value through "Preset Configuration", which ranges from 20 to 63.	0x14

3.6.9 HDLC User-defined (0x20)

Table 3-11 HDLC User-defined Register

Name	Bit(s)	Type	Description	Default
hdlc_user_mask	31:16	RO	It takes effect only when hdlc_rate is 3'b111. 16bit corresponds to the enable signal for the 16byte control word, indicating the byte position where HDLC data needs to be transmitted is user-defined. Note! Reserved for Design, disabled in V1.0	0x0
rsv	15:4	RO	N/A	0x0
hdlc_user_byte	3:0	RO	It takes effect only when hdlc_rate is 3'b111, the range of 0~15, which indicates the user-defined HDLC byte number needs to be transmitted. Note! Reserved for Design, disabled in V1.0	0x0

3.6.10 Statistics of Errors that Occurred During Reception (0x24)

Table 3-12 Receiving Error Statistics Register

Name	Bit(s)	Type	Description	Default
rsv	31:16	RO	N/A	0x0
rx_err_cnt	15:0	RC	Statistics of errors that occurred during reception, read-clear	0x0

3.6.11 Loopback Configuration (0x28)

Table 3-13 Loopback Configuration Register

Name	Bit(s)	Type	Description	Default
rsv	31:0	RO	N/A	0x0

3.6.12 Delay Register (0x2c)

Table 3-14 Delay Register

Name	Bit(s)	Type	Description	Default
total_rx_delay	31:16	RO	The number of delay CLK received within IP (in rx_clk_i clock region), excluding SerDes Hard Core receiving.	0x0
total_tx_delay	15:0	RO	The number of delay CLKs transmitted within IP (in the tx_clk_i clock region), excluding SerDes Hard Core	0x0

Name	Bit(s)	Type	Description	Default
			transmitting.	

3.6.13 Synchronous Status on SerDes Receive Side (0x30)

Table 3-15 SerDes Receiving Synchronous Status Register

Name	Bit(s)	Type	Description	Default
rsv	31:1	RO	N/A	0x0
rx_sync	0	RC	Receiving SerDes Synchronous Status Register High, indicates that the link synchronization is normal.	0x0

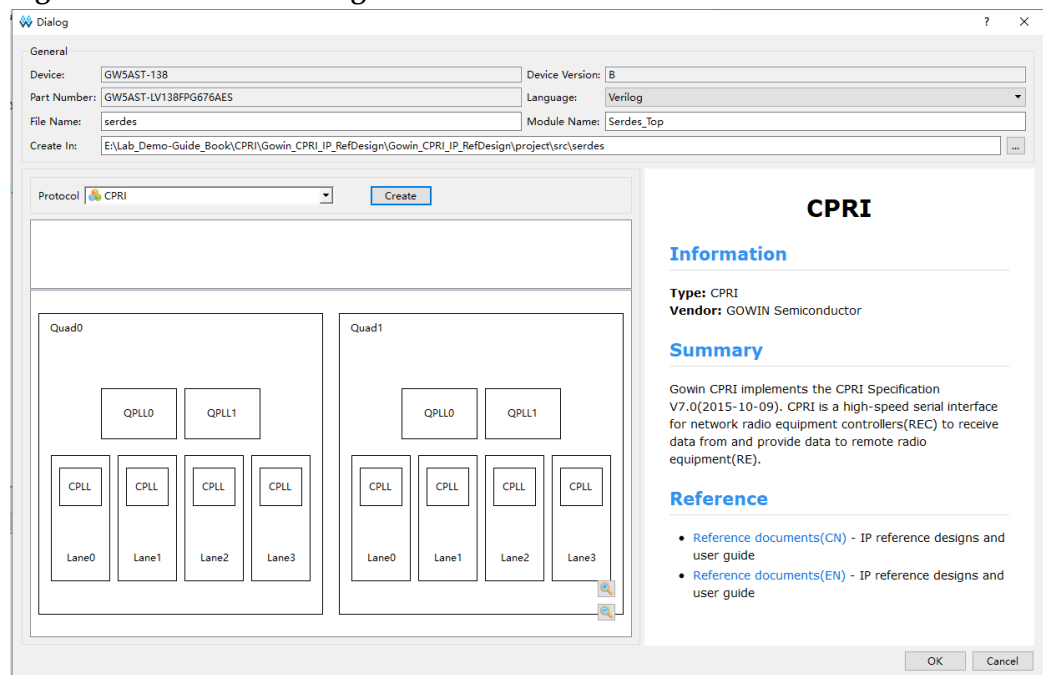
4 Interface Configuration

You can call and configure Gowin CPRI IP using the IP core generator tool in the IDE.

1. Open SerDes IP

After creating the project, click the "Tools" tab in the upper left interface, click "IP Core Generator" from the drop-down list to open Gowin IP Core Generator. Then locate SerDes under the Soft IP Core directory, and double-click to open SerDes IP.

Figure 4-1 SerDes IP Configuration Interface



2. Open CPRI IP

After opening SerDes IP, find CPRI in the "Protocol" drop-down list and click "Create" to open the CPRI IP protocol configuration interface.

Figure 4-2 CPRI IP Configuration Interface

General

Device: GW5AST-138 Device Version: B

Part Number: GW5AST-LV138FPG676AC2/I1 Language: Verilog

File Name: cpri Module Name: CPRI_Top

Create In: m\Gowin_CPRI_RefDesign_DK_D-Board_JESD-CPRI_V1_8chCPRI_addupar\project\src\serdes\cpri

CPRI Core Configuration | PHY Configuration | AFE Configuration | Optional Ports Configuration

Speed Selection

☐ 3.072G and Under

☐ 6.144G and Under

☐ 9.8304G and Under

☒ 10.1376G and Under

☐ 12.16512G and Under

Speed Enable

☐ 0.6144Gbps ☐ 6.144Gbps

☐ 1.2288Gbps ☐ 9.8304Gbps

☐ 2.4576Gbps ☐ 8.11008Gbps

☐ 3.072Gbps ☒ 10.1376Gbps

☐ 4.9152Gbps ☐ 12.16512Gbps

Master or Slave

☒ Master

☐ Slave

Ethernet Selection

☐ MII

☒ GMII

☐ Fixed Config Enable

Config Clk Period: 50 (1~150MHz)

☐ Real Time Vendor

Preset configuration

Initial Protocol Version: ☒ 1 ☐ 2

Initial Ethernet Pointer: 14 (6'h14~6'h3f)

Initial HDLC Rate: 2 (8'h0~8'h7)

Initial Scrambler Seed: 00000000 (31'h0~31'h7ffffff)

User HDLC Byte: 0 (4'h0~4'hf)

User HDLC Mask: 0000 (16'h0~16'hffff)

OK Cancel

3. Configure CPRI IP protocol

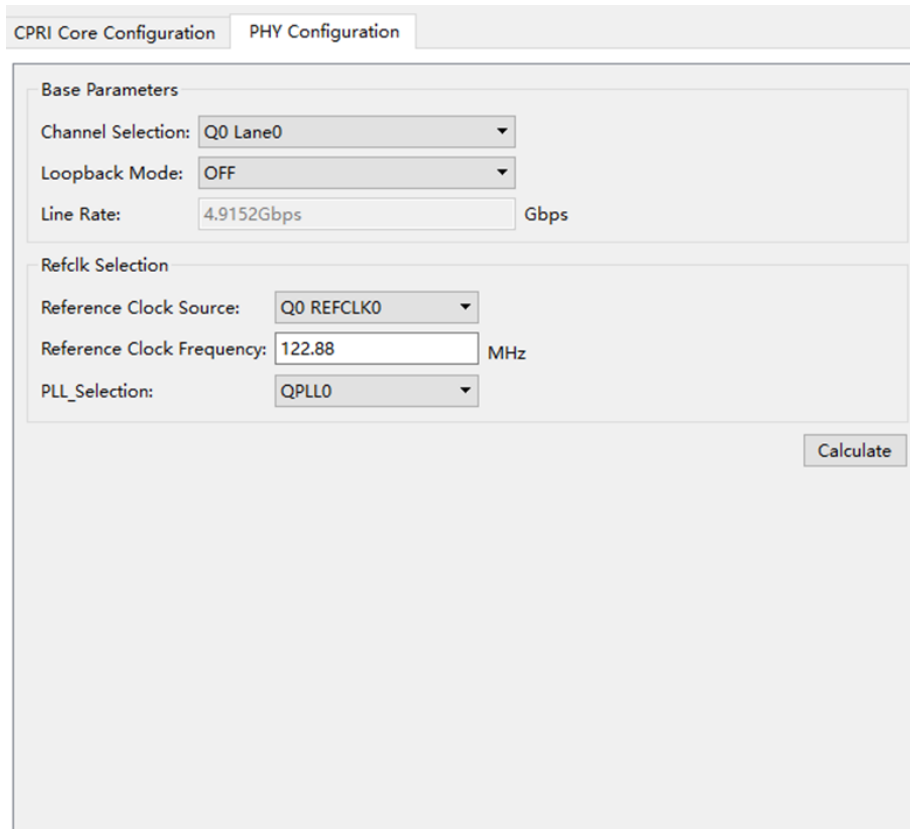
The CPRI IP configuration interface includes "CPRI Core Configuration" and "PHY Configuration", as shown in Figure 4-3 and Figure 4-4. You can select the parameters related to CPRI IP specification on the "CPRI Core Configuration" interface and the parameters related to CPRI IP SerDes on the "PHY Configuration" interface. The descriptions of parameters are shown in Table 4-1. When you have selected the CPRI IP parameters, click the "OK" button to generate the configuration associated with CPRI IP protocol.

4. Complete SerDes IP configuration

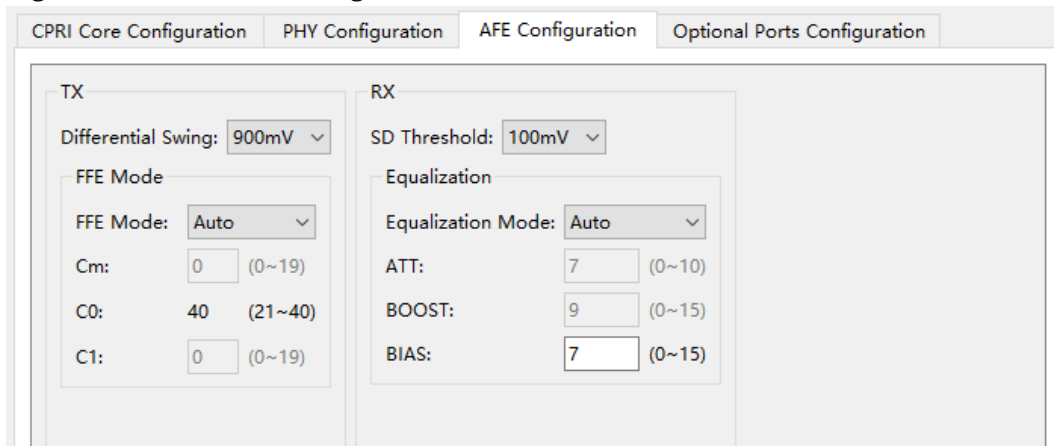
In the SerDes IP interface, the user completes the configuration of all protocols and then clicks the "OK" button to complete the generation of the SerDes IP. In the SerDes IP top-level file, the signal with the `cpri_` prefix is the signal associated with CPRI IP.

Figure 4-3 CPRI Core Protocol Configuration Interface

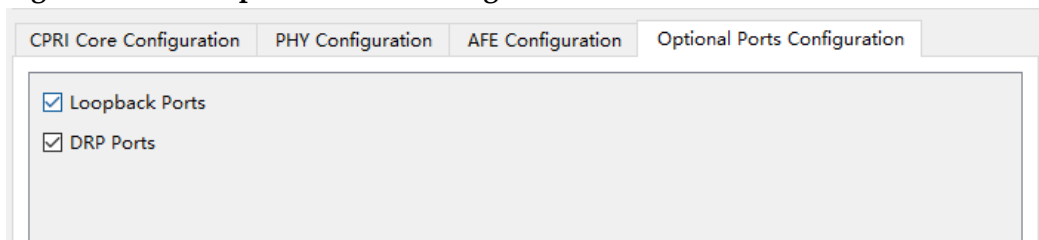
CPRI Core Configuration	PHY Configuration	AFE Configuration	Optional Ports Configuration
Speed Selection ☐ 3.072G and Under ☐ 6.144G and Under ☐ 9.8304G and Under ☒ 10.1376G and Under ☐ 12.16512G and Under Speed Enable ☐ 0.6144Gbps ☐ 6.144Gbps ☐ 1.2288Gbps ☐ 9.8304Gbps ☐ 2.4576Gbps ☐ 8.11008Gbps ☐ 3.072Gbps ☒ 10.1376Gbps ☐ 4.9152Gbps ☐ 12.16512Gbps			
Master or Slave ☒ Master ☐ Slave Ethernet Selection ☐ MII ☒ GMII			
☐ Fixed Config Enable Config Clk Period 50 (1~150MHz) ☐ Real Time Vendor			
Preset configuration Initial Protocol Version ☒ 1 ☐ 2 Initial Ethernet Pointer 14 (6'h14~6'h3f) Initial HDLC Rate 2 (8'h0~8'h7) Initial Scrambler Seed 00000000 (31'h0~31'h7ffffff) User HDLC Byte 0 (4'h0~4'hf) User HDLC Mask 0000 (16'h0~16'hffff)			

Figure 4-4 CPRI PHY Configuration Interface


The screenshot shows the 'PHY Configuration' tab of the CPRI Core Configuration interface. It contains two main sections: 'Base Parameters' and 'Refclk Selection'. In the 'Base Parameters' section, 'Channel Selection' is set to 'Q0 Lane0', 'Loopback Mode' is 'OFF', and 'Line Rate' is '4.9152Gbps'. In the 'Refclk Selection' section, 'Reference Clock Source' is 'Q0 REFCLK0', 'Reference Clock Frequency' is '122.88 MHz', and 'PLL_Selection' is 'QPLL0'. A 'Calculate' button is located at the bottom right of the configuration area.

Figure 4-5 CPRI AFE Configuration


The screenshot shows the 'AFE Configuration' tab of the CPRI Core Configuration interface. It is divided into 'TX' and 'RX' sections. The 'TX' section includes 'Differential Swing' (900mV), 'FFE Mode' (Auto), and three input fields: 'Cm' (0, range 0~19), 'C0' (40, range 21~40), and 'C1' (0, range 0~19). The 'RX' section includes 'SD Threshold' (100mV), 'Equalization Mode' (Auto), and three input fields: 'ATT' (7, range 0~10), 'BOOST' (9, range 0~15), and 'BIAS' (7, range 0~15).

Figure 4-6 CPRI Optional Ports Configuration


The screenshot shows the 'Optional Ports Configuration' tab of the CPRI Core Configuration interface. It contains two checked checkboxes: 'Loopback Ports' and 'DRP Ports'.

Table 4-1 CPRI IP Configuration Interface Parameters

Name	Range	Default	Description
CPRI Core Configuration			
Speed Selection	3.072G and Under, 6.144G and Under, 9.8304G and Under, 10.1376G and Under 12.16512G and Under	None	Rate range selection. The port signal bit width differs from the three options, but the valid bit width is bound to the rate. See 3.4 Port List for more details. ● 3.072G and Under, data link bit width of 16 bits, vendor-specific control word 40 bits. ● 6.144G and Under, data link bit width of 32 bits, vendor-specific control word 80 bits. ● 9.8304G and Under, data link bit width of 64 bits, vendor-specific control word 128 bits. ● 10.1376G and Under, data link bit width of 64 bits, vendor-specific control word 128 bits. ● 12.16512G and Under, data link bit width of 64 bits, vendor-specific control word 128 bits. For example, if the user's Speed Selection selects 9.8304G and Under, the Speed Enable checks 3.072Gbps, the bit width of iq_tx_data_i and iq_rx_data_o of the port is 64 bits, but only the lower 16bit is actually valid.
Speed Enable	1.2288Gbps, 2.4576Gbps, 3.072Gbps, 4.9152Gbps, 6.144Gbps, 9.8304Gbps, 8.11008Gbps, 10.1376Gbps 12.16512Gbps	None	Enable CPRI IP work line rate, the user can check the supported rate. Currently, only one rate is supported to be checked, and multiple rates are not supported to be checked.
Ethernet Select	MII, GMII	MII	The user selects the Ethernet interface as either the MII interface or the GMII interface.
Fixed Config Enable	Check/Uncheck	Unchecked	Fixed configuration options: ● If checked, part of the configuration is fixed when initialized and does not support on-line configurations, including protocol version number, scrambler seed, HDLC rate, and Ethernet P Pointer. It is beneficial for resources and timing when this option is checked. ● If unchecked, on-line configuration is supported, and the user can modify the protocol version number, scrambler seed, HDLC Rate and Ethernet P Pointer via configuring the interface.

Name	Range	Default	Description
Config Clk Period	1 to 150MHz	50MHz	Configuration clock frequency at which the CPRI IP Configuration Module operates.
Real Time Vendor	Check/Uncheck	Unchecked	Enables or disables Vendor-specific Control Word for 10.1376Gbps and above line rate Example: When the line rate is 10.1376Gbps, if user choose to check "Real Time Vendor", then in addition to the 128-bit basic control word, the additional 32-bit control word will use the interface timing defined in 3.5.6 Real-time Vendor-specific Interface Timing Diagram to send and receive data. If the user chooses not to check "Real Time Vendor", the additional 32-bit control word is used to transmit IQ data.
Initial Protocol Version	1, 2	1	The protocol version control word reset default value
Initial Scrambler Seed	31'h0~31'h7ffffff	0	Scrambler seed reset default value
Initial Ethernet Pointer	6'h14~6'h3f	6'h14	Ethernet P pointer control word reset default value
Initial HDLC Rate	8'h0~8'h7	8'h2	The HDLC rate control word reset default value
PHY Configuration			
Channel Selection	Q0 Lane0, Q0 Lane1, Q0 Lane2, Q0 Lane3, Q1 Lane0, Q1 Lane1, Q1 Lane2, Q1 Lane3,	None	SerDes lane selection Q0 and Q1 correspond to two Quads for SerDes. Lane0, Lane1, Lane2, and Lane3 indicate the 4 Lane numbers for each Quad of SerDes.
Loopback Mode	OFF, LB_NES, LB_FES, LB_ENC	OFF	SerDes Loopback Mode Selection: ● OFF indicates Normal mode, SerDes data is transmitted and received normally. ● LB_NES, SerDes internal loopback, data is looped back to receive side from the transmit side of SerDes. ● LB_ENC, SerDes internal loopback, data is looped back to receive side from the transmit side of SerDes. ● LB_FES, SerDes external loopback, data is looped back to transmit side from the receive side of SerDes.
Reference Clock Source	● For devices GW5AST-138/GW5AT-138/GW5AT-75 Q0 REFCLK0, Q0 REFCLK1, Q1 REFCLK 0, Q1 REFCLK 1	Q0 REFCLK0	● For devices GW5AST-138/GW5AT-138/GW5AT-75: The reference clock selection for high-speed transceivers is as follows: Q0/Q1 corresponds to the two Quads of SerDes. REFCLK0 and REFCLK1 correspond to the two input reference clocks for each SerDes Quad. Users can

Name	Range	Default	Description
	For devices GW5AT-60 Q0 REFCLK0, Q0 REFCLK1, Q0 REFCLK2, Q0 REFCLK3, SERDES Q0CLKIN0, SERDES Q0CLKIN1, SERDES Q0CLKIN2, SERDES Q0CLKIN3		select the input reference clock according to their application needs. For devices GW5AT-60: The reference clock selection for high-speed transceivers is as follows: Q0REFCLK0, Q0REFCLK1, Q0REFCLK2, and Q0REFCLK3 correspond to the four input reference clocks for Quad0. SERDES Q0CLKIN0, SERDES Q0CLKIN1, SERDES Q0CLKIN2, and SERDES Q0CLKIN3 correspond to the input reference clocks for dedicated GPIO pins. The selectable input reference clocks vary depending on the chip package.
Reference Clock Frequency	User input	122.88M	The input reference clock for high-speed transceivers. After inputting the reference clock, you can click the "Calculate" button to confirm if the frequency is correct.
PLL Selection	QPLL0, QPLL1, CPLL	QPLL0	PLL selection
AFE			
Differential Swing	100mV~900mV	900mV	Configure TX differential signal swing Vdiffpp, Vdiffpp=2xVdiff
FFE Mode	Auto, Manual	Auto	Configure TX FFE mode - Auto: Auto mode - Manual: Manual mode
Cm	0~19	0	Transmit FFE pre-cursor
C0	21~40	40	Transmit FFE main-cursor
C1	0~19	0	Transmit FFE post-cursor
SD Threshold	25mV~200mV	100mV	Receive differential signal SD threshold
Equalization Mode	Auto, Manual	Auto	Configure RX equalization mode - Auto: Auto mode - Manual: Manual mode
ATT	0~10	7	Adjust RX intermediate-frequency attenuation, with smaller values indicating greater attenuation.
BOOST	0~15	9	Adjust RX high-frequency amplification, with larger values indicating larger gain.
BIAS	0~15	7	Configure SerDes amplification parameters for the RX signal. The higher the configuration, the stronger the amplification of the signal.
Optional Ports			
Loopback Ports	Checked/Unchecked	Unchecked	Loopback Port Selection: If checked, the IP outputs SerDes loopback port. The port supports the configuration of SerDes PMA internal and external loops.

Name	Range	Default	Description
			● If unchecked, the IP does not output this port.
DRP Port	Checked/Unchecked	Unchecked	DRP Port Selection: ● If checked, the IP outputs the DRP port. The port supports access to SerDes internal registers. ● If unchecked, the IP does not output this port.

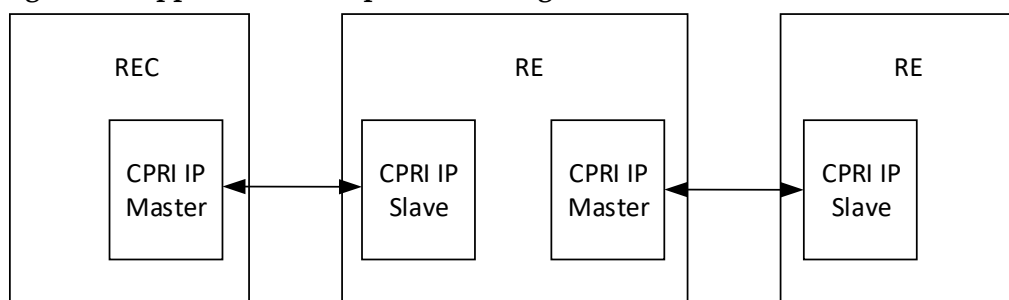
5 Reference Design

For more information, please see the CPRI reference designs at [Gowin website](#).

5.1 Applications

Gowin CPRI IP can be used as REC or RE. Figure 5-1 shows an application example consisting of REC and two-level RE.

Figure 5-1 Application Example Block Diagram



The line rates supported by CPRI IP in different Gowin devices are shown in Table 5-1.

Table 5-1 Supported Line Rate

Series	Device	Speed	Supported Line Bit Rates (Gbps)
GW5A	GW5AT-138/ GW5AST-138	C1	1.2288, 2.4576, 3.072, 4.9152, 6.144, 9.8304, 8.11008
GW5A	GW5AT-138/ GW5AST-138	ES/C2	1.2288, 2.4576, 3.072, 4.9152, 6.144, 9.8304, 8.11008, 10.1376, 12.16512Gbps

5.2 Reference Design Features

The Gowin CPRI IP reference design not only includes CPRI IP and peripheral code but also includes the following functions for transmitting test data and verifying data on receive side:

- Support IQ channel test data generation on transmit side and received data detection on receive side, and test data supports both PRBS and incremental numbers.
- Support Ethernet message generation on transmit side and received

data detection on receive side, supports GMII and MII interfaces, and test data is fixed Ethernet messages.

- Support HDLC generation on transmit side and received data detection on receive side, test data is PRBS data.
- Support vendor-specific control word data transmit and receive.
- Support debug module, users can directly read the internal registers of FPGA to get status, error statistics and perform on-line register configuration through the serial port tool.

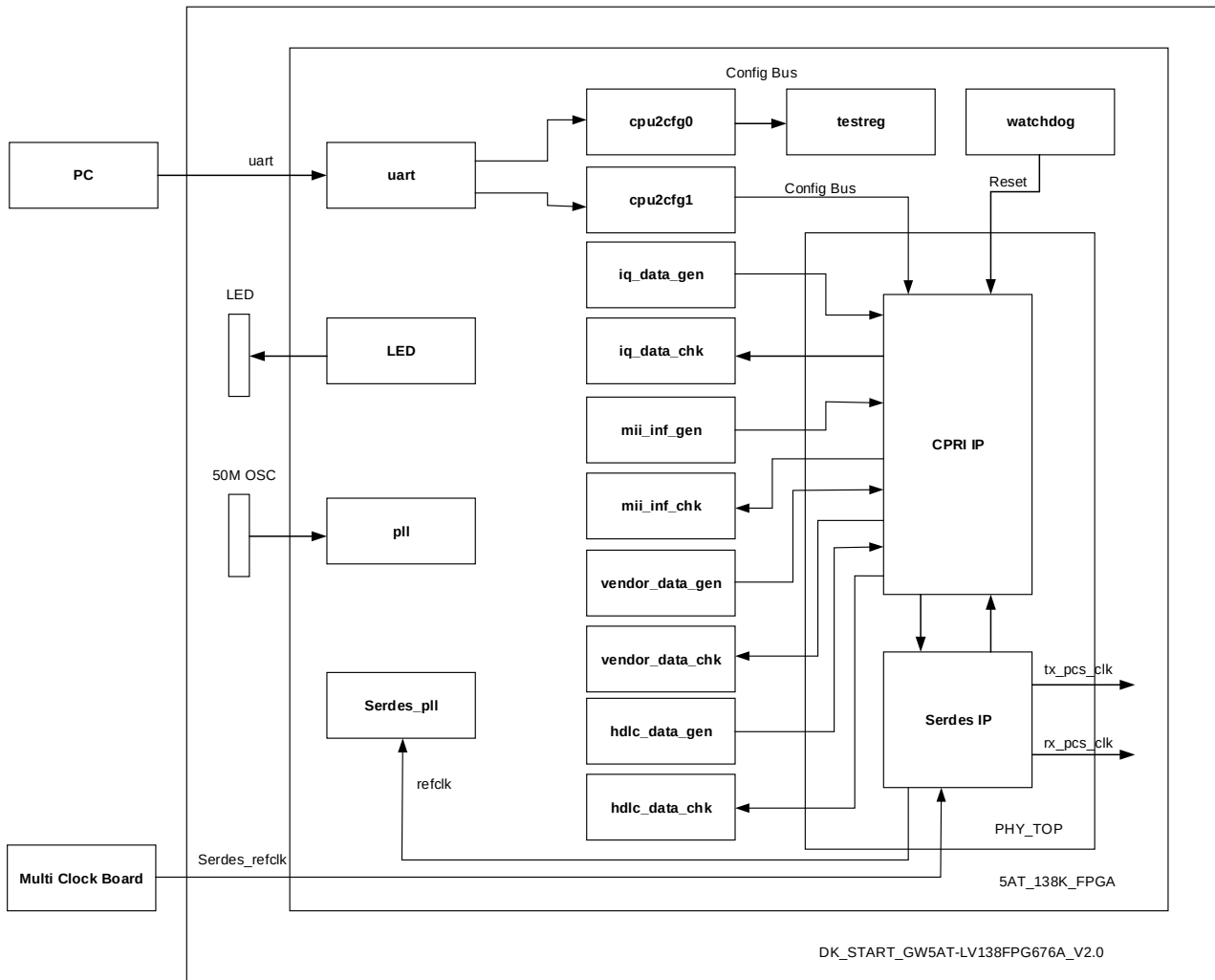
5.3 CPRI IP Reference Design Project

PC can access the testreg module registers and CPRI IP internal registers within the reference design through the serial port tool. The address space of testreg is 0x000~0x3ff (byte address) and the address space of CPRI IP is 0x400~0x7FF (byte address). PC can get the interface link status and statistics directly through the register.

The reference design contains the following modules:

- Uart to Bus: Serial port to configuration bus module
- testreg: Maintain a set of internal registers, users access to obtain link status
- watchdog: The watchdog resets the link at intervals if the link fails to synchronize
- led: If the internal data verification is passed, the light will be on, so that users can directly observe the test results through LEDs, etc.
- gowin_pll: The output of the single board internal 50MHz crystal oscillator is used as the input of PLL. And PLL locks the phase and outputs the clocks for the configuration module and Ethernet module (MII 25MHz, GMII 125MHz)
- gowin_pll_serdes: Uses gtr12_tx_pcs_clk_o output from SerDes as the PLL reference clock to lock out the frequency needed for IP operation. For example, for 10.1376Gbps rate, use 158.4MHz gtr12_tx_pcs_clk_o as the PLL reference clock, and output 153.6MHz as the IP operation clocks tx_clk_i and rx_clk_i
- iq_data_gen: IQ test data generation module
- iq_data_chk: IQ test data detection module
- mii_inf_gen: MII interface test data generation module
- mii_inf_chk: MII interface test data detection module
- vendor_data_gen: Vendor-specific control word test data generation module
- vendor_data_chk: Vendor-specific control word test data detection module
- hdlc_data_gen: HDLC test data generation module
- hdlc_data_chk: HDLC tests the data detection module

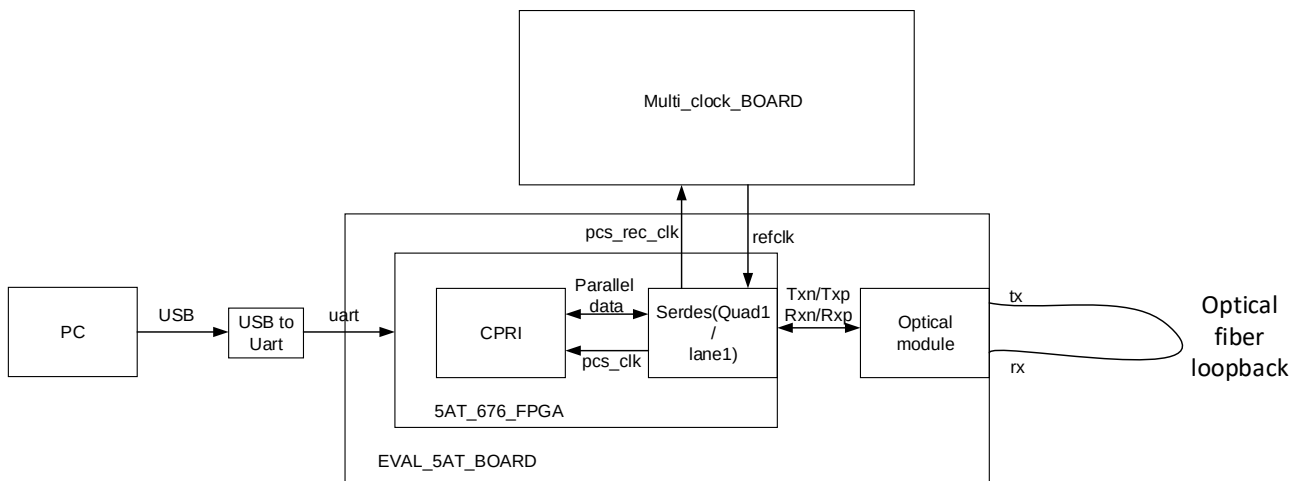
Figure 5-2 Reference Design Instance Basic Structure Diagram



5.4 Reference Design Board Test

The steps for reference project board test are as follows:

- Download the project from the website and compile to generate bit file.
- The build environment is shown in Figure 5-3.

Figure 5-3 Test Environment Block Diagram

When the environment is built, input "R 0" in the serial port tool and the register value is displayed as shown in Figure 5-4. If you input "W 0 value", the register value corresponding to value will be written to the register, and if you readback "R 0", the register will change to the re-written value.

Note!

The register address operated by the serial port tool is the word address, and the word address multiplied by 4 equals the byte address in the register list. For example, R2, indicating the read address 0x2, corresponds to the address 0x8 bytes in the register list.

Table 5-2 testreg Register Description

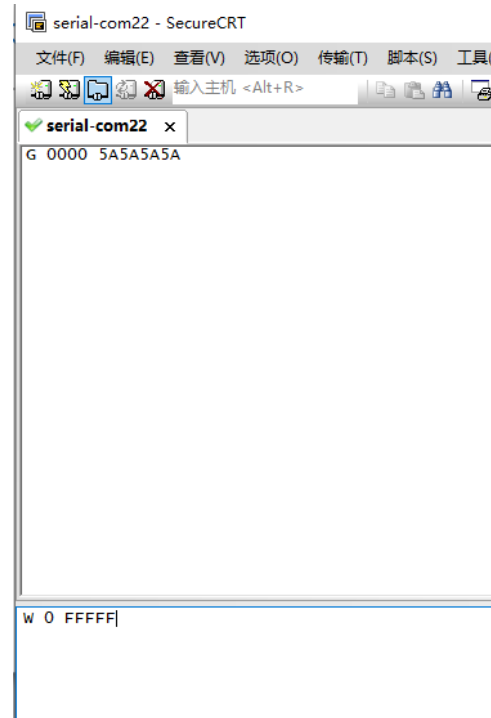
Address (Byte)	Type	Data Width	Signal Name	Description
0x0	RW	[31:0]	test_reg	Test registers that can be written and read back, confirming the register read and write function.
0x4	RO	[31:10]	Rsv.	N/A
	RW	[9]	test_mode	RSV test data select PRBS or incremental numbers, reference project is disabled.
	RW	[8]	insert_err	Insert error code during RSV and PRBS test, reference project is disabled.
	RO	[7:2]	Rsv.	N/A
	RW	[1:0]	loop_en	RSV reference project is disabled and can be used to configure loopback points.
0x8	RO	[31:8]	Rsv.	N/A
	RW	[7:4]	speed_sel	Rate selection, 0~0xa corresponds to the rate of CPRI ● 4'd0, rsv ● 4'd1, 1.2288Gbps ● 4'd2, 2.4576Gbps ● 4'd3, 3.072Gbps ● 4'd4, 4.9152Gbps ● 4'd5, 6.144Gbps ● 4'd6, 9.8304Gbps ● 4'd8, 8.11008Gbps ● 4'd9, 10.1376Gbps

Address (Byte)	Type	Data Width	Signal Name	Description
				● 4'd10, 12.16512Gbps
	RO	[3:1]	Rsv.	N/A
	RW	[0]	local_lof	LOF indication, 0 indicates no frame loss of lock, normal.
0xc	RO	[31:16]	Rsv.	N/A
		[15:0]	frame_count	Receive frame statistics
0x10	RO	[31:16]	Rsv.	N/A
		[15:0]	mii_package_cnt	Ethernet frame statistics
0x14	RO	[31:24]	vendor_err_cnt	Vendor-specific control word error statistics
		[23:16]	hdlc_err_cnt	HDLC error statistics
		[15:0]	iq_error_count	IQ data error statistics
0x18	RO	[31:8]	Rsv.	N/A
		[7:0]	mii_err_cnt	Ethernet frame error statistics

Note!

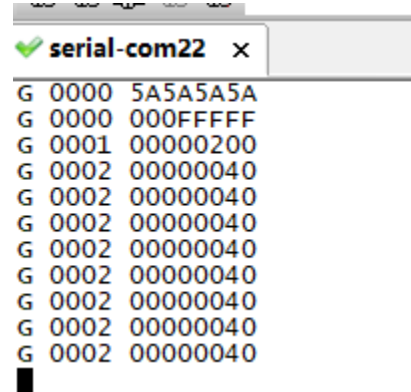
Register read/write definition:

- RO indicates read-only
- RW indicates read-write

Figure 5-4 Serial Port Tool Display 1

Open the CRT read register to confirm the link status. Read register 0x2, bit0 being 0 indicates that lof is low without frame loss of lock. bit3~bit7 indicates the line rate at which the current RTL protocol is operating. As shown in Figure 5-5, bit3~bit7 being 0x4 indicates that the current line rate is 4.9152Gbps.

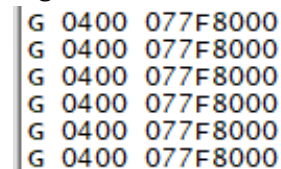
Figure 5-5 Serial Port Tool Display 2



Read the IP core internal registers to confirm the link status.

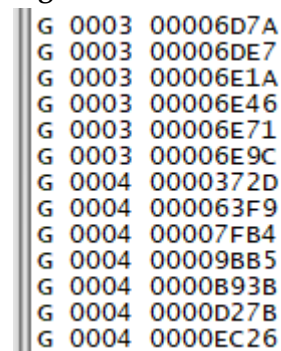
Read register 0x400, which is the register address 0x0 within the CPRI IP. Bit0, bit1, and bit3 are all low, indicating no LOS/LOF/RX_ERR status currently. The _event suffix indicates an event. See [3.6.1 Link Status \(0x0\)](#) for register descriptions.

Figure 5-6 Serial Port Tool Display 3



Read the receive frame statistics and the Ethernet packet statistics, an increase indicates that the link is transmitting and receiving normally. Read registers 0x3 and 0x4. The 0x3 register indicates CPRI radio frame statistics and 0x4 indicates Ethernet receive frame statistics.

Figure 5-7 Serial Port Tool Display 4



Plug in and unplug the fiber to confirm if the interface is relinked:

When the fiber is unplugged, 0x2 registers show frame loss (the 0x2 register value bit0 is high), the receive frame statistics do not increase (the 0x3 register indicates receive frame statistics and the 0x4 indicates Ethernet message statistics), while error frames do not increase (the 0x5 and 0x6 registers).

Figure 5-8 Serial Port Tool Display 5

```

G 0002 00000041
G 0002 00000041
G 0002 00000041
G 0003 000030CD
G 0003 000030CD
G 0004 00001BCC
G 0004 00001BCC
G 0005 070011EC
G 0005 070011EC
G 0006 00000011
G 0006 00000011

```

When the fiber is replugged in, 0x2 indicates frame synchronization (the 0x2 register value bit0 is low), receive frame statistics increase (the 0x3 register indicates receive frame statistics and the 0x4 indicates Ethernet message statistics), while error frames do not increase (the 0x5 and 0x6 registers).

Figure 5-9 Serial Port Tool Display 6

```

G 0002 00000040
G 0002 00000040
G 0002 00000040
G 0002 00000040
G 0002 00000040
G 0003 00003989
G 0003 000039B8
G 0003 000039E9
G 0004 00006F3D
G 0004 00008ED4
G 0004 0000ABCA
G 0005 34102FA2
G 0005 34102FA2
G 0005 34102FA2
G 0006 000000C6
G 0006 000000C6
G 0006 000000C6

```

Read IQ/HDLC/vendor/Ethernet error statistics, continuous non-increase indicates that the link is stable and the verification data is correct:

- 0x5 registers: Bit0~15 IQ error statistics, bit16~bit23 HDLC error statistics, bit24~bit31 Vendor error statistics.
- 0x6 register: Bit0~7 indicates Ethernet receive frame error statistics.

Figure 5-10 Serial Port Tool Display 7

```

G 0005 0003001E
G 0005 0003001E
G 0005 0003001E
G 0005 0003001E
G 0005 0003001E
G 0006 00000000
G 0006 00000000
G 0006 00000000
G 0006 00000000
G 0006 00000000

```

The reference project also provides LED indication for users to quickly determine the link status by LED status. The development board provides 4 LEDs for users. The reference project design is:

- LED0 indicates PLL status. Constant on indicates normal and both pll and SerDes_pll PLLs are locked; Other conditions indicate abnormal.
- LED1 indicates synchronization status. Constant on indicates normal and CPRI frame is no loss of lock; Other conditions indicate abnormal.
- LED2 indicates receive message status. Constant on indicates normal and CPRI radio frame and Ethernet message are received normally; Other conditions indicate abnormal.
- LED3 indicates receive data verification status. Constant on indicates normal and receive data verification is correct (IQ, Vendor, HDLC, Ethernet); other conditions indicate abnormal.

6 File Delivery

The delivery files for the Gowin CPRI IP includes the documents, the design source code, and the reference design.

6.1 Documentation

The folder mainly contains user guides in PDF version.

Table 6-1 Documents List

Name	Description
IPUG1017, Gowin CPRI IP User Guide	Gowin CPRI IP User Guide, that is this manual.

6.2 Design Source Code (Encryption)

The Encryption Code Folder contains the RTL encryption code of Gowin CPRI IP used for the GUI, to generate the IP cores as needed.

Table 6-2 Gowin CPRI IP Design Source Code List

Name	Description
cpri_core_encryption.v	The top-level file of the IP core, which provides users with interface information, encrypted.

6.3 Reference Design

The Gowin CPRI IP RefDesign folder contains the netlist file for Gowin CPRI IP, user reference design, constraints file, top-level file, and project file, etc.

Table 6-3 Gowin CPRI IP RefDesign Folder Content List

Name	Description
cpri_ed_top.v	The top module of reference design
cpri_ed_top.cst	Project physical constraints file
cpri_ed_top.sdc	Project timing constraints file
test	The test incentive folder contains the test incentive module cpri_test.v, ROM initialization files gmii_eth_package.txt, and mii_eth_package.txt.
SerDes	The SerDes IP folder contains the SerDes files and CPRI protocol folder generated by the EDA tool.

Name	Description
debug	The debug and test folder contains output LED module led.v, test register module testreg.v, and Watchdog module watchdog.v.
gowin_pll	The PLL module folder uses the external input 50MHz clock as a reference clock and outputs the internal configuration clock.
gowin_pll_serdes	The PLL module folder, which uses the PCS clock output from SerDes as a reference clock to lock out the IP operating clock, and it is used only for line rates of 8.11008Gbps, 10.1376Gbps, and 12.16512Gbps.
uart_to_bus	Uart to Bus IP folder for converting a serial port to internally configurable bus.

