



Gowin LPC Peripheral IP

User Guide

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Revision History

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1 About This Guide

1.1 Purpose

The purpose of Gowin LPC Peripheral IP User Guide is to help you learn features and usage of this product by providing the descriptions of functions, ports, timing, GUI and reference design, etc.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find related documents at www.gowinsemi.com:

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS821, GW1NS series of FPGA Products Data Sheet](#)
- [DS861, GW1NSR series of FPGA Products Data Sheet](#)
- [DS871, GW1NSE series of SecureFPGA Products Data Sheet](#)
- [DS881, GW1NSER series of SecureFPGA Products Data Sheet](#)
- [DS891, GW1NRF series of Bluetooth FPGA Products Data Sheet](#)
- [DS841, GW1NZ series of FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [DS971, GW2AN-9X & 18X Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
IP	Intellectual Property
LUT	Look-up Table
LPC	Low Pin Count

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Introduction to Gowin LPC Peripheral IP

Gowin LPC Peripheral IP is a general-purpose LPC peripheral interface that complies with LPC standard protocol. This IP can implement I/O read and write functions of the LPC protocol.

Table 2-1 Gowin LPC Peripheral IP Overview

Gowin LPC Peripheral IP	
Supported Devices	● GW1N series ● GW1NR series ● GW1NS series ● GW1NSR series ● GW1NSE series ● GW1NSER series ● GW1NRF series ● GW1NZ series ● GW2A series ● GW2AR series ● GW2ANR series ● GW2AN series
Logic Resource	Please refer to Table 3-1.
Delivered Doc.	—
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	—
Synthesis Software	GowinSynthesis

Gowin LPC Peripheral IP	
Application Software	Gowin Software (V1.9.8.07 and above)

2.2 LPC Introduction

LPC interface is a low bandwidth bus with performance up to 33MHz. It is used to connect CPU peripherals and replace the low-performance ISA bus. Compared to the 52 signal lines of ISA bus, LPC requires only a minimum of 7 signal lines to complete the transmission.

3 Features and Performance

3.1 Features

- Support the standard LPC interface
- Can be as an LPC peripheral interface
- Support I/O read and I/O write
- Users can control the insertion of SYNC wait cycles.

3.2 Working Frequency

Gowin LPC Peripheral IP supports 33MHz operating frequency.

3.3 Resource Utilization

Gowin LPC Peripheral IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different device, or at different density, speed grade or the different mode of IP configuration.

Take GW1N-9 series of FPGA with default configuration for an instance to introduce resource utilization. The resource utilization is shown in Table 3-1. For application verification on other Gowin FPGA, please pay attention to the later release information.

Table 3-1 LPC Peripheral Resource Utilization

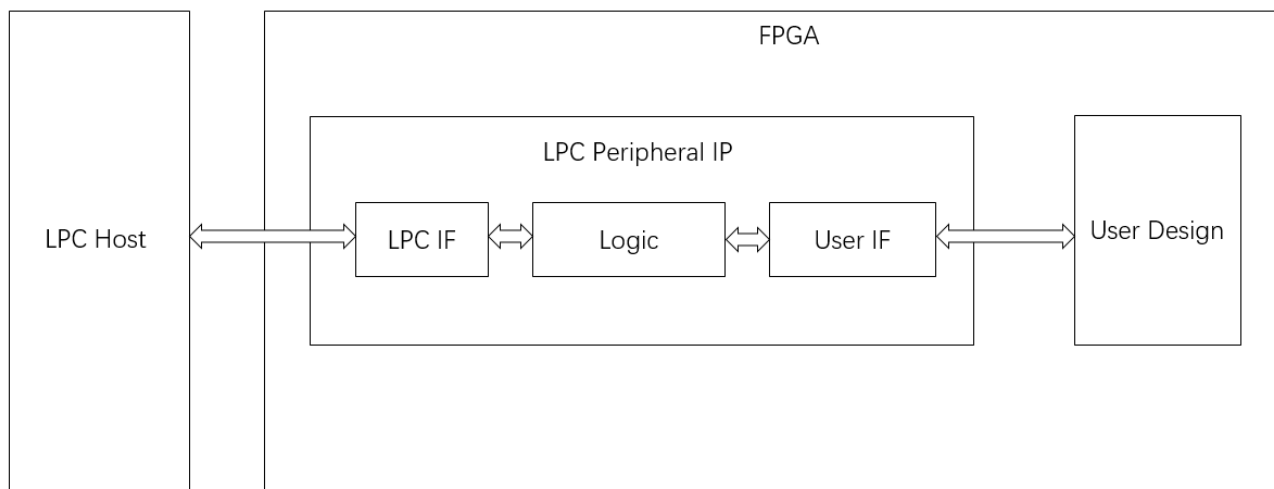
Device	Speed Grade	Name	Resource Utilization	Notes
GW1N-9	C6/I5	LUT	88	-
		REG	31	

4 Functional Description

4.1 LPC Peripheral Structure

Gowin LPC Peripheral IP structure is shown in Figure 4-1. The LPC Peripheral IP allows the LPC Host to interact with the user design.

Figure 4-1 LPC Peripheral Block Diagram



4.2 Port Description

The IO ports of Gowin LPC Peripheral IP are shown in Table 4-1. All signals are synchronized with lclk.

Table 4-1 I/O List of Gowin LPC Peripheral IP

Signal	I/O	Data Width	Description
LPC interface signal			
lclk	input	1	LPC Peripheral LCLK signal
lreset_n	input	1	LPC Peripheral LRESET# signal

Signal	I/O	Data Width	Description
LPC interface signal			
lframe_n	input	1	LPC Peripheral LFRAME# signal
lad	inout	1	LPC Peripheral LAD signal
User interface signal			
io_addr_hit	input	1	Address valid signal
io_addr_hit_ready	output	1	Address valid ready signal
io_wr_en	output	1	IO write enable
io_rd_en	output	1	IO read enable
io_addr	output	16	IO Write/Read address
io_wr_data	output	8	IO write data
io_rd_data	input	8	IO Read data
io_rd_data_ready	output	1	IO read data ready
io_wr_sync_zero	input	1	IO Write Sync=0000 output by IP enable
io_rd_sync_zero	input	1	IO Read Sync=0000 output by IP enable

5 Timing Description

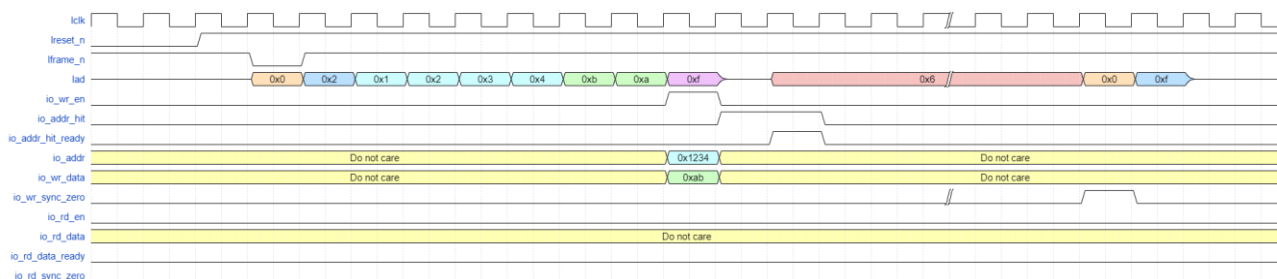
The timing of Gowin LPC Peripheral IP is shown in Figure 5-1 and Figure 5-2.

I/O Write Timing

Gowin LPC Peripheral IP I/O write timing is shown in Figure 5-1.

When the user detects that the `io_wr_en` signal is 1, `io_addr` and `io_wr_data` signals are valid. Then the user determines whether `io_addr` is within the range allowed by the slave. If it is within the range, the `io_addr_hit` signal is pulled up until `io_addr_hit_ready=1` is detected, and then the `io_addr_hit` signal is pulled down; if it is out of the range, the `io_addr_hit` signal does not need to be pulled up. At any time after the user detects `io_addr_hit_ready=1`, the user can set `io_wr_sync_zero =1`, then the IP sends `Sync=0000` to the LPC bus to complete a bus operation. If `io_wr_sync_zero` is always 0, the IP inserts `Sync=0110` cycles to the LPC bus to prevent the end of this write operation. The write address and write data are the values of `io_addr` and `io_wr_data` respectively when `io_wr_en=1`.

Figure 5-1 Gowin LPC Peripheral IP I/O Write Timing



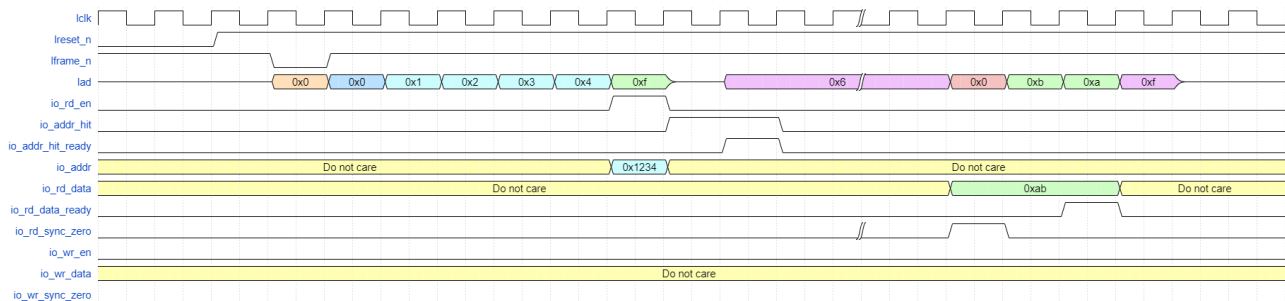
I/O Read Timing

Gowin LPC Peripheral IP I/O read timing is shown in Figure 5-2.

When the user detects that the `io_rd_en` signal is 1, `io_addr` signal is

valid. Then the user determines whether `io_addr` is within the range allowed by the slave. If it is within the range, the `io_addr_hit` signal is pulled up until `io_addr_hit_ready=1` is detected, and then the `io_addr_hit` signal is pulled down; if it is out of the range, the `io_addr_hit` signal does not need to be pulled up. At any time after the user detects `io_addr_hit_ready=1`, the user can set `io_rd_sync_zero = 1`, then the IP sends `Sync=0000` to the LPC bus. At the same time, the user needs to assign the read data to the `io_rd_data` signal until `io_rd_data_ready=1` is detected. At this point, an IO read operation is completed. If `io_rd_sync_zero` is always 0, the IP inserts `Sync=0110` cycles to the LPC bus to prevent the end of this read operation. Read address is the value of `io_addr` when `io_rd_en=1`; read data is the value assigned to `io_rd_data` when `io_rd_en=1`.

Figure 5-2 Gowin LPC Peripheral IP I/O Read Timing

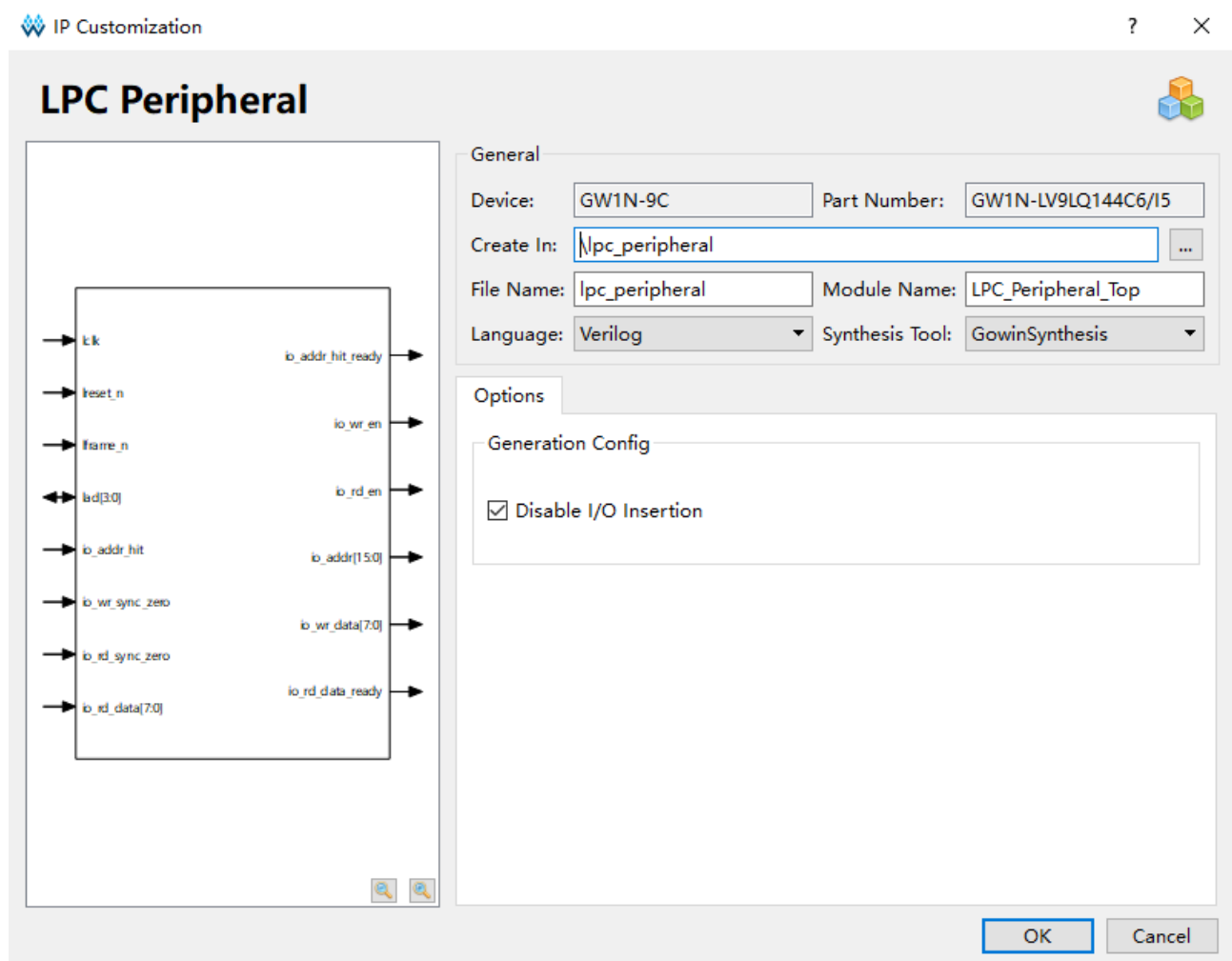


6 Interface Configuration

You can select Tools in Gowin Software to start the IP Core Generator to invoke and configure Gowin LPC Peripheral IP.

Gowin LPC Peripheral IP configuration interface is shown in Figure 6-1.

Figure 6-1 Gowin LPC Peripheral IP Interface Configuration



7 Reference Design

Please see Gowin LPC Peripheral IP [Reference Design](#) for details at Gowin website.

8 File Delivered

The delivery file of Gowin LPC Peripheral IP includes documentation and reference design.

Table 8-1 Gowin LPC Peripheral IP Doc. List

Name	Description
IPUG799, Gowin LPC Peripheral IP User Guide	Gowin IP User Guide, namely this one.
RN799, Gowin LPC Peripheral IP Release Note	Gowin IP Release Note

