



Gowin Integer Division IP

Release Note

RN798-1.0E, 07/22/2022

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Revision History

Date	Version	Description
07/22/2022	1.0E	Initial version published.

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About This Guide

This release includes Gowin Integer Division IP User Guide.

Gowin Integer Division IP User Guide is available at Gowin website. Specific parameters had been taken as an example for the reference design, which can be used for simulation and instantiation of the overall synthesis, placement and routing after user design.

Overview

Gowin Integer Division IP can implement integer division, output quotients and remainders.

Table 1 Gowin Integer Division IP Overview

Gowin Integer Division IP	
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.8.07 and above)

Documents

The software release file contains Gowin Integer Division IP User Guide, which is listed in below.

Table 2 Document List

Documents	Description
IPUG798 , Gowin Integer Division IP User Guide	PDF
RN798, Gowin Integer Division IP Release Note	PDF

IP Support

Since the requirements of user design and the maximum frequency are different, the reference design does not include FPGA specific location (.cst) and timing constraints (.sdc) documents, and you can determine the location and timing constraints on your own.

For the customized IP design and support, please contact Gowin sales and support line.

Website: www.gowinsemi.com

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