



Gowin Integer Division IP

User Guide

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Revision History

Date	Version	Description
07/22/2022	1.0E	Initial version published.
04/27/2023	1.1E	● Fraction output supported. ● I/O list updated. ● Table 3-1 Gowin Integer Division IP Resource Utilization updated.

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1 About This Guide

1.1 Purpose

Gowin® Integer Division IP User Guide mainly includes the descriptions of the functions, features, ports, timing, call and configuration, and reference design, etc. It mainly helps you quickly understand the features, characteristics and usage of the Gowin Integer Division IP products.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com.

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS821, GW1NS series of FPGA Products Data Sheet](#)
- [DS871, GW1NSE series of FPGA Products Data Sheet](#)
- [DS881, GW1NSER series of FPGA Products Data Sheet](#)
- [DS861, GW1NSR series of FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS971, GW2ANR series of FPGA Products Data Sheet](#)
- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
ALU	Arithmetic Logical Unit
FPGA	Field Programmable Gate Array
IP	Intellectual Property
LUT	Look-up Table

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Gowin Integer Division IP Overview

Gowin Integer Division IP is designed to realize integer division operations with less logic resources.

Table 2-1 Gowin Integer Division IP Overview

Gowin Integer Division IP	
IP Core Application	
Logic Resource	Please refer to Table 3-1.
Delivered Doc.	
Design Files	Verilog
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.8.07 and above)

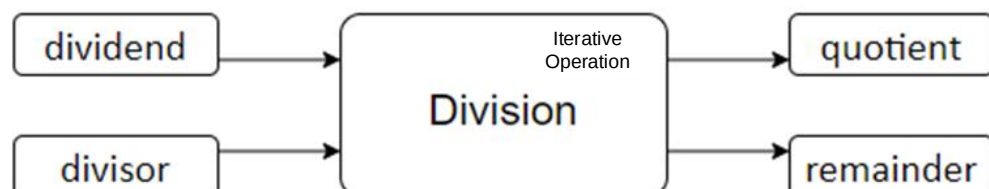
Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Introduction to Gowin Integer Division IP

Gowin Integer Division IP is an IP designed to provide users with the purpose of implementing division between integers and outputting quotient and remainder blocks, and its structure diagram is as shown in Figure 2-1.

Figure 2-1 Gowin Integer Division IP Structure Diagram



3 Features and Performance

3.1 Features

- Supports signed and unsigned integer division operation
- Input data bit width supports 4-64 bits
- Supports "With Remainder"/"Without Remainder"/"Always Positive Remainder", and "Fractional" output
- The output latency can be configured

3.2 Max. Frequency

The max. frequency of Gowin Integer Division IP is mainly determined by speed grade of the selected devices.

3.3 Latency

The output latency of Gowin Integer Division IP is determined by the configuration parameters.

3.4 Resource Utilization

Integer Division can be realized by Verilog language. Its performance and resource utilization may vary when the design is employed in different devices, or at different density, speed grade.

Take the GW2A-55 FPGA as an example. See Table 3-1 for the resource utilization. For the applications on the other GOWINSEMI devices, please refer to the later release.

Table 3-1 Gowin Integer Division IP Resource Utilization

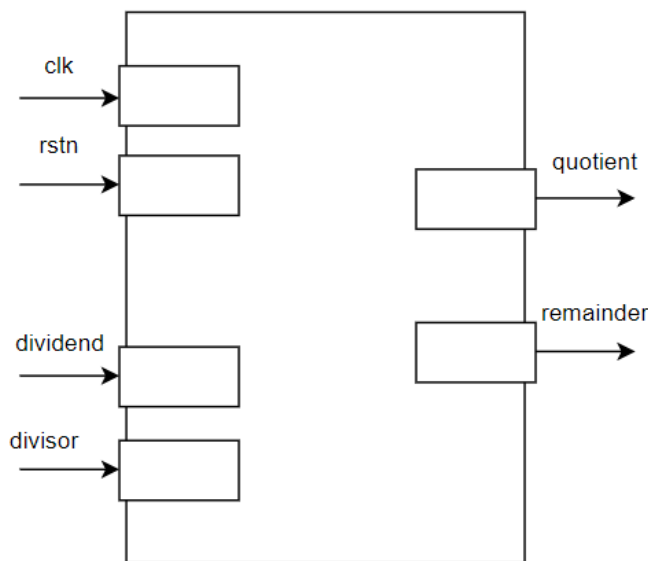
Device	Speed Grade	Resource Name	Resource Utilization
GW2A-55	C8/I7	LUTs	1366
		ALUs	598
		Registers	1471
		I/O Buffer	134

4 Functional Description

4.1 Integer Division Structure and Function

Gowin Integer Division IP can realize signed and unsigned integer division operations. And you can configure parameters as required when generating the module. The structure diagram is as shown in Figure 4-1.

Figure 4-1 Gowin Integer Division IP Interface Implementation



4.2 Data Setting

You can select input data as signed or unsigned through GUI. And you can configure the bit width of the input data dividend and divisor separately, with a maximum bit width of 64 bits and a minimum bit width of 4 bits.

4.3 Remainder Mode Selection

You can select three remainder output modes through GUI, including remainder (the sign of the remainder is identical to the sign of the divisor), non-remainder, and positive remainder.

5 Port Description

For the detail IO port description of Gowin Integer Division IP, see Table 5-1. The structure diagram is as shown in Figure 4-1.

Table 5-1 Gowin Integer Division IP I/O Port List

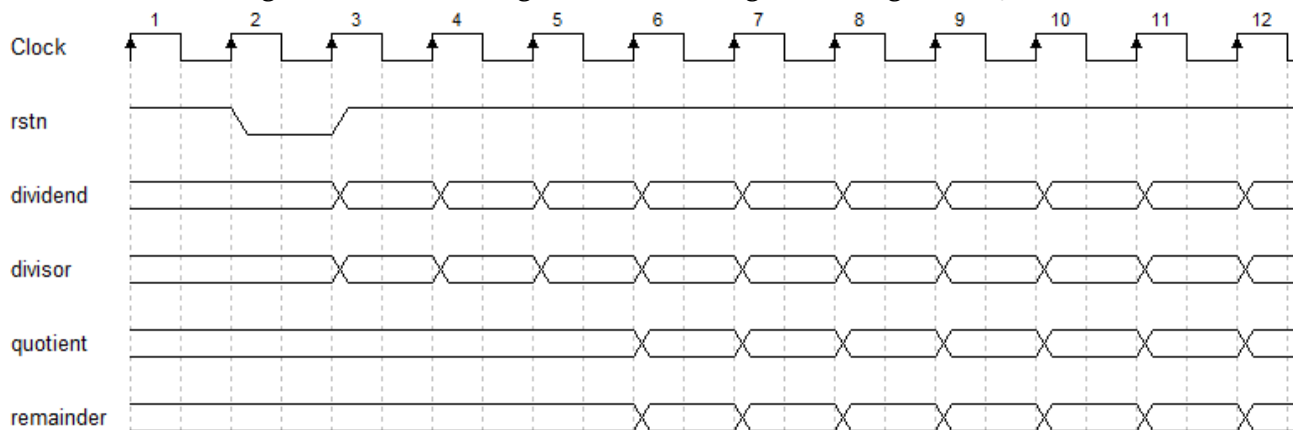
Signal	I/O	Width	Description
clk	Input	1	Clock signal
rstn	Input	1	Reset signal, active-low
dividend	Input	4-64	Input dividend
divisor	Input	4-64	Input divisor
quotient	Output	4-64	Output result: Quotient (its bit width is equal to that of dividend)
remainder	Output	1-64	Output result: Remainder (its bit width is equal to that of divisor)

6 Timing Description

This chapter mainly introduces the timing of Gowin Integer Division IP.

Integer Division Signal Timing

Figure 6-1 Gowin Integer Division IP Signal Timing, Latency = 3



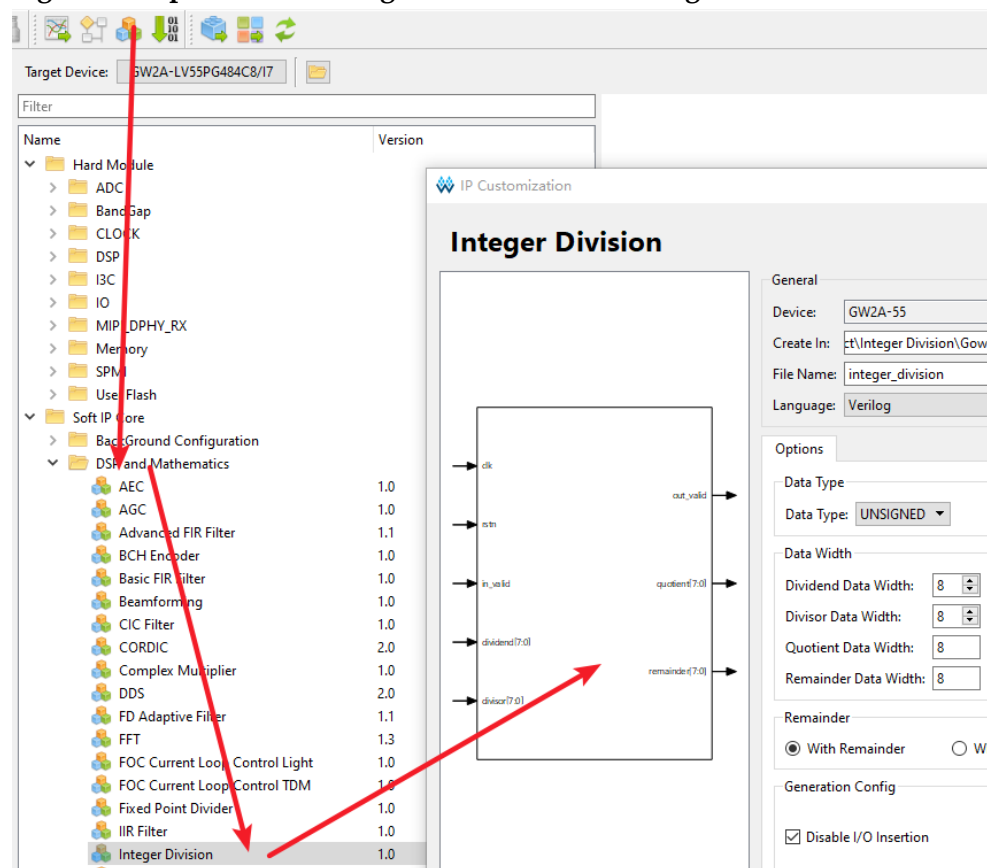
As shown in Figure 6-1, when the latency is set to 3, for the first input dividend and divisor, the quotient and remainder will be output after 3 clocks.

7 GUI Configuration

7.1 Invoke IP

Start "IP Core Generator" from the "Tools" menu in the Gowin Software, then you can call and configure "Integer Division" in "DSP and Mathematic". Toolbar icon is also available as shown in Figure 7-1.

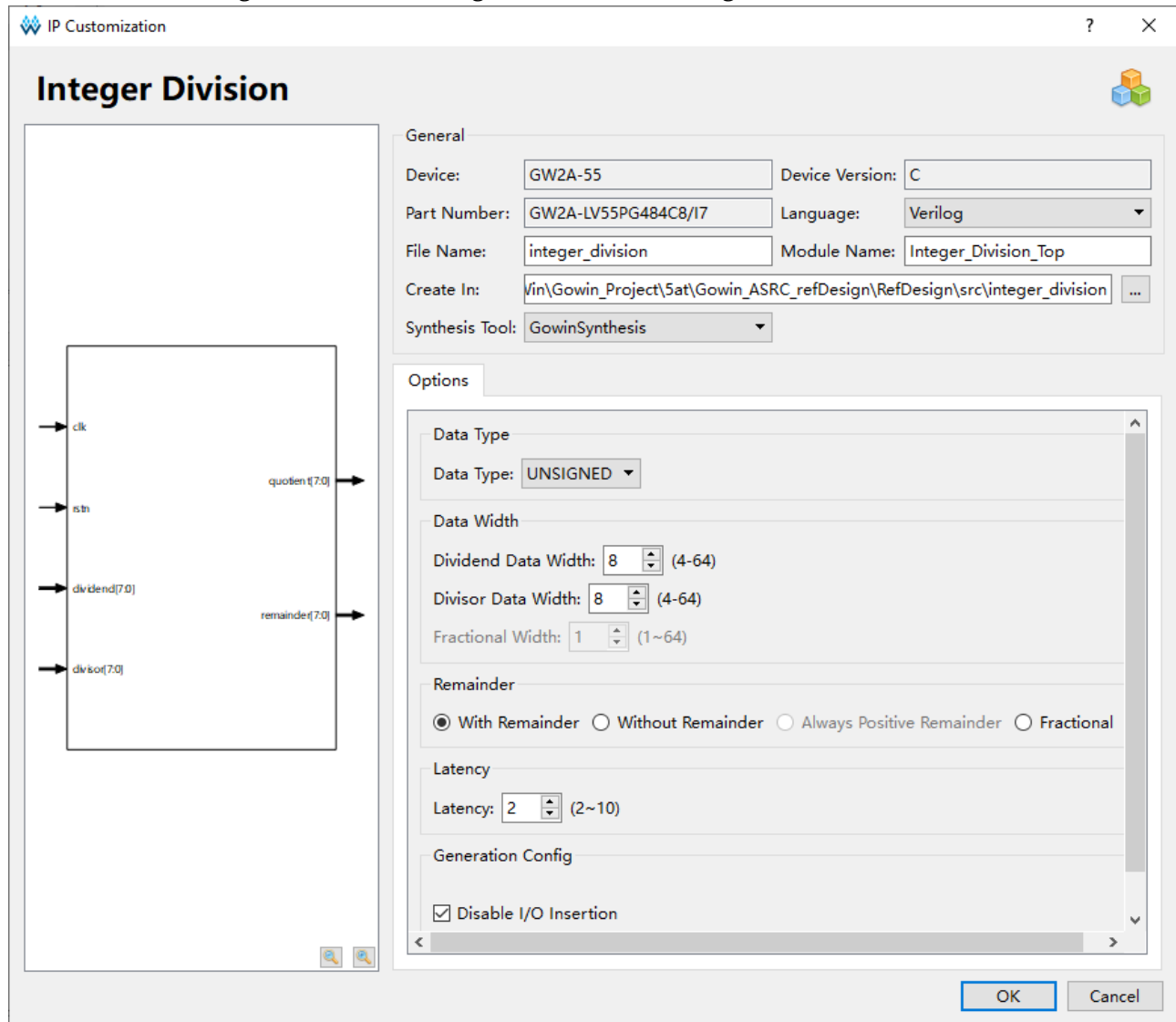
Figure 7-1 Open the IP Configuration Interface Through Toolbar Icon



7.2 Configuration Interface

Gowin Integer Division IP configuration interface is as shown in Figure 7-2.

Figure 7-2 Gowin Integer Division IP Configuration Interface



- "Create In" displays the path of IP core folder, and you can modify the path.
- "File Name" displays the generated IP name, and you can modify the name.
- "Module Name" displays the generated IP module name, and you can modify the name.

8 Reference Design

For the reference design of Gowin Integer Division IP, please refer to the related test cases in [RefDesign](#).

9 Documents Delivered

The delivery file for Gowin Integer Division IP includes documents and reference design.

Table 9-1 Gowin Integer Division IP Document List

Name	Description
IPUG798, Gowin Integer Division IP User Guide	Gowin IP User Guide, namely this one
RN798 , Gowin Integer Division IP Release Note	Gowin IP Release Note

